The Mysterious Bipolar Bias Temperature Stress from the Perspective of Gate-Sided Hydrogen Release

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***Abstract*— While the bias temperature instability has provided many puzzles for more than half a century, the observation that bipolar ($+V_g/-V_g$) AC stress can lead to larger degradation than DC or unipolar ($V_g/0$) AC NBTI/PBTI combined, is particularly mysterious. Interestingly, similar observations have been made for oxide breakdown and hot carrier injection. Both have been linked to accelerated hydrogen release from the oxide under alternating positive and negative bias which then causes the creation of near-interface states. Based on these observations, we investigate the phenomenon from the perspective of the recently proposed gate-sided hydrogen release model for BTI. We suggest a mechanism which can explain the accelerated degradation observed during bipolar AC stress and investigate and validate possibilities for mitigating the effect by reducing the oxide volume from which H is released.**

I. Introduction

Based on the vast experimental and theoretical knowledge available on the behavior of H in semiconductor devices, we have recently suggested the gate-sided hydrogen release (GSHR) model to explain a range of peculiarities observed in bias temperature instabilities (BTI) [1–4]. The GSHR model is based on previously suggested models for irradiation damage [5] and incorporates experimental evidence that during BTI stress H tends to migrate from the oxide towards the interface [6]. A defining feature of the GSHR model is that once the H reaches the channel side of the insulator, it can become trapped again to create new oxide defects, for instance hydroxyl-E' centers [7–9] (donor-like oxide defects), or break Si-H bonds directly at the Si/SiO_2 interface to create P_b-centers [10]. During recovery, the H trapped in oxide defects moves back to its original positions. Note that the GSHR model is fundamentally different from the reaction-diffusion (RD) model as it assumes the reactions of H to be rate limiting rather than the actual diffusion, which is very fast [11]. As a consequence and consistent with experimental observations [6], in the GSHR model hydrogen moves in opposite directions as postulated by the RD model. In addition, the parameters of the GSHR model are consistent with independent experiments as well as theoretical considerations, while those of the RD model are not [11, 12]. Contrary to previously used models, which focus on the time evolution of ΔV_{th} in pMOS devices, we have shown that the GSHR model can consistently explain ΔV_{th}, ΔV_{FB}, ΔN_{ot} and ΔN_{it} during NBTI and PBTI in both pMOS and nMOS devices [13] as seen in MSM and CV measurements. This is insofar important as ΔV_{th} measured in (non-HK) nMOS devices is typically much smaller than ΔV_{FB} and the standard assumption nMOS devices is much smaller than in pMOS devices only valid for ΔV_{th} shifts [13]. The reason for this discrepancy is because in these devices donor-like traps with energy levels below the Si conduction band dominate the degradation which are mostly neutral during V_{th} measurements in nMOS devices but clearly visible in CV data.

Independently of BTI, the release of H from the SiO_2 as a response to various stimuli has been studied from many different angles. For instance, it has long been known [14] that the injection of electrons into positively charged traps causes H release and subsequently the creation of N_{it}. This mechanism has been invoked e.g. to explain *post-stress* degradation after hot-carrier stress [15] or the instability observed after vacuum ultraviolet irradiation [16]. The important aspect in all these studies seems to be that the oxide defects have to be *positively charged first and upon neutralization release a H atom* [17]. Similar conclusions have been drawn for time-dependent dielectric breakdown (TDDB), where it has been speculated that H redistribution in the oxide first leads to stress-induced leakage currents (SILC) and subsequently to oxide breakdown [18–20].

The most likely explanation here is that H-related oxide defects lose their H upon neutralization [17]. These H can become trapped again at different oxide sites, break Si-H bonds at the interface or passivate dopants. The details of the H release mechanism remain speculative, but it has been suggested that the excess energy provided by the tunneling electrons is responsible [18, 20], an explanation not applicable to our low-energy BTI experiments.

Along similar lines, it has been observed that bipolar BTI stress can lead to more severe degradation than DC or AC NBTI/PBTI stress combined [21–24]. This is insofar puzzling as PBTI and NBTI are typically considered independent phenomena. If one rapidly switches between the two, one expects to roughly obtain the sum of AC PBTI and NBTI degradation. We will demonstrate in the following that the H release mechanism caused by electron injection into positively charged traps perfectly fits the AC NBTI/PBTI scenario and also supports the GSHR model.

II. Experimental

To understand the physics of bipolar BTI stress, we perform multi-frequency CV (1 kHz – 1 MHz) measurements on large-area (50 µm × 50 µm) pure SiO_2 pMOS (p-channel) and nMOS (n-channel) capacitors with a junction ring, subjected to DC, unipolar AC (AC for short), and bipolar AC (bipolar for short) stresses. If not explicitly specified, 100 kHz CV data are shown. During AC stress, the bias supply of the LCR used for the CV measurements is digitally switched between V_s and zero at 0.5 Hz. For bipolar stress, $\pm V_s$ is applied. To avoid

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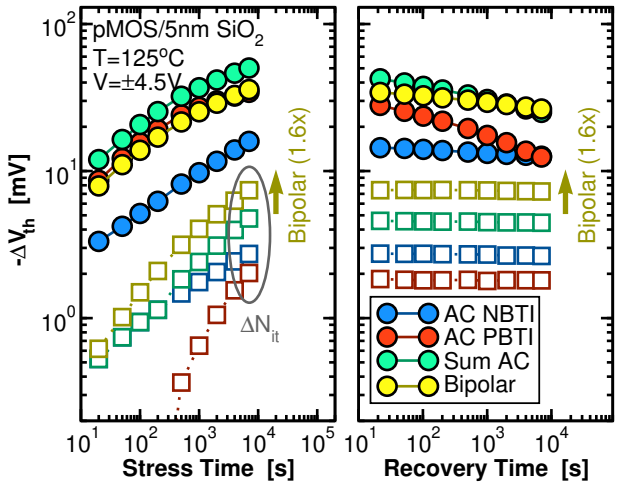

Fig. 1. Comparison of $\Delta V_{\rm th}$ after AC NBTI, AC PBTI, and bipolar BTI for the 5 nm SiO_2 pMOS. $\Delta N_{\rm it}$ following bipolar BTI is 60% larger than the sum of AC NBTI and AC PBTI. (CV @ 100 kHz).

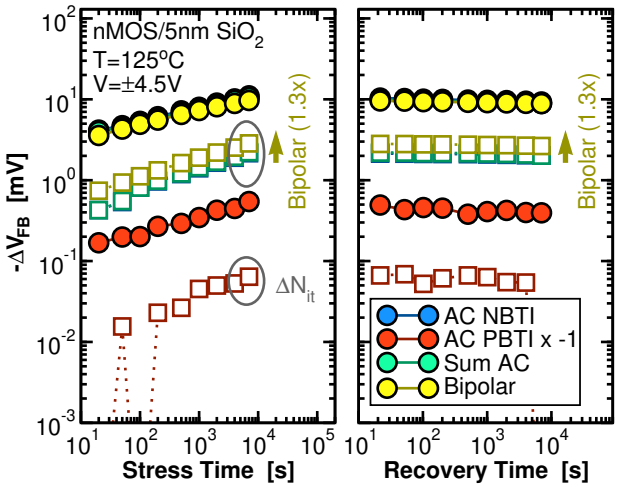

Fig. 2. Same as Fig. 1 but for the nMOS. Shown is $\Delta V_{\rm FB}$ which is more relevant than $\Delta V_{\rm th}$ for nMOS devices. $\Delta N_{\rm it}$ following bipolar BTI is 30% larger than the sum of AC NBTI and AC PBTI. Note that $\Delta V_{\rm FB}$ after AC PBTI is positive [13].

excessive leakage currents, which would interfere with our CV measurements, we chose relatively thick SiO_2 insulators with $t_{\rm ox}$ = 5 nm. In addition, we used a process split in which a 2 nm ALD layer of HfO_2 was deposited onto the same 5 nm SiO_2 layer. Due to scavenging, the EOT of this HK stack was nearly equivalent to the pure SiO_2 samples, allowing for a fair comparison at the same stress voltages. We extract $\Delta V_{\rm th}$, $\Delta V_{\rm FB}$ and $\Delta D_{\rm it}(E)$ from the CV measurements using the simple methodology suggested previously [13]: after determining $\Delta V_{\rm th}$ and $\Delta V_{\rm FB}$ from the CV measurements at the two gate voltages corresponding to $(C_{\rm min}+C_{\rm max})/2$, we use these extracted values for $\Delta V_{\rm th}$ and $\Delta V_{\rm FB}$ to linearly correct for the stretch-out between the current and initial CV curve at the respective frequency. With the stretch-out correction, the true change in the capacitance due to interface/border states, $\Delta C(E)$, can then be estimated and converted to $D_{\rm it}(E)$. By

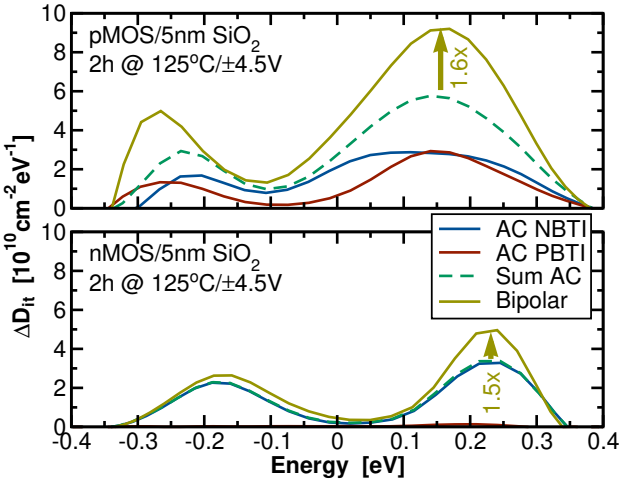

Fig. 3. Comparison of $\Delta D_{\rm it}$ after a 2h stress for the 5 nm SiO_2 pMOS (top) and nMOS (bottom), showing the increase of the peak $\Delta D_{\rm it}$ following bipolar BTI by 60% and 50%, respectively. Note that the impact of PBTI on $\Delta D_{\rm it}$ is negligible in the nMOS.

integrating $D_{\rm it}(E)$ over the bandgap we obtain $\Delta N_{\rm it}$, which is then sometimes converted to an equivalent $\Delta V_{\rm th}^{\rm it}$ shift assuming all $\Delta N_{\rm it}$ to be positively charged (donor-like states) to provide an upper bound for their contribution.

III. Results and Discussion

The extracted $\Delta V_{\rm th}$ and $\Delta N_{\rm it}$ obtained after AC NBTI, AC PBTI, and bipolar BTI stress are shown in Fig. 1 for the pMOS. While the measured $\Delta V_{\rm th}$ was about the same, $\Delta N_{\rm it}$ *after* bipolar stress is 60% larger than the sum of AC NBTI/PBTI. Analogous results for the nMOS are shown in Fig. 2. However, since $\Delta V_{\rm th}$ in nMOS transistors does not reveal the full amount of degradation caused by the donor-like traps, $\Delta V_{\rm FB}$ is shown [13]. Note that while PBTI is extremely small in the nMOS, 30% larger degradation than AC NBTI is obtained in the bipolar case. Note the large peak in the upper half of the bandgap seen in the $D_{\rm it}$ profiles of Fig. 3, suggesting the creation of H-related defects [25–30]. This is supported by the f-dependent CV results shown in Fig. 4. Particularly for the pMOS, even at 1 MHz the $D_{\rm it}$ clearly differs from what is expected from $P_{\rm b}$-centers [31].

Fig. 5 shows the typical (standard) defect bands of SiO_2 as available in our compact physics BTI simulator Comphy [33] for PBTI and NBTI stress. In order to be consistent with the suggested H-release mechanism, the hole traps (lower band) have to change their charge state between the negative and positive voltages. The four-state non-radiative multiphonon (NMP) model [34] of the hydroxyl E' center provides a consistent mechanism for H release, see Fig. 6. DFT calculations show [35] that during the short transition of the metastable states 1' and 2', additional pathways for H release from the defect are possible. As the defect only remains in states 1' or 2' for a short time, repeated switching increases the likelihood [36]. This also consistently explains the previously observed f-dependence of bipolar BTI [24], as the more often the

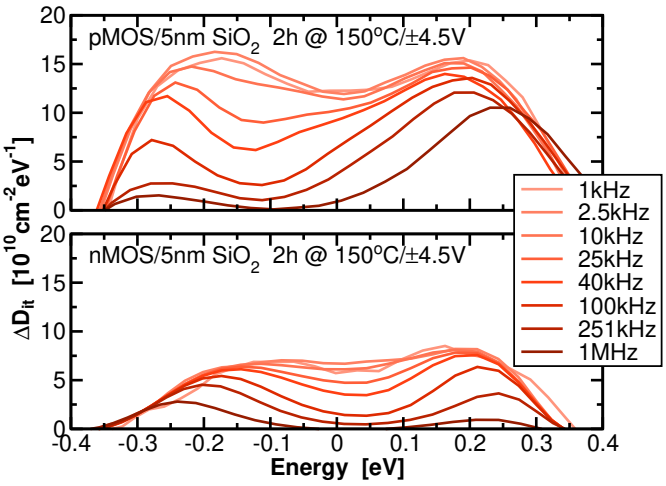

Fig. 4. CV-frequency dependence of ΔD_{it} after a 2h bipolar stress for the 5 nm SiO_2 pMOS (top) and nMOS (bottom). The peak in the upper half of the bandgap remains large even at 1 MHz, indicating the presence of very fast hydrogen-related border traps for the pMOS while the high-frequency nMOS data resembles the D_{it} know from P_b-centers.

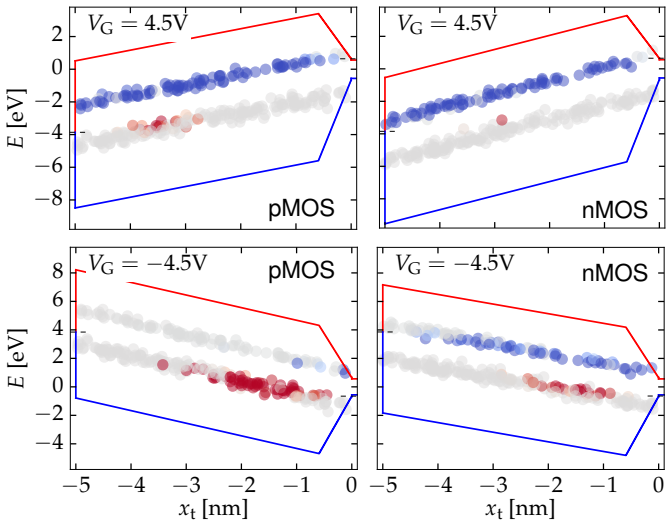

Fig. 5. Depending on the bias scenario and the transistor type, H relocates from different regions. The major difference between pMOS and nMOS is that in the latter the H related defects do not become positively charged during the PBTI phase and therefore subsequent electron injection during the NBTI phase does not lead to accelerated H release.

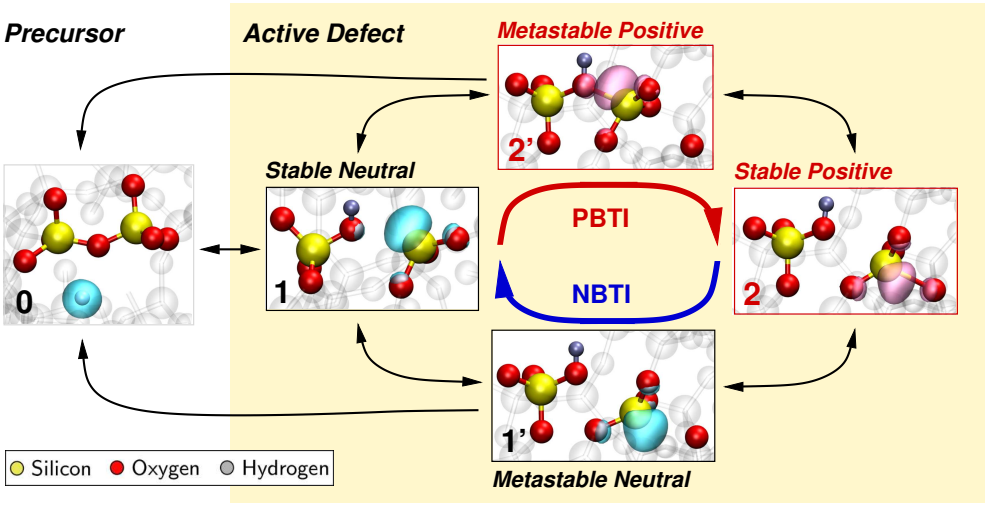

Fig. 6. Accelerated H release can be explained in the 4-state NMP model via an additional transition path away from the metastable states 1' or 2' towards the (inactive) precursor state 0. For this the defect needs to be repeatedly switched between states 1 and 2. Shown is a gate-sided defect, which becomes positively charged during PBTI stress (contrary to channel-sided defects).

defects are cycled between states 1 and 2, the more often the metastable states are transitioned.

The f-dependence is investigated in Fig. 7. In order to provide a clean HF signal to the gates, a 1MHz sine-stress is used. As expected, the HF bipolar stress leads to a significant change in the time dependence, in particular, an upward slant of the degradation curve. This would result in a significant reduction of lifetime.

Since the suggested mechanism requires oxide defects to become positively charged at the gate side, it is interesting to study the onset of the bipolar degradation effect. Fig. 8 confirms that for bipolar stress between −4.5 V and variable V_H, the effect kicks in for $V_H > 1$ V, providing additional support to the model.

A primary requisite of the GSHR model is the availability and release of H at the gate side of the insulator [35]. Consequently, modifying the insulator by adding a 2 nm HfO_2 layer on top of the SiO_2 will have a strong impact on the generated D_{it}. The band diagram and standard defect bands for this HK stack are shown in Fig. 9. Due to the changed geometry of the stack, the region where H used to be primarily released in the pure SiO_2 stack is now replaced by HfO_2. As a consequence, a drastic impact on the creation of interface states in general and the bipolar effect in particular is expected. This is confirmed experimentally in Fig. 10, where first of all PBTI is dramatically reduced together with a reduction of bipolar ΔN_{it} from 60% down to about 20%, albeit at the price of an overall increase in ΔN_{it} (also see D_{it} profiles in Fig. 11). While HfO_2 is also known for being able to store H, the barriers for release appear to be smaller, hence the

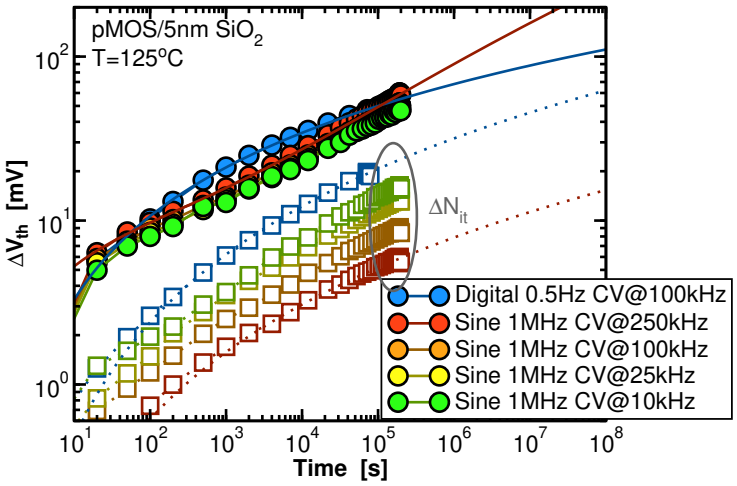

Fig. 7. For higher frequencies of the bipolar stress, the whole shape of the $\Delta N_{it}(t)$ curve changes. The solid/dotted lines are fits to the error-function model [32] and predict vastly different lifetimes for HF bipolar stress.

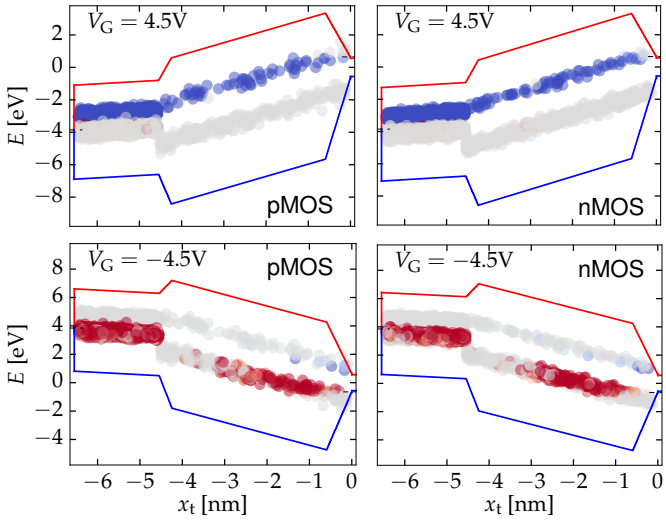

Fig. 9. When a HfO_2 layer is placed on top of SiO_2, the HfO_2 resides in the location where H is released in the pure SiO_2 stack. Apparently, while H can also be stored and released from HfO_2, the mechanism is simpler and is not accelerated when the defects are first charged positively.

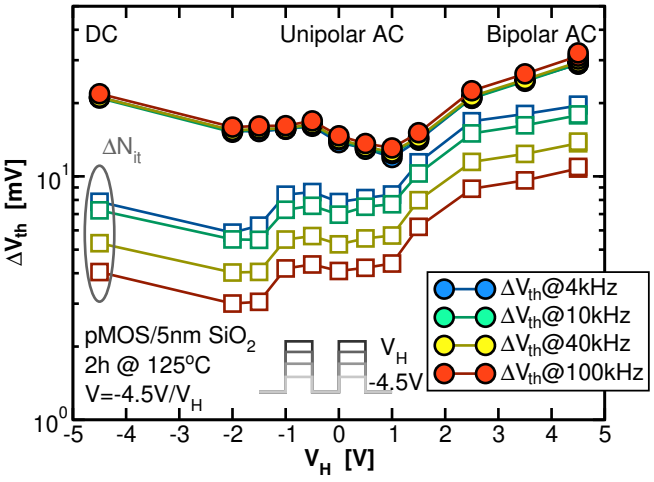

Fig. 8. Comparison of ΔV_{th} after BTI stress between $-4.5\,V$ and varying V_H. As special cases we obtain DC ($V_H = -4.5\,V$), unipolar AC ($V_H = 0\,V$), and bipolar AC ($V_H = +4.5\,V$) stress. For $V_H > 1\,V$ (sufficient number of positively charged defects), ΔN_{it} begins to increase rapidly.

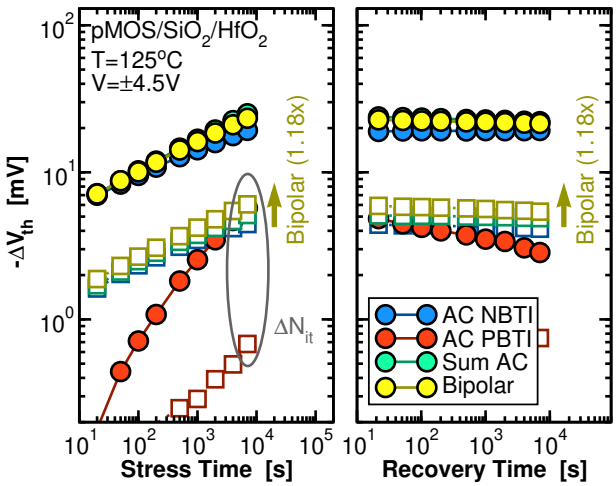

Fig. 10. Comparison of ΔV_{th} after AC NBTI, AC PBTI, and bipolar BTI for the 5 nm SiO_2/2 nm HfO_2 pMOS. ΔN_{it} following bipolar BTI is only about 18% larger than the sum of AC NBTI and AC PBTI.

increase in N_{it}. In addition, the release mechanism appears to be simpler as compared to SiO_2. Interestingly, even though both samples see about the same electric field at the Si/SiO_2 interface, N_{it} is larger in the HK sample, either due to the larger H concentration of the HK stack or the more efficient release of H from HfO_2. These results also confirm that it is not the field at the interface which drives the creation of N_{it}.

Finally, the two technologies are compared in Fig. 12. While in both technologies bipolar BTI is larger than DC, the HK stack shows a strongly reduced bipolar effect, both in terms of relative magnitude as well as in terms of the troublesome time slope, consistent with our arguments.

IV. Conclusions

We have investigated the mysterious effect of AC bipolar BTI, which defies expectations by being stronger than the combined effect of unipolar AC NBTI and PBTI, as well as pure DC stress. Using the well established fact that electron injection into positively charged traps leads to the release of H, which can then create near-interface states, we argue that the gate sided hydrogen release model is perfectly consistent with experimental data. In particular, modification of the dielectric by adding a HfO_2 layer without modifying the EOT, significantly reduces the bipolar effect, consistent with the idea that H release is no longer accelerated by bipolar switching in the HfO_2 layer.

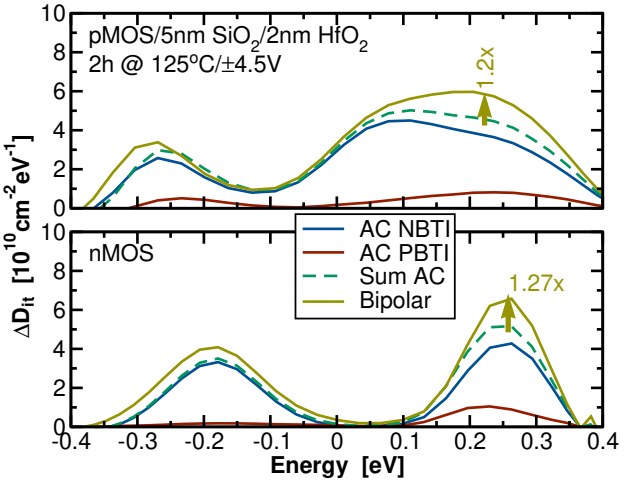

Fig. 11. Comparison of ΔD_{it} after a 2h stress for the 5 nm SiO_2/2 nm HfO_2 pMOS (top) and nMOS (bottom), showing the increase of the peak ΔD_{it} following bipolar BTI by 20% and 15%, respectively.

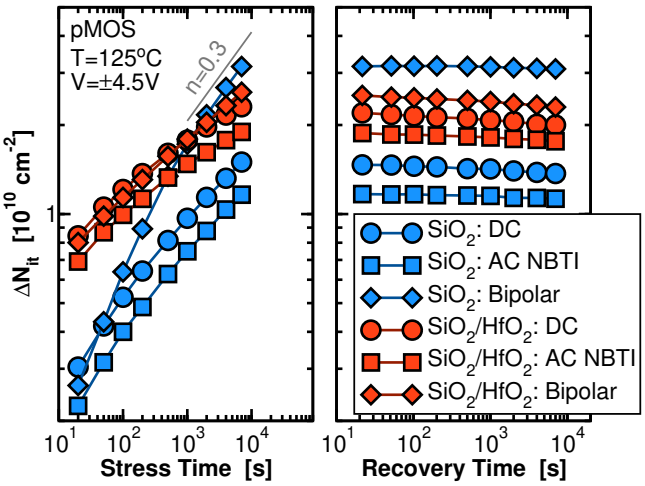

Fig. 12. Comparison of ΔV_{th} after DC NBTI, AC NBTI, and bipolar BTI for the 5 nm SiO_2 and 2 nm HfO_2 pMOS. While bipolar BTI is larger than DC BTI, the bipolar effect is much stronger in the SiO_2 FET, both in terms of relative increase and, particularly troublesome, time slope $n = 0.3$ (vs. 0.19).

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