On the impact of mechanical stress on gate oxide trapping

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***Abstract*—The electrical performance and reliability of MOSFETs and charge-trap flash memories are influenced by the traps in the gate dielectric. Trap properties depend on the atomic structure of the dielectric and are thus expected to be affected by mechanical stress, which modifies the bonds between atoms. Consequently, the mechanical stress, either engineered or created as a side effect of fabrication, needs to be considered in order to improve the device performance and reliability. This work demonstrates a systematic and controlled experimental study of the trapping process in individual gate oxide defects under externally applied mechanical stress. The significant and reversible impact of the mechanical stress on the trapping behavior is demonstrated and a theory to explain the observations is proposed.**

***Index Terms*-- Mechanical stress, oxide traps, TDDS, FEM**

I. Introduction

The electrical performance and reliability of the MOSFET strongly depend on traps in the gate dielectric. For example, the bias temperature instability (BTI) effect is a major reliability concern related to the trapping process in the gate oxide [1]. In addition, in charge-trap flash memories, gate dielectric defects are crucial for memory operation [2]. An aspect that has not received a lot of attention yet is the impact of mechanical stress (MS) on the trapping behavior. MS modifies lengths and angles of bonds between the atoms in dielectric [3] and thus can potentially alter the properties of the traps (e.g., increase the trap energy level [4], Fig.1, but also other "internal" barriers [5]).

MS can reside in the device as a side effect of fabrication, and this is especially true for 3D integration [6, 7]. The produced MS levels depend on the structure design as well as the processing conditions, and values ranging from a few hundred MPa to some GPa can be found in the literature [7, 8]. MS can also be deliberately engineered (e.g., using SiGe source/drain stressors), as has been done from the 90 nm node of CMOS technology. The MS engineering techniques include but are not limited to the use of SiGe source/drain stressors and Si_3N_4 contact etch-stop layers [9]. MS as high as 1.5 GPa [10] induced by SiGe S/D was previously reported.

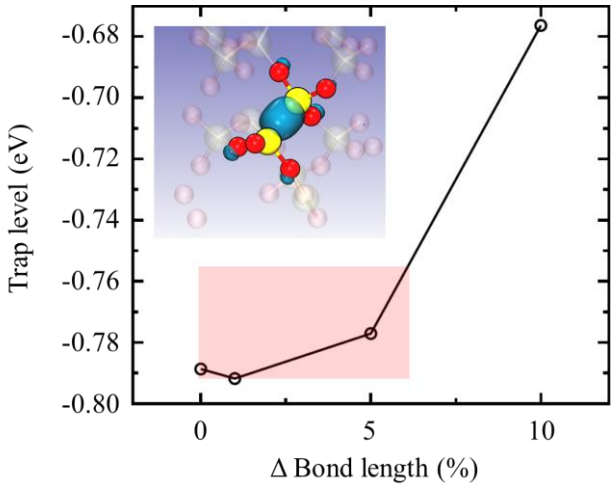

Figure 1. *First-principles calculation (inset) of the effect of varying atomic bond lengths on the SiO_2 oxygen vacancy level (inset) [4]. With the SiO_2 Young's modulus of ~100 GPa, the maximum MS of ~6 GPa achievable by nanoindentation (Fig. 3) should have at most a weak impact on the trap level (red region).*

It is, thus, of high interest to investigate the impact of MS on gate oxide trapping. This work proposes an experimental approach that relies on electrical characterization of the trapping process, at the individual trap level, during the application of external force (and thus MS) with a nanoindenter. The nanoindenter allows to control the amplitude of the force and the position of its application. It can produce much higher MS values compared to bending techniques. It was used before to study impact of MS on device performance for FinFETs and 3D NAND devices [11, 12], but it was never applied to study impact of stress on traps. Thus, the proposed technique provides the means for systematic and reproducible tests required to gain fundamental

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understanding of the impact of MS on the trapping behavior in the gate dielectric.

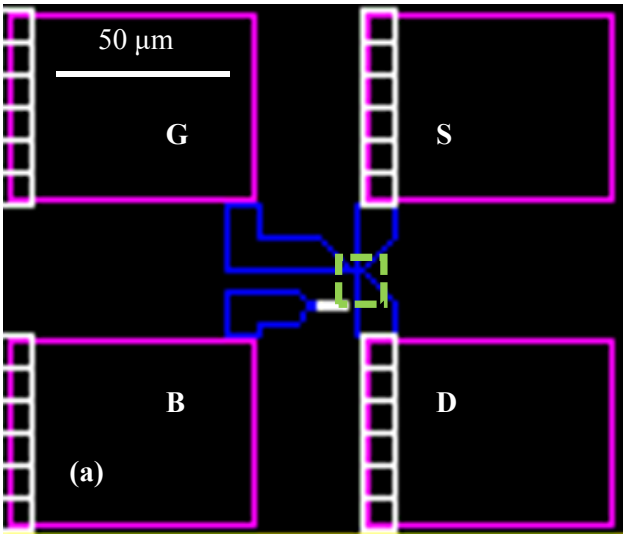
II. Device and Methodology

To characterize gate oxide trapping under MS we performed Time Dependent Defect Spectroscopy (TDDS) [13] while applying external mechanical force to the device under test (DUT). The DUT was a planar Si MOSFET featuring a 1.8 nm thick SiON gate dielectric and a L × W = 70 × 90 nm^2 (nominal dimensions; $L_{effective}$ = ~45 nm [14]). Both p-FET and n-FET devices were used in the experiments (with the channel polarity explicitly indicated in corresponding figures captions).

A vertical force ranging from 0.1 to 3 mN was applied to our devices using a cube-corner tip of a Hysitron TI 950 nanoindenter. To position the tip above the gate and to determine the exact tip position, a topography scan was performed before and after force application (Fig. 2).

Stress values produced in the device by each force were calculated using a 3D finite element model (FEM) created in MSC.Marc, Fig. 3 [15]. The model accounts for the device structure, tip geometry (approximated by a conical tip based on calibration [16]), applied force and tip positioning offset. The device topmost layer materials, copper and SiO_2, were modelled as isotropic perfect plastic with a yield stress of 0.5 and 5.5 GPa respectively, while other materials in the model were treated as isotropic linear elastic. According to the model, vertical and compressive MS of ~5.5 GPa is induced in the DUT with a 1.6 mN force (Fig. 3(b)).

The experimental sequence (Fig. 4) consisted of TDDS measurements at different (increasing) forces. Before application of each increasingly higher force (Fig. 4 top row), TDDS was repeated on the mechanically unstressed device to check if it has recovered from the force application (Fig. 4 bottom row). Each TDDS test was performed as follows.



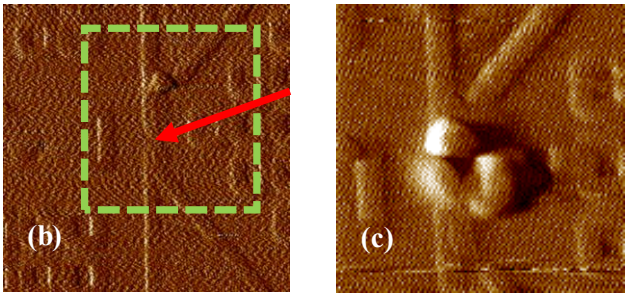


Figure 2. *(a) The layout of the DUT and nanoindenter scan (b) before and (c) after measurement. Despite the visible changes to the top layer morphology, the DUT still operates with almost unmodified IV characteristics (cf. Figs. 6, 7) after mechanical stress is removed. Red arrow: DUT location; green dashed lines: approx. position of the subsequent panel in this figure.*

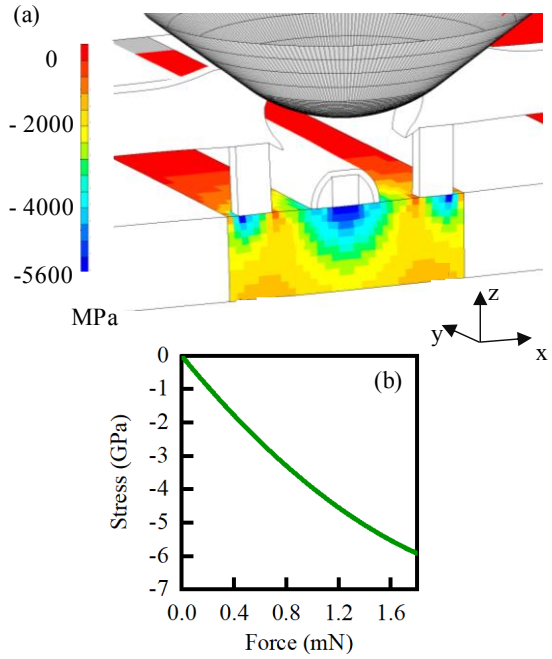


Figure 3. *(a) 3D FEM of the L×W=70×90 nm^2 DUT under mechanical strain in a nanoindenter with a tip ~ 400 nm radius. (Note: wafer passivated after Metal1.) (b) The simulation converts the constant force maintained by the instrument to strain in the DUT.*

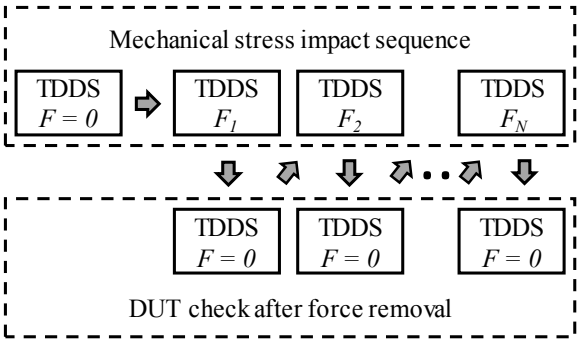


Figure 4. *TDDS is measured on the same DUT with an increasing force (i.e., mechanical stress; top row). Each such TDDS sequence is followed by a TDDS run with no mechanical stress to isolate the impact of the mechanical strain on the trapping process (bottom row).*

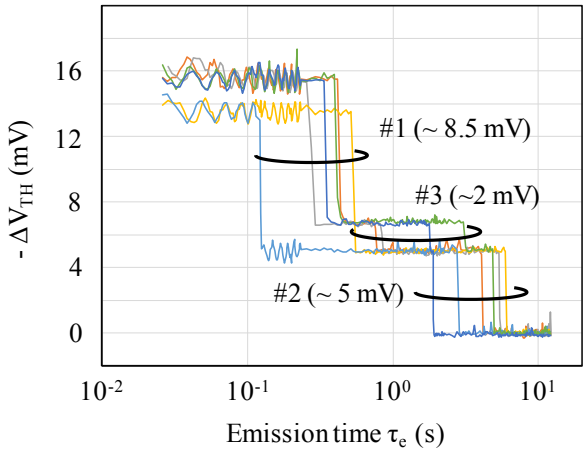


Figure 5. *An example of five TDDS discharging traces measured on a 70×90 nm² pFET after a charging pulse of $V_{G,charges} = V_{TH} - 1.5$ V and 0 mN force applied [cf. Fig. 8(a)]. Signatures of three traps (#1-3) are clearly visible, each with a characteristic emission time (time-to-step) τ_E and impact on the DUT threshold voltage (step height) ΔV_{TH}.*

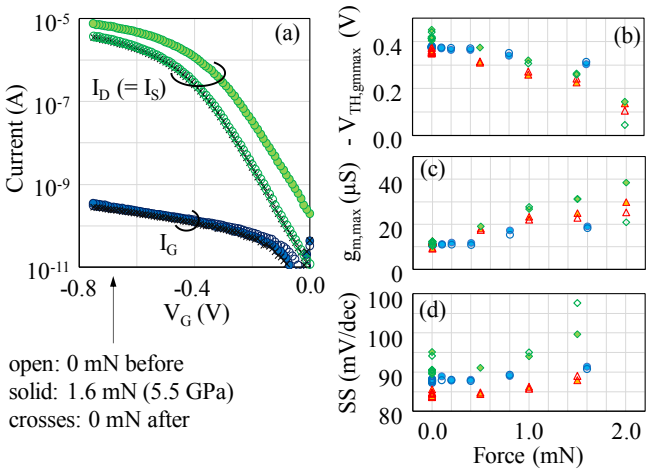


Figure 6. *(a) 70 × 90 nm² pFET $I_{D,S}$-V_G and I_G-V_G characteristics before, during, and after the application of 1.6 mN (5.5 GPa). "Before" and "after" I-V's are almost identical. Mechanical stress does not appear to affect the gate current (at low V_G's) but it (b) significantly decreases $|V_{TH}|$, (c) (by up to 3x) increases transconductance g_m (i.e., the channel mobility), and (d) somewhat degrades subthreshold slope. The device parameters do not vary strongly during TDDS sequences under strain [(b-d) colors: three different DUTs; solid symbols: TDDS start; open symbols: TDDS end].*

First, an initial linear-regime I_D-V_G curve was measured and the device threshold voltage V_{TH} (defined at fixed drain current) was extracted. Then a 1 s long charging pulse with amplitude $V_{G,CH} = V_{TH}$ -1.5 V was applied to the gate to charge the dielectric traps. The pFET drain, source, and bulk were biased at -0.1, 0, and 0 V, respectively. After charging, the drain current was monitored for ~15 s (Fig. 5) for each cycle. Twenty charge-and-discharge traces were measured during force application (limited by the ~5 min nanoindenter drift window) and 50 traces when no force was applied (limited by the total duration of experiment on the manual measurement setup). The minimum detectable charge transition rates were limited by 50 Hz noise emanating from the nanoindenter. A final linear-regime I_D-V_G curve was measured after every TDDS sequence to assess the DUT state. From the recovery steps, the emission times and V_{TH} shifts (deduced from I_D steps using the initial I_D-V_G) of multiple traps were extracted and analyzed as a function of MS.

III. RESULTS AND DISCUSSION

A. *MS impact on FET*

A strong effect of MS on current conduction and gate control is observed in both nFETs and pFETs. As illustrated in Fig. 6 (a), application of compressive MS of 5.5 GPa to the pFET DUT channel significantly impacts its transfer characteristic (which recovers when force is removed) but leaves the (low V_G) gate leakage unchanged. The change in the transfer characteristics shown in Fig. 6 manifests itself as an increase in the maximum drain current I_D due to a strong (up to ~3×) increase in transconductance g_m, i.e. the carrier mobility, under compressive MS. A decrease in $|V_{TH}|$, combined with a slight subthreshold swing (SS) increase are then responsible for an increased leakage current I_{OFF}. The change in all mentioned parameters can be ascribed to a significant reduction in the Si band gap E_G at GPa's of MS. For example, for 5.5 GPa (1.6 mN) E_G was estimated to be 0.52 eV based on deformation potential calculations [17]. E_G will be considerably smaller for 3 mN, consistent with I_{OFF} increase up to 5 orders of magnitude observed in a particular nFET (Fig. 7).

B. *MS impact on oxide trapping process*

MS also has a pronounced impact on gate oxide trapping. As can be seen in Fig. 8, this DUT has three distinguishable dominant traps [#1-3, panel (a)]. All three traps are detectable

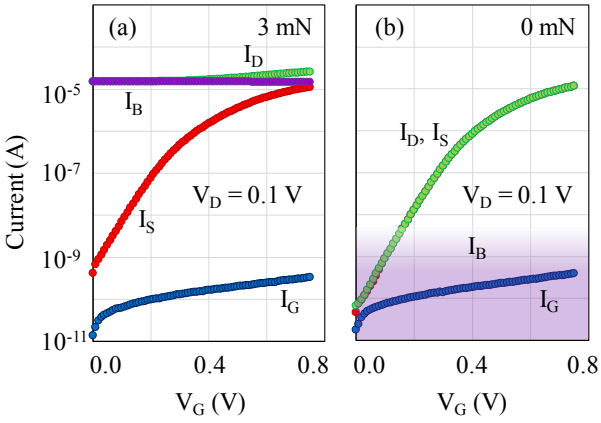


Figure 7. *(a) Application of a substantial, 3 mN, force results in a significant drain-to-bulk junction leakage in a 70×90 nm² nFET. (b) The same DUT after force/MS removal. The DUT operates normally, with I_B below 10^{-8} A (the resolution of the Bulk terminal in the nanoindenter setup, purple region).*

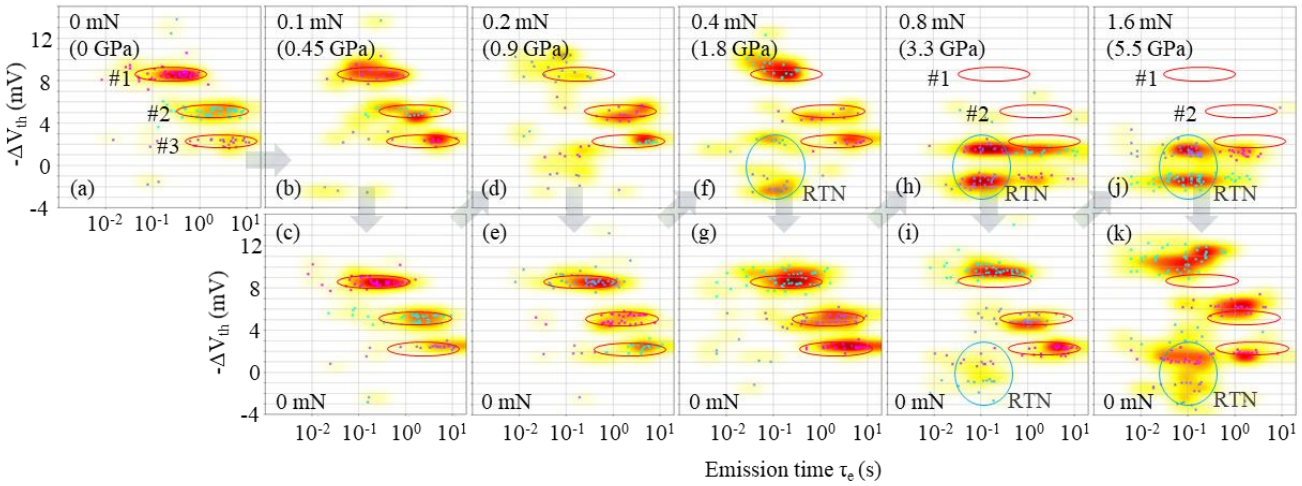


Figure 8. *Impact of increasing mechanical stress on charge trapping. Panels are arranged according to the measurement sequence in Fig. 4. Each panel represents a TDDS spectrum, and each cluster of (τ_e, ΔV_{TH}) points (cf. Fig. 5) in each spectrum represents a "fingerprint" of a single trap in the DUT. Three traps (#1-3) are clearly visible, marked by red ellipses in each panel. All three traps respond up to ~1.8 GPa (trap #2 occupancy appears to dwindle at that point (f)). At higher strains, traps #1 and #2 cease to respond (h,j), but reappear when the strain is removed (i,k). The high strain also induces additional permanent RTN (f-k) and some permanent shifts in trap step heights ΔV_{TH} (h-k).*

at MS below ~1.8 GPa (0.4 mN). When MS is further increased, traps #1 and #2 disappear from the spectrum (Fig. 8 h, j), but return when MS is removed (Fig. 8, i, k). Upon closer inspection, the emission time τ_e of all three traps decreases at high MS (Fig. 9a).

The MS dependence of the trap occupancy (which depends on both emission time τ_e and capture time τ_c) is seemingly more complex (Fig. 9b). The occupancy of trap #1 drops at high MS because its τ_e leaves the limited TDDS range (< 3 decades in time; from ~1/50 s to ~15 s). The measured occupancy of trap #3 increases for the same reason, as its decreased τ_e at high MS enters the TDDS range. Trap #2 has its τ_e safely within the measurement range and the above explanation does not apply. We, therefore, conclude that the occupancy of trap #2 drops because high MS increases its capture time τ_c (trap does not charge at high MS). This observation suggests that MS can be beneficial for pMOS NBTI reliability.

The increase (decrease) of τ_c (τ_e) with elevated MS is consistent with the above observation of high leakage: high MS can strongly reduce Si E_G, which results in both i) high junction leakage (Fig. 10a), and ii) increase of the energy difference between the trap states and the inversion carriers (Fig. 10b). This is also consistent with the expected weak impact of GPa MS on the trap energy level depicted in Fig. 1.

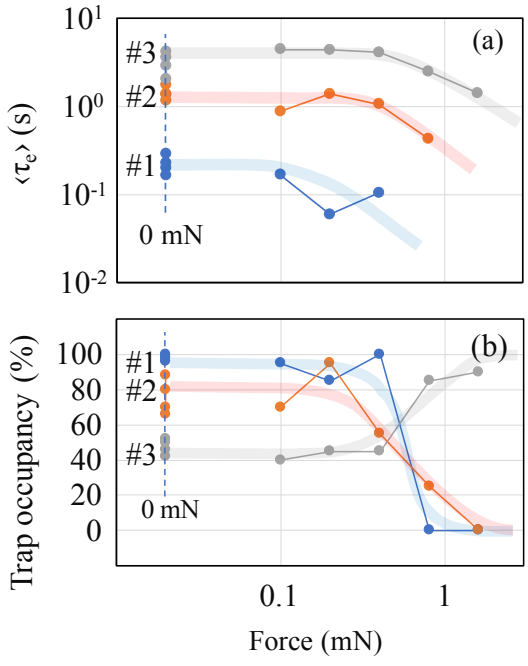


Figure 9. *(a) Emission times ⟨τ_e⟩ of traps #1-3 appear to decrease with increasing MS. (b) Trap occupancy is affected by MS through both ⟨τ_c⟩ and ⟨τ_e⟩ moving in the limited measurement window. (Thick lines serve as guides to the eye.*

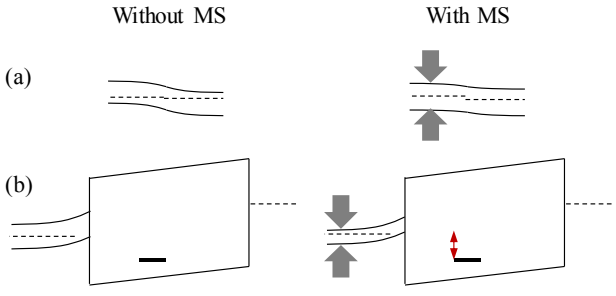


Figure 10. *Schematic explanation of (a) increased drain-to-bulk junction leakage (non-zero $|V_D|$ applied) and (b) reduced trapping through larger channel/trap level misalignment (red arrow) with mechanical stress (MS) reducing Si substrate band gap (bold arrows).*

IV. CONCLUSIONS

A methodology is demonstrated for investigating the impact of GPa mechanical stress (MS) on the trapping and detrapping processes of individual FET gate oxide traps. High MS increases (decreases) trap τ_c (τ_e), consistent with the increase (decrease) of trapping (detrapping) barriers, most likely related to the considerable decrease of Si E_G at GPa MS and documented by strong changes in FET parameters and junction leakage increase. These effects have potential implications for the design and operation of devices with intrinsically or externally induced MS. Further studies are required to investigate the magnitude and type of stress (compressive/tensile) that can be beneficial for improving NBTI and PBTI reliability. In addition, correlating the response of a trap to MS with ab-initio calculations might help identify the type of trap and pave a way for new methods of characterizing defects.

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