Generation of Hot-Carrier Induced Border and Interface Traps, Investigated by Spectroscopic Charge Pumping

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***Abstract*—Hot-carrier degradation in silicon devices is typically assumed to create interface states, so-called P_b centers, which are located at the Si-SiO_2 interface. However, published energy distributions of these interface states do not always agree with the known energetic distribution of P_b centers. We closely investigate these energy profiles caused by hot-carrier stress using spectroscopic charge pumping and compare those to previously published results. It is shown how apparently different profiles can be explained by the additional appearance of border traps. Constant high charge pumping (CP) is used as a tool to additionally characterize those defects. It is found that the CP pulse voltages can have a larger impact on the measured border trap density than the CP frequency, which is usually used to separate border from interface traps.**

***Index Terms*—Hot Carrier Degradation, charge pumping, P_b Centers, Border Traps**

I. Introduction

HOT-CARRIER degradation (HCD) is one of the main degradation mechanisms impeding the quality of the Si-SiO_2 interface in MOS-transistors and has been studied for decades [1]. The dominant microscopic effect driving the degradation is commonly believed to be the dissociation of Si-H bonds at the Si-SiO_2 interface by high-energetic carriers [2], [3] creating dangling Si bonds, i.e. chargeable defects. However, it has also been shown that, additionally to interface defects, border traps are created in the degradation process [4]. We investigate the interplay of border- and interface traps and their influence on the energy density of states in the band gap.

II. Structures and Measurement Procedure

The dedicated test structures (Fig. 1) used for all experiments are lateral Si-nMOSFETs with a channel length of 6 µm, a width of 100 µm and a 30 nm thick SiO_2 insulator. We chose a device with a very long channel to ensure that the dominant microscopic defect creation mechanism is due to single carrier and not multi-vibrational excitations [5]. This ensures that we can adjust the stress dose with the stress temperature [5], where higher temperatures cause milder stress conditions. The material used for the gate electrode is n^{++} doped poly-silicon. The transistors are embedded in a poly-silicon heater setup [6] on wafer-level which will be used to efficiently regulate device temperature. With the help of a three-step calibration procedure of the poly-silicon heater [7], the device can be heated to a well-defined device temperature in the spectroscopic CP experiments which require access to a broad temperature range. In the first step, the transfer characteristics of the device are measured at various chuck temperatures to find a suitable operating point for the drain current which shows a strong temperature dependence. At this operating point (constant drain and gate voltage), the relation between drain current and chuck temperature, which is equal to the device temperature in this step, can be obtained. In the second step, the poly-silicon heater voltage is swept at various chuck temperatures while the drain current at the operating point and poly-silicon heater current are monitored. The drain current can be transformed into device temperature with the previously obtained relation. The poly-silicon heater current yields the power dissipated in the heater. The thermal resistance

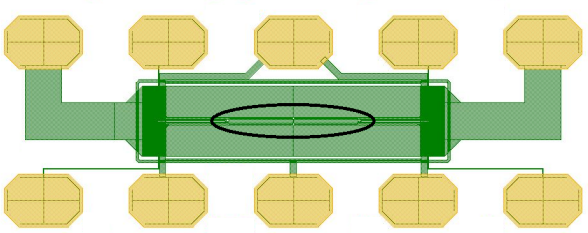

Fig. 1. Layout of the nMOSFET embedded in a poly-silicon heater. The actual transistor is circled in the figure. Same structure as used in [6].

$$R_{\mathrm{TH}}(T) = \frac{\mathrm{d}T}{\mathrm{d}P} \tag{1}$$

can be extracted at each chuck temperature T with a linear regression for small Joule-heated device temperature increases. At last, the device temperature is calculated with [7]

$$T(P) = T_0 - \frac{1}{\alpha} + \left(\frac{1}{\alpha} + T_{\mathrm{chuck}} - T_0\right) \exp\left(\alpha R_{\mathrm{TH}}^{\mathrm{sub},0}\right). \tag{2}$$

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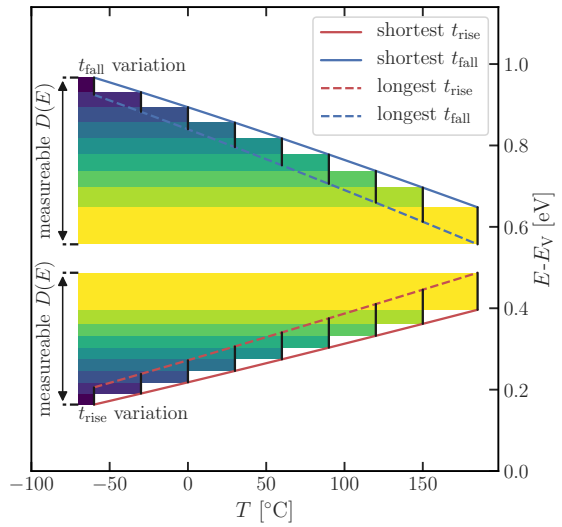

Fig. 2. Principle of spectroscopic CP: The accessible range in the bandgap of CP is varied by sweeping the rise- and fall times of the pulse at different temperatures. This enables energetic scanning of the lower and upper half of the band gap.

The parameters α, $R_{\mathrm{TH}}^{\mathrm{sub},0}$ and T_0 can be extracted from another linear fit while R_{TH} can be modeled as

$$R_{\mathrm{TH}} = R_{\mathrm{TH}}^{\mathrm{sub},0}\left(1+\alpha\left(T-T_0\right)\right). \tag{3}$$

The base temperature of the wafer is always set to -60 °C for all experiments, except the aforementioned calibration process.

With the help of this poly-heater setup, the efficient application of the spectroscopic charge pumping method [8] is possible. This charge pumping (CP) approach allows obtaining the energetic density of trap profiles with a high sensitivity. The method relies on the variation of rise- and fall times of the CP pulse, as well as the variation of measurement temperature to energetically scan the band gap. As a consequence of varying these parameters, parasitic emission, which lowers the scan-able band gap of CP, is modified, thereby allowing for the extraction of the energetic trap density of states (Fig. 2).

For the separation of interface- and border traps we use two methods (Fig. 3): The change of saturation behavior observed in the constant high CP method and the often used CP frequency sweep [9]. In accordance with CP theory, signals of the constant high method must saturate as the number of chargeable traps in an oxide is finite. In practice, a fully saturated signal is sometimes difficult to obtain: The oxide will eventually break down when its breakdown voltage is exceeded by either the CP high or low level.

For the applied HCD stress we used the worst case scenario (Fig. 4), V_{D}=8 V and V_{G}=4 V. After the stress, the slower saturation of the constant high CP signal can be attributed to newly created border traps (Fig. 3 top). As the CP pulse base voltage increases, border traps move into the active energy window of charge pumping, due to an increase of the

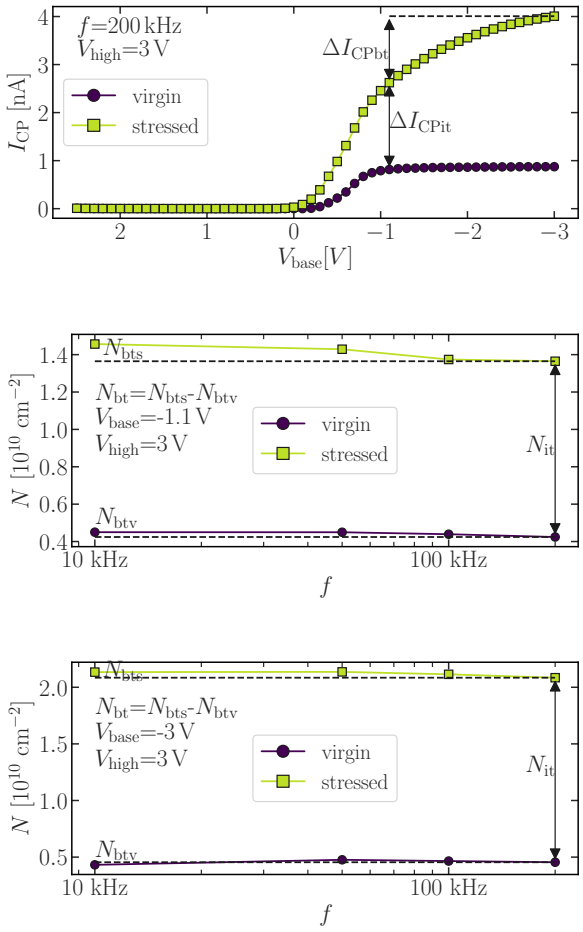

Fig. 3. Interface- and voltage dependent border traps are approximately separated at a base level of -1.1 V in constant high CP (top) and by the increase of the trap density in the CP frequency sweep (center and bottom) as the deviation from the 200 kHz signal.

oxide field [11]. The respective band diagrams are shown in Fig. 5. At -3 V (Fig. 5 bottom), significantly more traps can be accessed than at -1.1 V (Fig. 5 top). This leads to a faster increase of the CP current, which is proportional to the trap density [8], with higher CP low levels. We define the low level of -1.1 V as the approximate cutoff level for interface traps as this is the level where accumulation is definitely reached, i.e. the main increase of the constant high CP signal has taken place. As for the second method (Fig. 3 center and bottom), low frequencies allow for more time to also involve slower traps [11], thus allowing border traps to contribute to I_{CP}. We consider 200 kHz as the frequency at which approximately a negligible amount of border traps are observed. The lowest frequency in our setup, 10 kHz, includes border- and interface traps. For this frequency dependent CP method, more border traps are detected at a pulse base level of -1.1 V (Fig. 3 center) than at -3 V (Fig. 3 bottom). This means that some border traps are activated at all frequencies by a higher pulse base level but can be selectively activated by frequency dependent CP at lower pulse base levels. Therefore, to allow for the detection

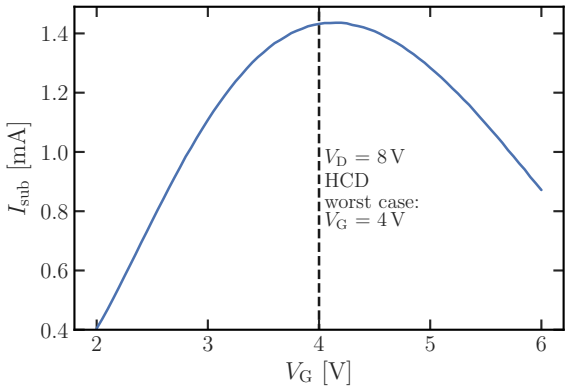

Fig. 4. Extraction of the worst-case condition for HCD: For a set drain voltage, the gate voltage with the highest substrate current I_{sub} is selected. High impact ionization rates, a symptom of HCD, are the source of I_{SUB} [10].

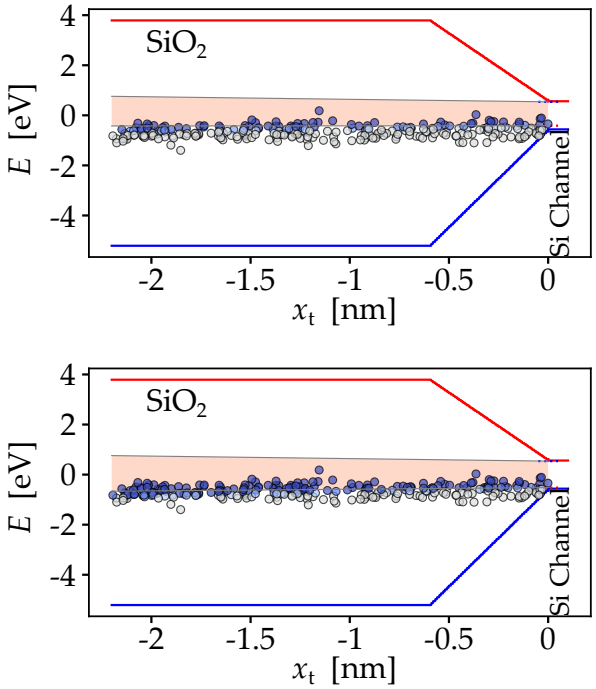

Fig. 5. Qualitative visualization of the active energy region of the MOS structure for different high levels of the CP pulse, as predicted by Comphy [12], [13]. Top: Trap levels that can be accessed with a CP pulse of a base- and high level of -1.1 V and 3V, respectively. Bottom: Increased energy region accessible at a CP base and high level of -3 V and 3 V, respectively.

of as many border traps as possible, -1.1 V is considered as a base level for further investigations with frequency dependent CP. The constant high and frequency sweep CP methods extend the CP theory, which was originally developed for interface traps, to consider the different nature of border traps. While the voltage dependency is investigated in the constant high method, the behavior due to additional time constants is captured in the frequency dependent CP. Due to the nature of the CP method, which is always based on the filling and

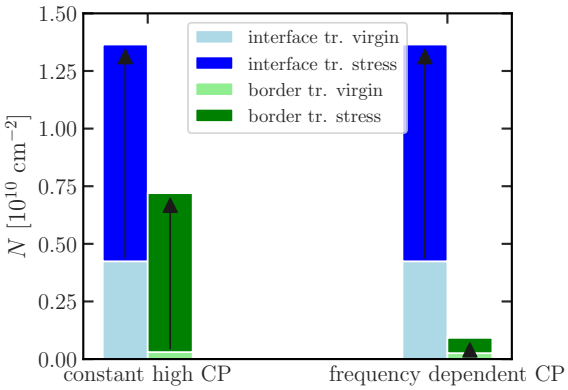

Fig. 6. Histogram showing the four trap densities as defined in Fig. 3, measured before and after a 20 ks stress at -60 °C. The base level is set to -1.1V, the high level to 3 V for the frequency dependent CP. Clearly, the constant high CP method up to -3 V can access a larger active energy region (cf. Fig. 5) and thus see more border traps than the frequency dependent CP method.

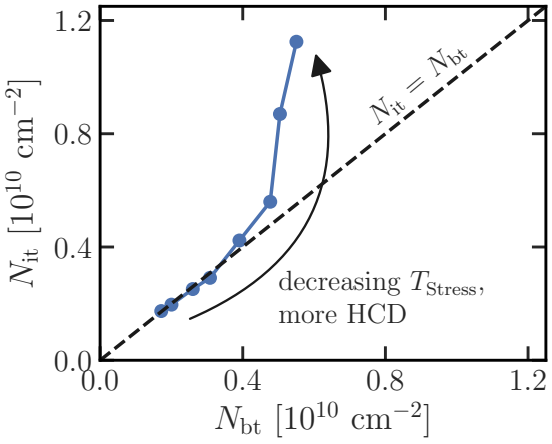

Fig. 7. Correlation of the voltage dependent border traps N_{bt} with the number of interface traps N_{it} in the constant high CP measurement. The dashed line represents $N_{it} = N_{bt}$.

emptying of traps states, all traps detected after stress must be newly generated defects and not preexisting traps which get charged during HCD. All presented trap measurement methods can be applied to structures and materials where regular CP is also possible.

III. Results and Discussion

A comparison of the extracted interface and border traps with the two aforementioned methods is shown in Fig. 6. For this technology, the voltage dependence of the border traps, measured with constant high CP, is significantly stronger than the frequency dependence of the frequency dependent CP. As the CP frequency sweep has always been used as a common method to detect border traps, interface traps have often been assumed to dominate HCD [14]. In order

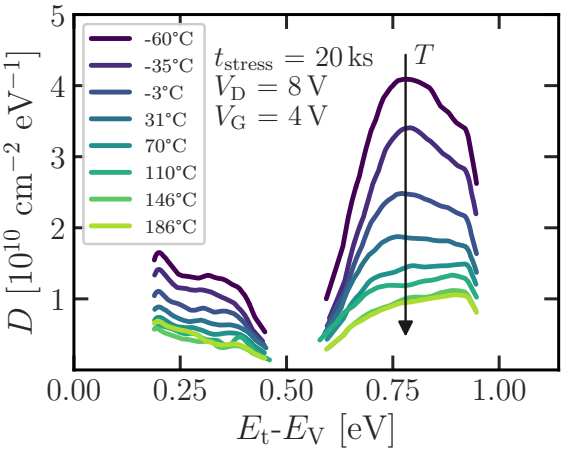

Fig. 8. Change of density of states after HCD at different stress temperatures measured by the spectroscopic CP method. With increasing stress temperature, the peak in the upper half of the band gap decreases. The data are smoothed with a Savitzky-Golay filter.

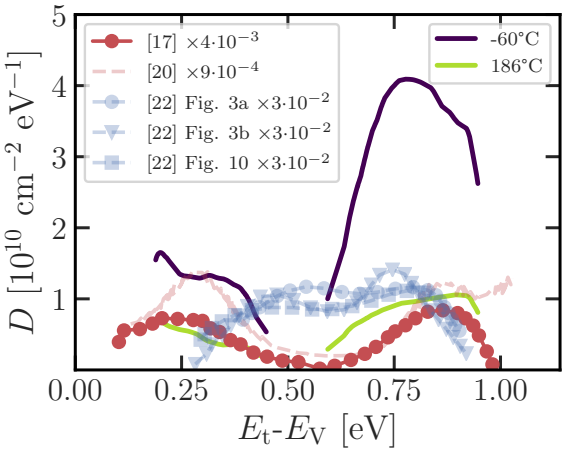

Fig. 10. The strongest and weakest stress depicted in Fig. 8 along with trap densities from literature (scaled with constant factors given in the legend). The red data refer to publications where P_b centers were investigated while the blue data was obtained after irradiation and HCD. Here, the literature data is qualitatively consistent with our data taken at 186 °C.

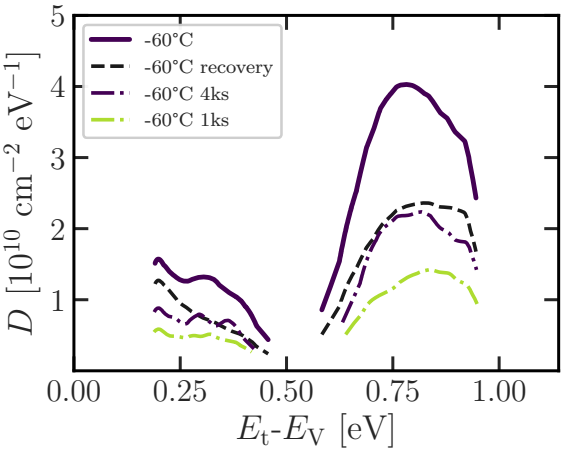

Fig. 9. Density of states as in Fig. 8. The dashed line represents the density of states after a stress for 20 ks at -60 °C and a subsequent recovery of 46.8 ks at 185 °C. For comparison, two other devices were stressed at -60 °C for 1 ks and 4 ks, respectively, and are shown with dash-dotted lines.

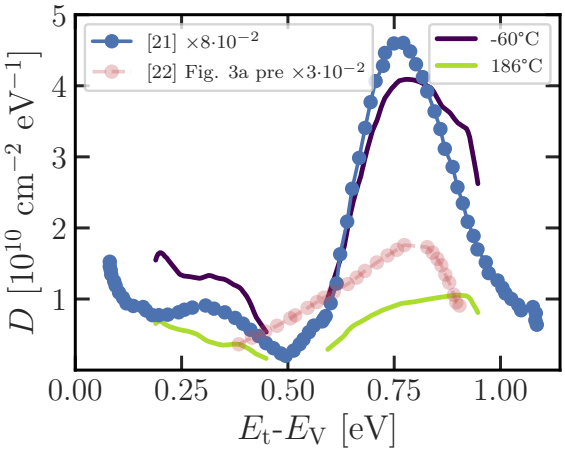

Fig. 11. The strongest and weakest stress depicted in Fig. 8 along with trap densities from literature (scaled with constant factors given in the legend). Here, all literature data show a markedly higher peak in the upper half of the bandgap, consistent with our -60 °C data, indicating the appearance of border traps.

to be able to properly asses border traps as well, we use constant high CP to investigate the relationship between the generation of border- and interface traps. For this investigation, the severity of HCD is adjusted with the stress temperature, which has long been known to impact HCD [2]: Lower temperatures increase HCD in these long-channel devices [15]. The results are shown in Fig. 7: For weak stresses, both trap types are generated at identical rates. At decreasing stress temperatures, the generation of interface traps is favored. A possible explanation for this observation is that the border traps are generated by the hydrogen released in the breaking of the Si-H bonds [16]. Eventually, this mechanism saturates as the released H can dimerize to H_2 before creating a border trap and predominantly interface states are generated. The combination of these two trap types is also observed in the density of states. Fig. 8 shows the hot-carrier induced defect spectra measured with the spectroscopic CP method described in [9]. The CP pulse base- and high level are -3 V and 3 V, respectively, such that both border- and interface traps are able to contribute to I_{CP}. In order to ensure that the variation of temperature creates the same density of states, thus the same defects, two shorter stress tests at the lowest temperature are conducted. They are shown in Fig. 9 and show that this assumption is

indeed valid. While interface traps created by depassivation of Si-H bonds, also called P_b centers, were shown to have two similar peaks in the lower and upper half of the band gap [17], we observe a deviation from this profile. The upper half of the band gap has a significantly higher trap density than the lower half. Therefore, the density of states must contain contributions from both interface- and border traps. Another hint at the involvement of both trap types is the recovery profile which was obtained after heating the sample stressed at -60 °C for 13 hours (Fig. 9). The basic shape of the recovered profile subtly deviates from the stress profiles in the lowest measurable segment of the band gap. This is due to different recovery mechanisms of interface- and border traps [4]. A possible candidate for such border traps is the hydroxyl E' center [18], [19].

Other authors [17], [20]–[22] have also found trap profiles with higher densities of states in the upper half of the band gap after different kinds of stress. Compared with the measurement of interface traps by Ragnarsson et al. [17], which clearly reveal the two humps typically associated with the P_b center, our trap profiles are depicted in Fig. 10. Uren et al. [20] obtained similar results in their measurement of the P_b center. It is noted that HCD observed by Devine et al. [21] fits very well to our harshest stress test (Fig. 11). Similarly, Ma [22] found matching profiles after HCD and irradiation.

IV. Conclusions

It is shown that the traps generated by HCD are not only interface but also border traps. The latter are separated from the former not only by frequency dependent CP but also by varying the high level of the CP signal. Both methods see different fractions of the newly created oxide traps and the active energy region probed by both methods has to be analyzed to understand their precise relation. Our data strongly suggest that at more severe stress conditions P_b centers seem to dominate while at less severe stress conditions, HCD creates the same amount of border traps and interface traps. Our stress temperature of -60 °C and stress time of 20 ks causes harsh conditions which have not been systematically investigated yet. In addition, border traps seem to recover faster than P_b centers, making the details of the experimental conditions important for the separation of these two contributions. Our results provide an explanation on the widely different energy distributions observed in previous studies and allow for improved physics-based modeling of technology reliability under HC stress. The distinction of border and interface traps is especially important for fast-switching applications as the border traps may only contribute to changes of the transistor parameters below certain frequencies.

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