Distribution of Step Heights of Electron and Hole Traps in SiON nMOS Transistors

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***Abstract*—The reliable operation of transistors is affected by electron and hole traps located inside the oxide and at the oxide/semiconductor interface. Each of the single defects can capture and emit a charge, alter the device electrostatics and thus affect the device behavior. As a consequence, a drift of the threshold voltage of the transistor can be measured. In nanoscale devices, the charge transition events of the defects can be observed as discrete steps in the device current. A significant benefit of investigating such scaled devices is, that we can study the impact of both electron and hole traps separately, which is not possible with their large-area counterparts. By probing scaled SiOX devices, the distribution of step heights caused by the single defects has been reported to follow a uni-modal exponential distribution. However, our results clearly reveal that the step heights of electron traps are bi-modal exponential distributed for positive BTI (PBTI) and negative BTI (NBTI) and for the hole trap/NBTI case, whereas a uni-modal distribution is observed for the hole trap/PBTI case. Of particular importance is the fact that if uni-modal distributions are considered for verification of the designs in circuit and device simulators the tail of the distributions, i.e. the large step heights, are fairly underestimated. This might give rise for an unexpected failure of the respective components. Furthermore, we demonstrate that for the underlying technology the charge sheet approximation (CSA) significantly underestimates the real impact of the defects too, which leads to pessimistic estimates for defect densities from experimental data.**

***Index Terms*—SiON MOS, Nanoscale devices, Single defects, Positive and negative bias temperature instability (PBTI, NBTI), Complementary cumulative distribution function (CCDF), Exponential step height distributions**

I. Introduction

As the geometry of MOS transistors scales down to a few tens of nanometers only, the number of defects per device becomes reduced. However, at the same time the impact of a single defect on the overall device behavior considerably increases [1]. This enables to study the charge trapping kinetics of electron and hole defects located in the oxide and at the oxide/interface, see Figure 1, by employing electrical measurements. This is possible, as the charging and discharging events of the defects lead to a discrete change of the threshold voltage, which can be monitored as the device current changes over time. This reliability issue is commonly referred to as Bias temperature instability and can be classified into positive BTI (PBTI) and negative BTI (NBTI), where the terms positive and negative refer to the sign of the applied gate bias during stress.

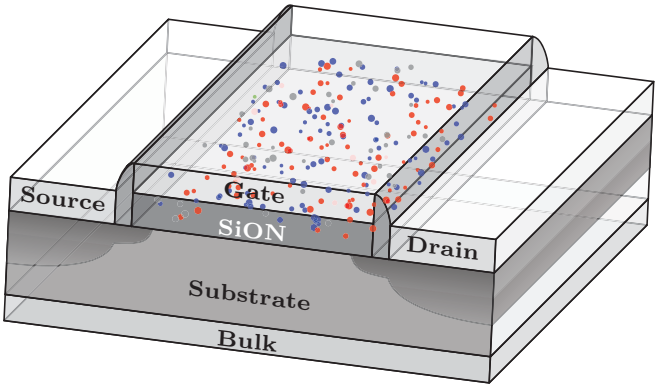

Figure 1. Schematic of a MOS transistor with indicated defects. Defects located within the device (oxide traps and interface states) affect the reliable operation of transistors. Electron traps (blue) and hole traps (red) can be examined when nanoscale devices are employed.

In large-area devices, studies of single defects cannot be performed, as their interaction with the carrier reservoirs, i.e. the channel and/or the gate, results in a continuous drift of the threshold voltage over time when MSM measurements are performed [2]. However, in nanoscale devices where only a handful of defects are present, charge transitions of individual defects can be observed as discrete steps in the corresponding measurement data enabling us to study the physical origin of charge trapping more closely.

Most of the single-defect investigations which have been performed so far, employ pMOS transistors [3]–[6] as for they are affected by a larger effective number of defects than nMOS device [7], which clearly simplifies their evaluation. In order to obtain a consistent explanation for the physics of charge trapping and the behavior of defects in general, studies on both types of MOS transistors have to be performed. Testing devices for both NBTI and PBTI can lead to further understanding of the position of defects and how it can be connected with their total impact.

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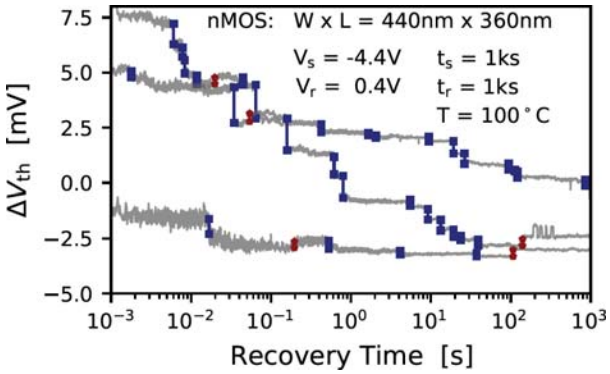

Figure 2. Selected recovery traces showing the drift of the threshold voltage after PBTI stress, measured using scaled SiON nMOS transistors. The recovery proceeds in discrete steps in these devices. Electron (blue) and hole (red) emission events can be observed as negative and positive discrete steps in the ΔV_{th} behavior, respectively.

II. Experimental

For our experiments, we employ the extended measure-stress-measure (eMSM) scheme. Before high stress voltages are applied to the gate of the devices to trigger charge transitions of the defects, an $I_D(V_G)$ sweep within a narrow gate bias range is typically performed. This sweep is used to obtain the initial threshold voltage of the device and use it to express the final traces in terms of equivalent shift of the threshold voltage ΔV_{th}, see Figure 2. The threshold voltage shift for the technology in our work is considered as the gate bias which has to be applied to achieve a drain-source current of $I_{\mathrm{DS}} = 500\,\mathrm{nA}$. Note, the initial bias sweep has to be performed within a very narrow gate bias range, in order to preserve the pristine state of the device. If the gate voltage sweeps over a too wide bias range, this can already cause considerable degradation of the device characteristics. After the stress phase a recovery bias at the value of the initial threshold voltage is applied, i.e $V_{\mathrm{Gr}} = V_{\mathrm{GS}}(I_{\mathrm{DS}} = 500\,\mathrm{nA})$, and the drain-source current is recorded. Afterwards the measurement data are analyzed and the discrete steps, i.e. the charge emission events of the defects are extracted from the data set [8]. At the recovery phase the defects that got charged during stress phase emit their charges and the drift of threshold voltage decreases. As can be seen from the data, the majority of the discrete charge emission events are due to electron trapping (blue), but there is also a number of hole trapping events visible (red). In order to investigate the impact of both kinds of traps at different biases we have a closer look at NBTI and PBTI employing SiON nMOS transistors with different geometries. The same stress and recovery times have been used for all eMSM sequences, however, the stress/recovery biases have been adjusted to account for the different threshold voltages of the different device kinds, see Table I.

Table I
Common experimental parameters, i.e. stress/recovery time and device temperature, and device-specific parameters which have been used in our study.

Common Parameters:

t_s	1ks
t_r	1ks
T	100°C

Device-Specific Parameters:

W(nm)	L(nm)	V_s(V)	V_r(V)
400	180	4.4	0.4
440	360	4.4	0.4
1000	700	7.56	0.35

III. Distribution of Step Heights

To describe the overall contribution of electron and hole traps in nanoscale devices a statistical description is required because of the variability of nanoscaled devices. Therefore, the complementary cumulative distribution function (CCDF) of step heights for each device kind is created and analyzed [2], [9], [10]. The CCDFs are created by the extracted step heights from recovery traces of the stress-measure scheme. At the aforementioned works distributions extracted from experimental data have been documented to have exponential characteristics. The respective probability distribution function (PDF) for a single-mode has been described by Kaczer et al. [2] by the following formula

$$f(\Delta V_{\mathrm{th}}) = \frac{1}{\eta}\exp\left(-\frac{\Delta V_{\mathrm{th}}}{\eta}\right), \tag{1}$$

where η is the mean threshold voltage shift caused by a single charge transition event of a single defect. From the PDF the corresponding CDF can be calculated as

$$F(\Delta V_{\mathrm{th}}) = \int f(\Delta V_{\mathrm{th}})\mathrm{d}\Delta V_{\mathrm{th}} = 1 - \exp\left(-\frac{\Delta V_{\mathrm{th}}}{\eta}\right) \tag{2}$$

By normalizing the CCDF to the number of devices, the following relation can be obtained

$$\frac{1-\mathrm{CDF}}{\#\mathrm{devices}} = \sum_i N_{\mathrm{T}i}\exp\left(-\frac{\Delta V_{\mathrm{th}}}{\eta_i}\right), \tag{3}$$

where $N_{\mathrm{T}i}$ is the number of defects per device for each existing exponential branch i, ΔV_{th} is the threshold voltage shift and η_i is the average threshold shift induced by a single carrier. The expression above accounts for multi-modal behavior of the experimental complementary CDFs [11], [12].

IV. Positive BTI

For the PBTI case the band diagram and the active energy region for charge trapping can be seen at Figure 3. Because of the applied positive stress voltages the valence and conduction bands bend towards lower energies. A necessary condition for a defect to contribute to ΔV_{th} is that the defect must be energetically located in the so called active energy region (AER) for charge trapping. For the PBTI case defects above the Fermi level of the channel carrier reservoir and below of

the poly-gate can become charged and then discharge under the initial conditions , provided that the bias is applied for a longer time larger than the charge capture and emission time of the respective defect. Thus, the bias used for the MSM measurements determines the energetic area spanned by the AER for charge exchange between the channel and the electron traps, but also between the poly-gate and the hole traps. The AERs where the aforementioned requirements can be fulfilled are marked as the blue and red areas at Figure 3. The blue area is for charge transitions between the defects and the channel while the red one for charge transitions between the defects and the gate.

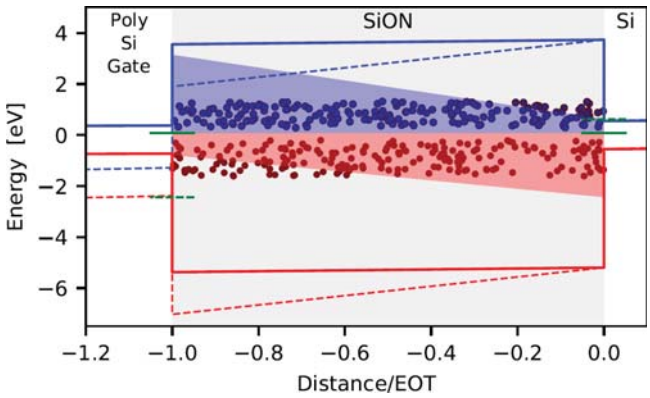

Figure 3. Band diagram of nMOS devices shown for the positive bias stress case. Electron (blue) and hole traps (red) are shown, with the respective active energy regions (AERs) for charge trapping. The AER for charge transitions between the defects and the channel is marked in blue and for charge transitions between the defects and the gate in red. These areas define the energetic regions inside of defects inside the oxide which can change their charge state during the experiments, and thus can contribute to the measurement signal. Note that the height of the AERs strongly change with the applied gate bias.

The collected CCDFs of three sets of devices with different geometries are depicted in Figure 4. As can be seen, the BTI behavior is dominated by electron traps, but also a small number of hole traps is found to be active. Note that, 85 defects (8%) are identified as hole traps among a total of 1065 traps for the PBTI case. Charge trapping of electrons has been recently assigned to defect/channel interactions, while hole trapping is due to defect/gate interactions [10]. A significant benefit of studying single-defects is that the contributions of the electron traps and hole traps can be separated, while in large-area devices only the average response of a multitude of defects can be measured.

The absolute contribution of a carrier type, for example electrons, to the total threshold voltage shift ΔV_{th}, is given by

$$r_{\mathrm{h}} = \frac{\sum_{i=1}^{N_{\mathrm{e}}} |d_{\mathrm{e}}|}{\sum_{i=1}^{N_{\mathrm{e}}} |d_{\mathrm{e}}| + \sum_{i=1}^{N_{\mathrm{h}}} |d_{\mathrm{h}}|}, \tag{4}$$

where N_e,N_h are the number of electron and hole defects respectively and $|d_e|$,$|d_h|$ the step heights of the single hole/electron emission events. It can be observed that hole trapping decreases the total $\Delta V\mathrm{th}$ by about 5.6% for the bias and temperature conditions used for the PBTI case

The CCDFs after PBTI stress clearly reveal a bi-modal exponential behavior for electron traps and a uni-modal exponential characteristics for hole traps, as can be seen in Figure 4. but also for the absolute values of all traps, see Figure 5. The behavior observed at Figure 5 is expected as the electrons traps contribute the most to this distribution.

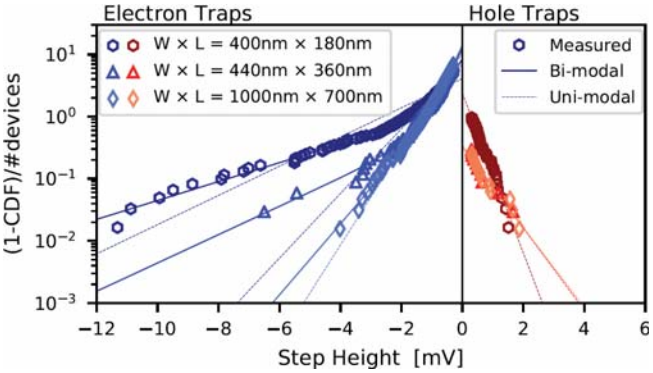

Figure 4. Distribution of step heights measured from SiON nMOS transistors after PBTI stress for three device sets with different geometries. The majority are electron traps (left) but a certain number of hole traps (right) can be observed too. The behavior of electron traps follows a bi-modal exponential distribution, while for the holes a uni-modal exponential behavior can be observed.

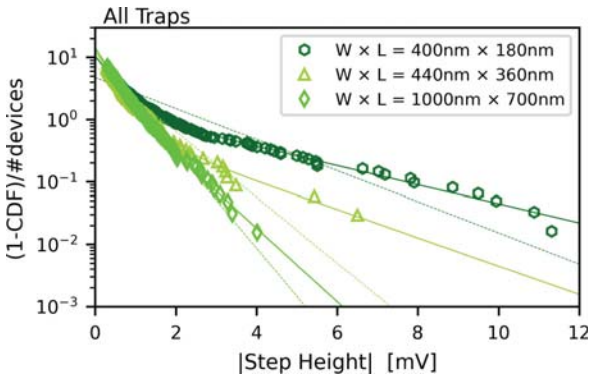

Figure 5. Distribution of the absolute value of all steps from Figure 4. The distributions show a bi-modal exponential behavior.

V. Negative BTI

For one device geometry we also evaluate the impact of negative bias stress conditions on the distribution of the active traps. The negative applied voltage, contrary to the PBTI case, creates a band bending of conduction and valence band towards higher energies. According to the respective band diagram from Figure 6 more holes traps and less electron traps are expected to contribute to the threshold voltage

shift compared to the PBTI case. This is clearly confirmed by the extracted CCDFs for both electron and hole traps from Figure 7, which is an evidence for the accuracy of our investigations. Furthermore, the CCDF for each kind of traps exhibits two branches, and considering a uni-modal model would lead to an underestimation of the tail of the distributions. A significant difference to the PBTI case is that here bi-modal exponential distributions can be seen for both kinds of traps.

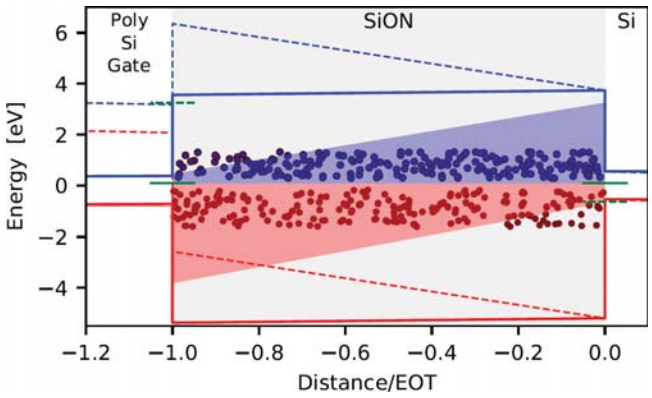

Figure 6. The band diagram for the negative stress gate bias case is shown here. In contrast to the PBTI case, more hole traps can contribute to total ΔV_{th} now. The AERs for charge transitions between the defects and the channel and for charge transitions between the defects and the gate are marked in blue and red color, respectively.

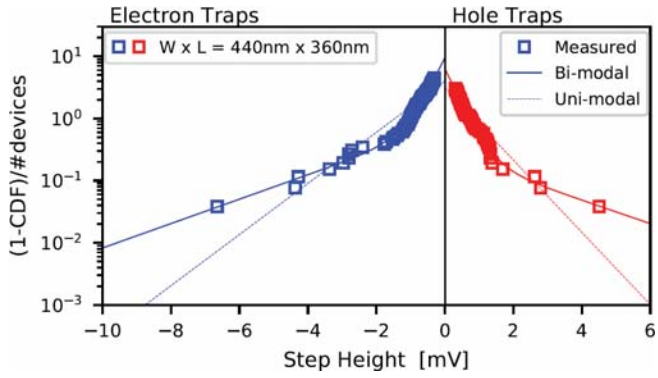

Figure 7. Distribution of step heights of defects extracted after NBTI stress. Both distributions follow bi-modal exponential behavior.

VI. Results

Bi-modal exponential distributions of the CCDFs of single-defects have been observed for devices with high-κ gate stacks [13]. In this work, each branch of the distribution has been assigned to charge transfer interactions of defects of one of the insulating layers with the channel. Recently, this kind of distribution has been reported for devices with SiON insulators too [12]. The overall bi-modal CCDF has been separated into two almost uni-modal ones, where one branch has been

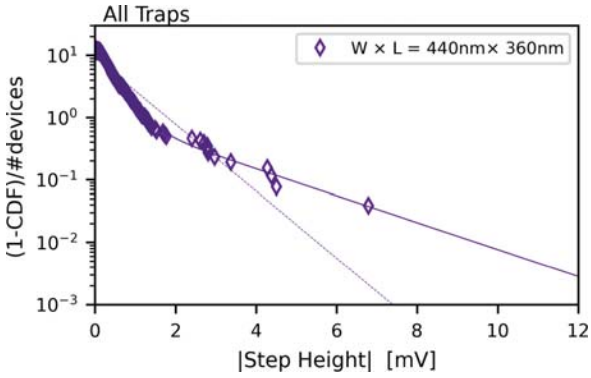

Figure 8. The step height distribution of the absolute values of all traps contributing to NBTI. The distribution consists of two exponential modes.

assigned to electron trap/channel interactions and the second one to hole trap/poly-gate interactions [10]. According to our latest results bi-modal CCDFs are obtained for each kind of traps. A detailed overview about the number of traps and their contribution is given in Table II.

For PBTI the behavior of nMOS devices is clearly dominated by electron traps ($\sim 92\,\%$ of all traps), whereas for NBTI hole trapping becomes increasingly important, i.e. ratio between electron/hole traps is $\sim 60\,\%$ / $40\,\%$. Note, as the hole traps are more likely close to the poly-gate [10], their average step height is small compared to the electron traps, and thus their measurement requires optimized low-noise tools [12]. Otherwise charge trapping at hole traps might completely vanish in the measurement noise. The extracted parameters, i.e. average step height and number of traps per device, considering uni-modal CCDFs and uni-modal are shown in Figure 9 and in Figure 10, respectively, together with charge sheet approximation (CSA) .

To estimate the impact of a single defect on the device behavior the CSA is often used in device simulators. This model assumes that the oxide charge is spread over the insulator and can be described by [14]

$$\Delta V_{\mathrm{th}} = -\frac{q}{\epsilon_0 \epsilon_{\mathrm{r}} W L} t_{\mathrm{ox}} \left(1 - \frac{x_{\mathrm{T}}}{t_{\mathrm{ox}}}\right), \tag{5}$$

where q is the elementary charge, ϵ_0 and ϵ_{r} the dielectric constants, t_{ox} the oxide thickness and x_{T} the position of the trap with respect to Si/SiON interface. By applying the CSA the trap density can be estimated from a given ΔV_{th}. In our work, we compare the extracted values of threshold voltage shift from CCDFs by considering the maximum impact given by the CSA which is $x_{\mathrm{T}} = 0$, i.e directly at the interface. It is clearly visible that for both distributions the CSA significantly underestimates the extracted average impact of the defects η. As a consequence too pessimistic results for defect densities will be extracted from ΔV_{th}. The results shown here are of particular importance to enhance charge trapping models and the accuracy of the simulations.

Table II

Extracted number of defects and their impact on threshold voltage shift for different device geometries. As can be seen, the total ΔV_{th} results from electron trapping, but also a significant amount of hole traps contribute to the threshold voltage shift. Thus, modeling of both contributions is essential for accurate modelling of BTI. #d is the number of devices, $\mathrm{N_{e,h,tot}}$ is the total number of electron/hole traps, $\eta^{\mathrm{e,h}}$ gives the average impact of electron/hole traps on the ΔV_{th}. The values for the total threshold voltage shift ΔV_{th} and the threshold shift per charge η are given in mV. The last line of the table refers to the NBTI case.

W(nm)	L(nm)	#d	$\mathrm{N^h_{tot}}$	$\mathrm{N^h/_{\#d}}$	$\Delta V^{\mathrm{h}}_{\mathrm{th}}$	η^{h}	$\mathrm{N^e_{tot}}$	$\mathrm{N^e/_{\#d}}$	$\Delta V^{\mathrm{e}}_{\mathrm{th}}$	η^{e}	$\mathrm{N_{tot}}$	$\mathrm{N_{tot}/_{\#d}}$	$\Delta V^{\mathrm{tot}}_{\mathrm{th}}$	η
400	180	61	59	0.97	36.6	0.62	320	5.25	439.2	1.37	379	6.2	402.4	1.06
440	360	34	10	0.3	6.5	0.65	231	6.8	195.2	0.845	241	7.1	188.7	0.78
1000	700	64	16	0.25	11.5	0.72	429	6.7	345.6	0.81	445	6.95	334.1	0.75
440(N)	360(N)	26	79	3.04	58.44	0.74	118	4.54	105.62	0.895	197	7.58	47.18	0.24

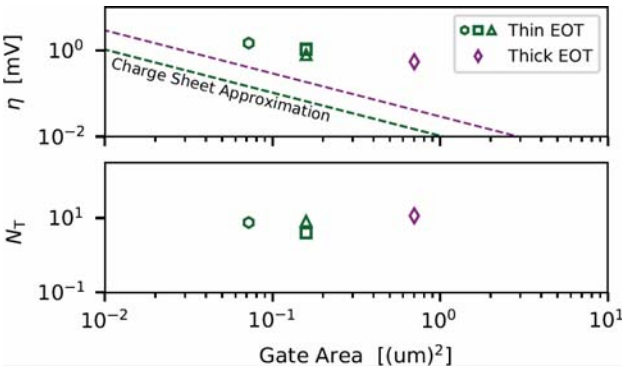

Figure 9. Extracted impact of a single defect on the ΔV_{th} (η) and number of traps per device ($\mathrm{N_T}$) considering uni-modal exponential distribution. Clearly visible is the underestimation of the charge sheet approximation of the defects impact, on the device behavior. The maximum impact of CSA is considered by considering the traps directly at the interface.

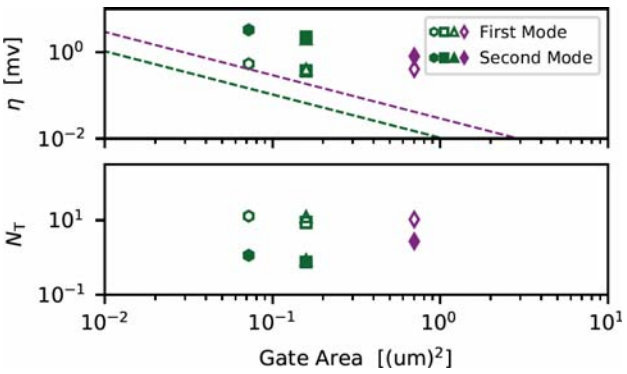

Figure 10. The extracted values for the two modes of the bi-modal exponential distribution are shown. As can be seen from Fig. 4 and Fig 7, the distribution follows more a bi-modal exponential behavior than a uni-modal one. Again, the charge sheet approximation significantly underestimates the impact of the defects, which lead to a too pessimistic estimation for defect density from ΔV_{th}.

VII. Conclusions

The accurate description of the impact of single defects on the device behavior is important for accurate device and reliability simulations. In our study we evaluate the impact of single defects on the behavior of nMOS SiON transistors, by analyzing the distribution of their step heights employing devices with different geometry. We clearly demonstrate that the distributions of electron and hole traps can follow a bi-modal behavior, contrary to what has been reported so far in literature. This can be explained by two different types of defect interactions, i.e. gate/trap and channel/trap charge transitions. Considering the distributions we further show that the typically used CSA significantly underestimates the effective impact of defects on the device behavior. A correct description of the defect impact seems vital for accurate device simulations especially for modelling devices with geometries of tens of nanometers.

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