TWO-DIMENSIONAL MATERIALS

Native high-*k* oxides for 2D transistors

The two-dimensional semiconductor Bi_2O_2Se can be oxidized to create an atomically thin layer of Bi_2SeO_5 that can be used as the insulator in scaled field-effect transistors.

Yury Yu. Illarionov, Theresia Knobloch and Tibor Grasser

For the past 60 years, technological progress in electronics has been driven by the exponential growth of the transistor count in integrated circuits. As a result, modern electronic chips contain billions of field-effect transistors (FETs) and state-of-the-art silicon FETs are built from structures as thin as seven nanometres, which corresponds to 13 atomic layers[1]. However, three-dimensional materials like silicon show a dramatic drop in mobility upon further reduction in their thickness. In addition, the impact of the amorphous and rough channel/oxide interface (which is also present in advanced high-*k* technologies such as hafnium dioxide, HfO_2; *k*, dielectric constant) becomes increasingly detrimental. Thus, further scaling of modern electronic devices by relying solely on standard silicon technologies is slowly coming to a halt[2].

One of the most promising solutions to continue device scaling is to use FETs with atomically thin two-dimensional (2D) channels[3,4], which intrinsically offer channel thicknesses in the sub-nanometre regime. However, 2D technologies lack competitive insulators that work as effectively as silicon dioxide (SiO_2) does with silicon. Ideally, such insulators must be scalable down to below a single nanometre in equivalent oxide thickness (EOT; the thickness of SiO_2 which would result in the same capacitance as a certain thickness of an alternative insulator) with a high enough quality to maintain low leakage currents. In addition, the insulators should have a well-defined interface with the channel, a low number of insulator defects, and a high dielectric stability. Writing in *Nature Electronics*, Hailin Peng and colleagues now show that the high-mobility 2D semiconductor Bi_2O_2Se can be conformally oxidized to its atomically thin native oxide, bismuth selenite (Bi_2SeO_5), which can subsequently serve as a gate insulator in FETs[5].

Currently, hexagonal boron nitride (hBN) is widely considered the most promising insulator for 2D electronics because it is crystalline and provides a clean van der Waals interface[6]. However, it is unlikely that hBN can meet the low leakage requirements

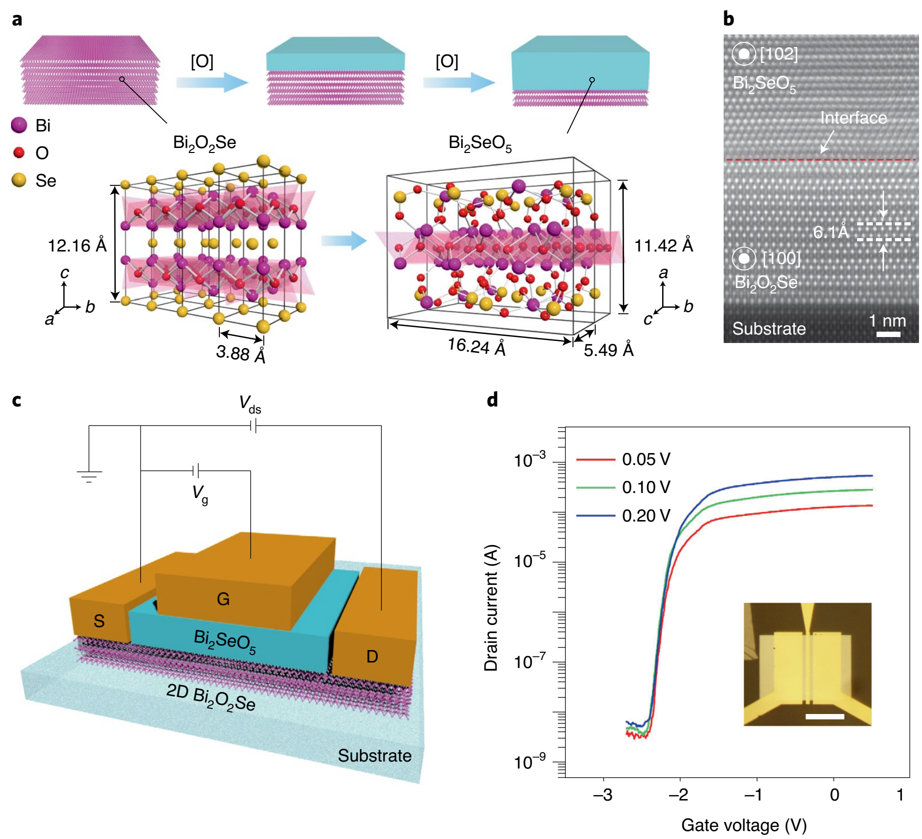

Fig. 1 | Development of FETs with Bi_2O_2Se channels and native Bi_2SeO_5 insulators. **a**, Step-by-step oxidation of multilayer Bi_2O_2Se towards Bi_2SeO_5 and the crystal structure of the two materials. **b**, Cross-sectional scanning transmission electron microscopy image confirming the atomically sharp interface. **c**, Schematic of the top-gated devices fabricated with a native gate oxide. **d**, Gate transfer characteristics of the devices with a 4.6-nm-thick Bi_2SeO_5 layer (EOT below 1 nm). Figure reproduced with permission from ref. [5], Springer Nature Ltd.

for sub-1-nm EOT. In the last twelve months or so there has though been a number of promising reports on scalable insulators suitable for 2D FETs. First, there was work on using ultrathin crystalline calcium fluoride (CaF_2) as a gate dielectric in MoS_2 FETs[7]. However, the devices studied were back-gated and the integration of CaF_2 as a top gate insulator is a requirement for circuit integration. There was then work on the use of molecular crystal monolayers to passivate the interface between ultrathin HfO_2 and MoS_2 (ref. [8]). Though top-gated devices with ultrathin insulators were demonstrated, it remains to be seen if the small thickness of such passivation layers formed by discrete molecules will suffice to effectively block charge trapping by border oxide traps[9] in the amorphous HfO_2. Now, this latest work provides an intriguing approach to create top-gated FETs suitable for circuit integration by oxidation of the 2D channel, thereby demonstrating the sub-1-nm EOT potential of a native oxide of a 2D material for the first time.

The researchers — who are based at Peking University, the Weizmann Institute of Science, the University of Texas at Austin, Tsinghua University and Nankai University — used layer-by-layer thermal oxidation of Bi_2O_2Se to obtain atomically thin dielectric layers of its native oxide Bi_2SeO_5 (Fig. 1a). This oxide has a high dielectric constant of about 21 and forms an atomically sharp interface to the layered semiconductor (Fig. 1b). They show that the Bi_2O_2Se/Bi_2SeO_5 system can support selective etching and scalable patterning. This allows them to fabricate top-gated FETs (Fig. 1c) that exhibit good performance, with a subthreshold swing below 75 mV dec^{-1} and a mobility of 250 $cm^2V^{-1}s^{-1}$, even for Bi_2SeO_5 insulators with less than 1 nm EOT (Fig.1d). At the same time, due to the crystalline nature of Bi_2SeO_5, a low density of oxide traps can be expected, which should lead to high mobilities and a small hysteresis. Furthermore, and despite the early stage of the research, the researchers were able to use their FETs to fabricate functional logic inverter circuits with a voltage gain as high as 150.

Hailin Peng and colleagues have created functional 2D FETs and circuits using the native oxide of the 2D channel material, and thus their work is a milestone in the development of 2D electronics. It is worth noting, however, that these prototype logic inverters have been fabricated using devices with 20-nm-thick Bi_2SeO_5. The demonstration of FETs with sub-1-nm EOT insulators is limited to a single device and the researchers suggest that the relatively small on/off current ratio of about 10^5 (Fig. 1d) is due to the large leakage current. Indeed, Bi_2SeO_5 has a narrow bandgap of 3.9 eV, which is likely to limit the future scaling potential of this particular material system. Nevertheless, the successful layer-by-layer oxidation of Bi_2O_2Se provides an exciting blueprint for the exploration of using native insulators in 2D electronics, and could lead to devices that have significant commercial potential. ❐

Yury Yu. Illarionov[1,2] ✉, Theresia Knobloch[1] and Tibor Grasser[1] ✉
[1]*Institute for Microelectronics, TU Wien, Vienna, Austria.* [2]*Ioffe Physical-Technical Institute, St Petersburg, Russia.*
✉*e-mail: illarionov@iue.tuwien.ac.at; grasser@iue.tuwien.ac.at*

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