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SHORT PAPER

A 2.4-GS/s Power-Efficient, High-Resolution Reconfigurable Dynamic Comparator for ADC Architecture

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Abstract

Reconfigurability is an important capability that provides flexibility in computing architecture and low-power technique. It is challenging in digital-in-concept for designing smart analog circuits operated on low power. This work presents a low-power, low-noise, and high-speed multistage feed-forward reconfigurable comparator for medium-to-high-speed analog-to-digital converter. A power-efficient reconfigurable comparator design at 180 nm is presented with a new power reduction and offset compensation technique. The proposed dynamic latch-based 2-stage comparator gives an 83.2% power saving compared with a 3-stage comparator. The reduced number of active stages in comparator lowers the load capacitance to the post-amplifier and the power consumption. The 2-stage comparator gives a high slew rate, low power consumption, and better result at a Nyquist rate of 2.4 GS/s as compared with the previous state of the art. We have also proposed the reconfigurable multistage comparator, which gives the features of both 2-/3-stage comparators. We have performed the post-layout simulation to validate the design for process variation and mismatch with proposed circuit and compared with state of the art. Further, the voltage gain is 100 dB with power supply 1.8 V while consuming 523.4 μW and 86.15 μW for 3-stage and 2-stage comparator, respectively.

Keywords Analog-to-digital converter · Modified dynamic latch · Multistage comparator · Runtime configurability · Process and mismatch

1 Introduction

In the on-chip Internet of Things (IoT) applications, demanding performance is required to push the limit for a solution over the power consumption in the analog front-end circuits. However, it needs system consideration like flexibility in modulation and analog-based solutions in architecture. The power consumption is one of the significant areas of research for the digital as well as analog circuit designs.

Extended author information available on the last page of the article

The settlement over the limitations is application-based reconfigurability in the circuit architecture. As the number of active transistors in a chip increases, the power dissipation also goes on hikes rapidly [1]. An inclusive architecture is required at all levels of the system design aspect, means architectures with the logic styles and the underlying technology. The application like ADCs and especially flash-type ADC is an ideal choice in ADCs for high-speed application (GS/s). Moreover, it consumes more power compared to the other ADC architectures. Since flash-type ADC is operating in parallel, the number of comparators increases exponentially with higher resolution, which leads to both significant amounts of power consumption and large area. Unfortunately, modern ADCs have the trade-off among power, speed, and accuracy with low complexity [5]. In very high-sampling-speed superconductor ADCs, it is utilizing periodic comparators that reduce hardware complexity and used for highly parallel large-bandwidth applications [7,12]. The frequency-dependent distortions resulting from impedance mismatches can be minimized over a wide bandwidth by clock signal distribution network which has been optimized with delay element [7]. The most significant bit (MSBs) in comparator ladder of the flash ADC is least sensitive to the input signal, and hence, because of jitter and threshold misplacement mostly has the threshold error. If we double the resolution of flash-type ADC, the analog least significant bit (LSB) value became halved and comparator comparison range will also half [12]. The design perspective, as the gain increases, will have the difficulties driving a large capacitive load [6]. The threshold mismatch $\Delta V_{\text{th}} = \text{AV}_{\text{th}}/\sqrt{\text{WL}}$ shows the relation with the design parameter, where AV_{th} is a constant and WL denotes the channel area. The observation from the equation states that WL must quadruple as double the resolution, which increases the leakage problem. The decrease in the supply voltage decreases the leakage and energy consumption at the cost of conversion speed. The comparator with offset cancelation technique is used in [2,11] which requires more active transistors.

A new remold approach to dealing with gain and offset, multiple gain stages may be used to relax the bandwidth requirements and does not require a power-down mechanism [8]. However, these techniques increase the circuit complexity in overall comparator design. The switch is used in between differential latch and preamplifier stage to reduce the kickback noise along with the offset cancelation technique [10]. The operation of the comparator has two phases, as a reset phase and comparison phase. Moreover, static power dissipation is minimized by isolating all responsible components other than bias current at the input stage, whereas sub-threshold biased transimpedance stage is used as a current sensing load [4]. The new design double-tail comparator is also proposed to reduce dynamic/static power and leakage current [3]. The conventional comparator includes a preamplifier, dynamic latch, and post-amplifier stages. From the observation, cascade stages in comparator can be bypassed with reconfigurable techniques. The differential comparator for low-power application is designed using a reconfigurable technique which bypasses power-hungry active stages in the comparator. However, the static power consumption by the remaining amplifier stages is still not desirable for given recent low power demand.

The conversion of continuous to discrete time is realized within the comparator. Apart from technological advancement, developing new circuit architecture which avoids stacking of too many transistors between the supply rails is preferable for low-

voltage, high-speed operation, especially if they do not increase the circuit complexity. However, investigation shows that the comparator consumes maximum area and power. In this paper, we have proposed efficient reconfigurable comparator. Many transistors' design style is proposed based on the application and properties. The TIQ technique uses two cascade inverters for the threshold comparison. The first stage is the inverter, which generates switching voltage internally, and the second stage acts as a gain booster [9,16]. The circuit with a basic model derives design conditions for improving the speed and resolution in clockwise CMOS transimpedance comparators [14]. The analysis gives two different architectures for the basic comparator, which depends on whether the input sensing node is capacitive or resistive. The multistage comparator is based on the cascade structure in a pipelined arrangement of modified input offset storage amplifier and the output offset storage amplifier. The topology maintains a good input common-mode range and improves speed due to reducing capacitive load. However, this technique increases the overall power consumption [15].

The rest of the paper is organized as follows: basic architecture of the proposed reconfigurable comparator is explained with circuit implementation of the prototype in Sect. 2. Section 3 shows the simulation results and discussion followed by a conclusion in Sect. 4.

2 Proposed Reconfigurable Comparator Circuit Implementation

This section describes the different block levels of the low-power reconfigurable comparator. The principle drawback with flash-type ADC is that the resolution increases and there is exponential growth in overall cost. The cost is interms of input capacitance, comparator kickback noise, power consumption, chip area, and complexity in routing the signal. Considering these limitations, reconfigurable multistage comparator proposed having stages, namely (1) preamplifier with bypass switch circuitry, (2) modified dynamic latch, and (3) post-amplifier, as shown in Fig. 1. The trend for 4-bit and above resolution, flash-type ADC needs better offset cancelation with a low-noise-sensitive comparator and high bandwidth. The 3-dB bandwidth for the amplifier is described as:

$$f_{3\,\mathrm{dB}} = \frac{1}{2\pi \times R_{\mathrm{Load}} \times C_{\mathrm{Load}}} \tag{1}$$

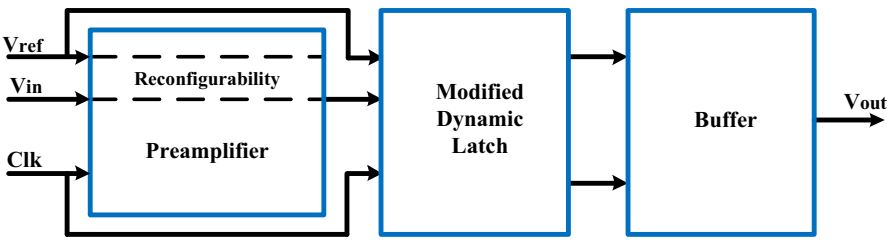

Fig. 1 Block-level architecture of runtime reconfigurable 2-/3-stage differential comparator. The same V_{ref} pin is applied to both stages of the proposed comparator, whereas V_{in} goes out through analog switch

where R_{Load} and C_{Load} are the resistive and capacitive load for the amplifier, respectively. Moreover, Eq. (1) states that, with increasing amplifier bandwidth, the value of R_{Load} must be reduced. The preamplifier is often used to relax the effects of comparator input offset voltage for better matching and metastability, but it increases the total power consumption. Besides, the parasitic input capacitance by the preamplifier remains a bottleneck in high-speed and low-power application.

Addressing the above problems, application-specific user can bypass the preamplifier stage. To do that, two important design aspects are considered. First, the proposed dynamic latch and another are application-dependent reconfigurability using analog switch [13]. The use of reconfigurable stages depends on V_{th} of $M6$ and $M7$. If the input is less than 0.5 V, the probability of noise and error is more; in that case, preamplifier used the reconfigurable comparator for increasing the gain and offset cancelation, while for higher input range preamplifier can be bypassed and only used the two stages of the comparator. The modified dynamic latch is designed in such a way that preamplification and decision both are done by the proposed modified circuit. The following section gives the detailed description of the reconfigurable comparator.

2.1 Preamplifier with Reconfigurable Logic Circuit Implementation

The preamplifier circuit with the controlled analog switch is shown in Fig. 2a which achieved the sampling rate of 2.4 GS/s. Depending on the input analog signal and user applications, it contains two steps. If input signal $V_{\text{in}} \leq (\mid V_{\text{th}} \mid)_{M_6,M_7}$, then preamplifier stage is active in differential amplifier. In the transistors with linear tunable transconductance, $M6$ and $M7$ sizes are identical, and V_{G1} and V_{G2} are at fixed switching voltage. However, the channel length will decide the switching potential. The MOS-level architecture of switch to bypass input signal is shown in Fig. 2b. Moreover, the input is passed through both NMOS (MS1) and PMOS (MS2) to the output terminal and its switching control by gate terminals.

The analog switch is used to bypass the input signal, and the concept behind this advancement is to save the power consumption by the preamplifier stage. If an input signal is higher than V_{th} of $M6$ and $M7$, mask the preamplifier stage and bypass the input analog signal. Pass transistor logic-based switch is used to get the perfect output without logic degradation. Pass transistor logic involves NMOS and PMOS transistors to transfer the charge from one node of a circuit to the anther node under the control of MOS gate voltage. An NMOS transistor is a perfect switch when passing a zero, i.e., it passes a strong '0.' However, the PMOS transistor is a perfect switch when passing one, i.e., it passes strong '1.' The circuit with pair connection gives the perfect output as input without logic degradation. In this case, input (V_{in}) and control (Ctr) are at the same logic. We have set the threshold voltage of Inv1 at which switch will on and bypass the preamplifier stage, i.e., input pass to the proposed dynamic latch. With this novel technique, we can save the power which is mostly consumed in the preamplifier stage. We have simulated switch circuit at different process corners for worst delay and power. The worst-case delay is calculated for slow–slow (SS) process corner and worse-case power consumption at fast–fast (FF) process corner. However, the switch output response and delay at worst process corner (mismatch) are shown in Fig. 2c.

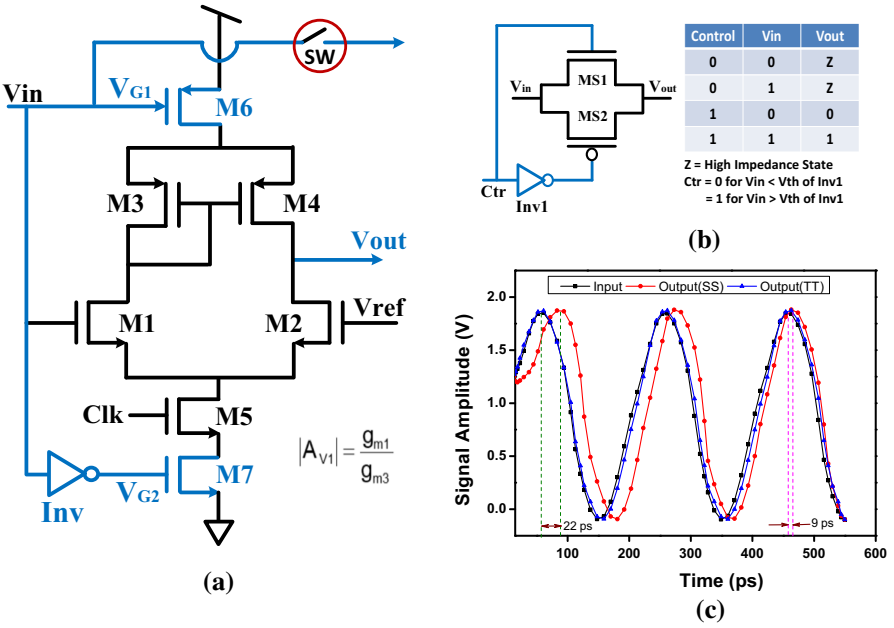

Fig. 2 **a** Preamplifier with controlled analog switch (SW) for threshold detection and bypassing the analog signal, **b** MOS architecture of switch with control pin, **c** analog switch output response at different process corners

The maximum delay generated by the MOS-based switch at the output for the first pick and the third pick at worse corner (SS) is 22 ps and 9 ps, respectively. The settling time is given by $T_s = 4/\zeta\omega_n$, where ζ is damping ratio and natural frequency ω_n. Thus, settling time within 2% for the underdamped condition with $\zeta = 1$, the preamplifier is achieved at 550 ps. This observation can ensure the zero switching delay up to 2.4 GS/s sampling frequency at the worse process corner.

2.2 Implementation of Proposed Dynamic Latch and Post-amplifier (Buffer)

The behavior of a first-order system having a single dominant pole shows stable phase margin without complicated frequency compensation. Self-bias circuit automatically generates bias voltages to sustain performance over a wide range of supply voltage. The circuit is designed and tested with post-layout simulation for the 1.8 V ± 10% supply. The 3-stage comparator consists of preamplifier followed by the proposed dynamic latch and post-amplifier. The preamplifier is followed by a proposed dynamic latch which is having good offset cancelation and driving strength. The proposed circuit is implemented, which can differentiate the signals without preamplifier, and that was the motivation behind the reconfigurability. To maintain the stable DC operating point, the transconductance of the input pair needs to increase with equal proportionality which implies raising current and power consumption. The differential comparator without preamplifier will say 2-stage comparator.

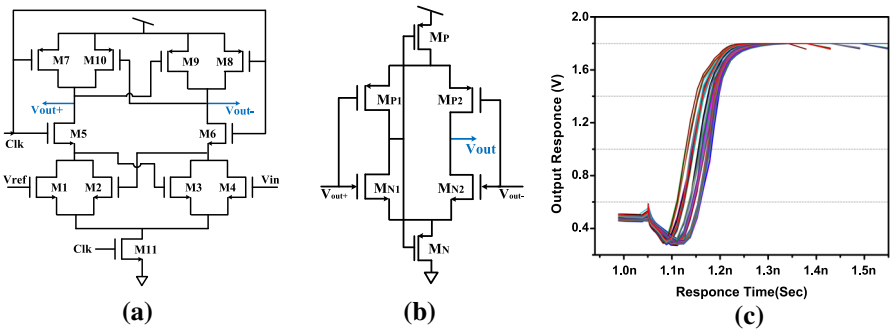

Fig. 3 **a** Proposed dynamic latch, **b** post-amplifier circuit, **c** Monte Carlo simulation for output response with load at all (process and mismatch) statistical variation

The 2-stage circuit consists of a proposed dynamic latch followed by post-amplifier and architecture, as shown in Fig. 3a, b, respectively. The proposed dynamic latch design contributes to the overall gain of a comparator. The proposed dynamic latch has an excellent driving strength with high voltage gain. The analog input $V_{\text{in}} \geqslant 0.5\,\text{V}$, and the performance of the comparator is as good as a 3-stage comparator at the given technology node. The use of 2-stage comparator is to reduce overall power consumption along with lower input offset voltage, which improves the gain for better matching. The total propagation delay (t_{P}) of a differential amplifier depends on the number of stages used, and it is calculated as:

$$t_{\text{P}} = t_{\text{Latch}} + t_{\text{Preamp}} \quad \text{whereas} \quad t_{\text{Latch}} = \frac{C_{\text{Load}}}{g_{\text{m}}} \ln\left(\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}}\right) \tag{2}$$

where ΔV_{in}, ΔV_{out}, C_{L}, and g_{m} are the differential input voltage, output voltage, load capacitance, and transconductance of latch, respectively.

The overall delay contribution by the differential comparator in real-time performance of the latch and the delay contribution by the latch are shown in Eq. (2). We have designed a dynamic latch with the minimum area and less delay by considering the delay parameters. The design principle and operation of a proposed differential latch are operated in preset and regeneration phase. During the preset/equalization phase when the clock is low, $M5$, $M6$, $M9$ and $M10$ are in cutoff mode and $M7$ and $M8$ are in on state. The drain of $M9$ and $M10$ transistors will charge toward V_{dd}, and $M7$ and $M8$ are an equalization of the differential output. Therefore, its output does not change in the equalization phase. When the clock is low, the output of the latch does not evaluate the input change. The MOS $M9$ and $M10$ are majorly responsible for the parasitic capacitance, which limits the bandwidth.

The current starts to flow during the regeneration phase, i.e., the clock is high and drain of $M5$ and $M6$ starts to discharge. The $M5$ and $M6$ are then used to pass the differential voltage from the input node to the regenerating stage. The cross-coupled transistors start to regenerate the differential voltage as $M5$ and $M6$ can't claim the output to the ground. Hence, the output nodes Out+ and Out− are discharged toward the ground. The input and reference voltage is connected to the $M1$–$M4$,

which are in the linear region and acts like voltage-controlled registers. Therefore, as the clock is high, we will get differential cross-coupled pair $M1$–$M4$ connecting the input differential signal to the output terminal. The $M9$ and $M10$ are for boosting magnitude toward the rail voltages, and $M11$ isolates the ground path when the clock is low, i.e., in preset phase. The coupled pair $M1$–$M2$ and $M3$–$M4$ gives the large input impedance. The large area of PMOS, i.e., $M9$ and $M10$, is taken for the design which gives the low output impedance. The above property of the design supports to increase the overall voltage gain of the comparator. The use of reconfigurable stages depends on the V_{th} of $M6$ and $M7$. If the input is less than 0.5 V the probability of noise and error is more; in that case preamplifier is used in the reconfigurable comparator for increasing the gain and preamplification, while for higher input range preamplifier can be bypassed and only used the two stages of the comparator. The modified dynamic latch is designed in such a way that preamplification and decision both are done by the proposed modified circuit. By doing this, we can save the huge power which is mostly consumed by preamplifier.

The comparator metastability occurs when very small signals appear at the input of the comparator and close to the comparator decision point which can be reduced using the $M7$, $M8$ and $M2$, $M3$, whereas $M2$ and $M3$ MOS supports the offset compensation and ground path during the regeneration phase. These MOSFETs help to compare the differential signal at the input. The small voltage input signal, i.e., in 'mV,' needs low noise sensitivity and high amplification gain, which is difficult to achieve on the same path. The 3-stage comparator is having high input impedance and very less variation at the reference voltage generation point as compared to the 2-stage comparator. The second stage is the post-amplifier, which is used to increase the slew rate. The overall proposed design increases the gain of the comparator and also minimizes the error specifically, which gives the logic signal (i.e., 0 or 1.8 V) from the output of the decision circuit.

The output stage buffer/post-amplifier should accept a differential input signal and does not have slew rate limitations for high-speed performance. The basic architecture of post-amplifier used for the design is shown in Fig. 3b. Table 1 gives the operating parameter specification for Monte Carlo simulation at 180 nm technology. We have applied power supply 1.8 V with $\pm$ 10% variation for worse-case performance. The W/L ratio for each transistor of the preamplifier and proposed dynamic latch is considered based on the circuit performance. We have simulated the proposed circuit at 2.4 GS/s with tolerable delay, and the observed voltage gain is 100 dB. The clock rise and fall time are considered as 25% of its on/off time.

2.3 Offset Voltage Compensation in a Proposed Dynamic Comparator

The input offset voltage is present in the comparator due to its positive feedback and transient response. However, it is difficult to predict the effect of offset analytically. The fully configurable dynamic comparator with no mismatch is reached in a balanced state. The time during transient in Fig. 3 response is $V_{\text{out}+} = V_{\text{out}-}$ in preset phase, and the voltage V_{in} can be applied to minimize the mismatch effect, and this voltage represents the input offset voltage. The mismatch and $\triangle V_{\text{in}}$ will affect the

bias magnitude of the comparator. In order to calculate offset voltage, a balanced state needs to be found to compensate mismatch. The mismatches in threshold voltage and current through $M5$ and $M6$ are the dominant factors which are responsible for the process variation. First, we have considered overall variation due to current factor $\beta = \mu C_{\text{ox}}\,\text{W/L}$ mismatch in transistor $M5$ and $M6$. However, $M2$ and $M3$ MOS is used in cross-manner for the compensation. The comparator to work at the balanced condition, $\triangle V_{\text{in}} = (V_{\text{OS}})_{M_5 M_6}$, which assures the offset compensation. The mismatch at the input is compensated using coupled transistor $M_{1,2,3,4}$. The offset voltage for M5 and M6 can be calculated as:

$$(V_{\text{OS}})_{M_{5,6}} = \frac{(\mu_n + \triangle\mu_{M_5})\left(\frac{W_5}{W_3}\right)(V_{\text{out}+} - V_{\text{s5}} - V_{\text{tn}})^2}{2\mu_n V_{\text{s5}}} - \frac{(\mu_{\text{n}} + \triangle\mu_{M_6})\left(\frac{W_6}{W_2}\right)(V_{\text{out}-} - V_{\text{s6}} - V_{\text{tn}})^2}{2\mu_{\text{n}} V_{\text{s6}}} \tag{3}$$

where V_{s5}, V_{s6} are the source node voltage. $\triangle\mu$ is the respective mobility variation during mismatch. V_{tn} and μ are threshold voltage and nominal mobility for NMOS, respectively.

3 Simulation Results and Discussion

In reference to the effectiveness of the proposed reconfigurable dynamic comparator, 180 nm CMOS technology from semiconductor laboratory is used. All the simulations are performed considering 1.8 V of supply voltage at $T = 27\,^{\circ}\text{C}$ operating temperature unless specified. The parameter specification of the proposed dynamic latch and preamplifier circuit is shown in Table 1.

Table 1 Parameter specification of the proposed dynamic latch and preamplifier

Process file	Proposed dynamic latch	Preamplifier
Power supply	$V_{\text{dd}} = 1.8\,\text{V} \pm 10\%$, $V_{\text{ss}} = 0\,\text{V}$	
Reference voltage	$V_{\text{ref}} = 0$–$1.8\,\text{V}$	
MOS sizing (W/L)	$M_{1,2,3,4} = (1.5\mu/0.180\mu)$	$M_{1,2} = (1.5\mu/0.180\mu)$
	$M_{5,6} = (1.0\mu/0.180\mu)$	$M_{3,4} = (1.0\mu/0.180\mu)$
	$M_{9,10} = (4.5\mu/0.180\mu)$	$M_5 = (4.5\mu/0.180\mu)$
Clock signal (CLK)	High = 1.8 V; low = 0 V	High = 1.8 V; low = 0 V
	Rise and fall time = 10 ps	Rise and fall time = 10 ps
	Speed = 2.4 GHz	Speed = 2.4 GHz
Switch (PMOS)	(W/L)$M_{7,8} = (1.5\mu/0.180\mu)$	M_6, $M_7 = (1.5\mu, 0.6\mu/0.180\mu)$

Table 2 Input voltage sensitivity of different comparators with temperature variation

Temperature (°C)	Input voltage sensitivity (μV/°C)			
	CMOS-LTE [9]	With active load [14]	3-Stage	2-Stage
25	500	100	17	13
50	460	125	14	11
75	440	132	13	10
100	320	140	11	10
125	280	146	10	9

3.1 Performance Metrics for Circuit Parameter

The proposed dynamic latch compared the input whether it is higher or lower than the reference level. We calculated the input sensitivity at different temperatures and also proposed the sensitivity of the proposed circuit w.r.t temperature. For the results, we considered a condition that minimum input voltage produces a consistent output. The constant output is assumed to represent a digital high or low level. Table 2 shows the input voltage sensitivity of state-of-the-art and proposed differential comparators. We found that the sensitivity of the proposed circuit is less affected by the temperature variation.

Table 3 summarizes the differential comparator performance metrics and compares it with the state of the art. The proposed comparator utilizes clock edges to generate voltage difference and directly latches this difference to post-amplifier, which enhances the speed of comparator. The hysteresis is the two different threshold voltages in the differential comparator observing at rising and falling threshold detection. In differential comparator for a very slowly varying input, output switching can be rather slow. For the calculation of hysteresis, the input signal must exceed the upper threshold (V_H) to transition low or below the lower threshold (V_L) to transition high. The power supply rejection ratio (PSRR) is the ability of a dynamic comparator to maintain its output voltage as its varying DC power supply. The PSRR is calculated using PSRR = (change in V_{dd})/(change in V_{out}). The input is driven with a voltage larger than the required and finds the response time for the proposed circuit and state

Table 3 Performance parameter metrics of differential comparators at 1.8 V power supply

Performance parameter	Comparators			
	CMOS-LTE [9]	With active load [14]	3-Stage	2-Stage
Technology CMOS	180 nm	180 nm	180 nm	180 nm
Sensitivity (μV) @27 °C	1000	10	0.1	0.13
Overdrive recovery time (pS)	71	175	35	23
PSRR (dB) @100 kHz	–	–	−43	−41
Hysteresis (mV)	15	85	10	15
Latching compatibility	No	Yes	Yes	Yes

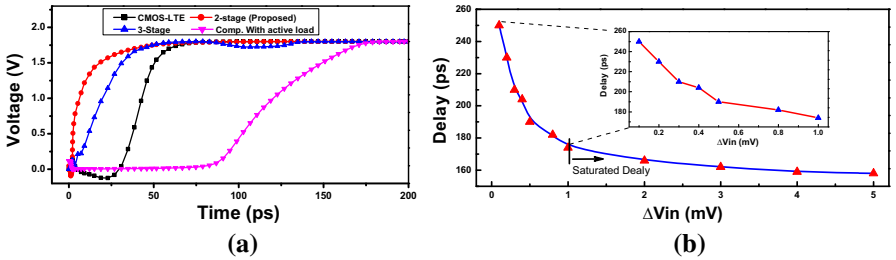

Fig. 4 **a** Settling and slewing behavior response with no load of proposed and state-of-the-art comparators during threshold detection, **b** delay variation of proposed comparator with change in input voltage difference (ΔV_{in}), i.e., the reference node voltage and the input voltage

of the art. The settling time is considered as 90% of its saturation value and response time is to reach 100% of its saturation value. However, the response time depends on the value of the overdriven voltage for a given input amplitude. The results demonstrate that the sensitivity of proposed 2-stage comparator is very less compared to other considered comparators. The 0.1 nV of sensitivity for the proposed 2-stage comparator provides the less voltage difference to sense. The proposed comparator has 3.09× less overdrive recovery time as compared to CMOS-LTE comparator. The proposed 2-stage comparator also has the latching capability which provides better performance of the circuit.

The proposed prototype can achieve competitive energy efficiency when compared with other voltage domain comparators. The voltage response concerning time is demonstrated in Fig. 4a which refers to the slew rate of a comparator. It helps us to identify maximum input frequency and amplitude applicable to the amplifier such that the output is not significantly distorted. The simulation results show the performance for different types of comparator at threshold crossing. In the proposed dynamic latch, area for $M9$ and $M10$ is more as shown in Fig. 3a which gives low output impedance. The simulation results of comparator transient response give a distinct idea for the speed of comparator. However, in line with the views of reconfigurability, the result demonstrates that the 2-stage comparator provides better performance with low power and high resolution. From the result, it is observed that the 2-stage comparator has a faster response as compared to the state of the art.

The working principle and result analysis of 2-stage and 3-stage comparator are described in Sect. 3. We performed the Monte Carlo simulation for the power consumption and found that the proposed 2-stage comparator has an average power of 86.15 μW with 3.73 μW of standard deviation. The voltage gain is 100 dB, and the Monte Carlo simulation gives average power consumption is 523.40 μW with standard deviation of 11.08 μW for a 3-stage comparator. This is due to mismatch and observes that the deviation for the proposed 2-stage comparator is very less as compared to the 3-stage comparator. From the simulation results, it proves that the preamplifier stage consumes more power as compared to later stages. This suggests that we will bypass in runtime and used proposed dynamic latch-based differential amplifier to save the power. This result highlights the runtime reconfigurability to save power and circuit complexity. The results conclude that the application-based reconfigurability in

architecture gives flexibility in operation and its characteristics. The proposed 2-stage comparator which simulated and measured the delay with respect to the differential input voltage is shown in Fig. 4b. It is proved that with increasing differential input voltage, the measured delay of the comparator decreases. Moreover, at a given V_{DD} supply, the larger differential voltage at the input provides smaller comparator delay. From the results, it is also concluded that the proposed comparator delay is inversely proportional to the input voltage difference of the input node and reference node voltages. From the above discussions, we can find that higher input voltage difference results in the minor output delay and vice versa. Through the cooperation among the calibration circuit, the proposed design can operate at 2.4 GS/s with 1.8 V power supply.

The voltage gain of the reconfigurable comparator is 100 dB at $f_{3\,\mathrm{dB}}$, i.e., the frequency at which the first pole occurs. The performance of the proposed architecture is better, which is revealed by comparing with the previous state of the arts. The 1000 Monte Carlo simulations have been performed for 3-stage and 2-stage comparator, as shown in Fig. 5. The result shows that the standard deviation in terms of power variation is less for 2-stage comparator as compared to the 3-stage comparator. The results clearly indicate the effect of device mismatch, and process variation effect is less in the proposed design. The performance comparison of the different comparator circuits is shown in Table 4. The observation shows that the proposed 2-stage comparator consumes less power as compared to previous works, including 3-stage comparator. The power consumption by the proposed design is 83.15 µW at 2.4 GS/s.

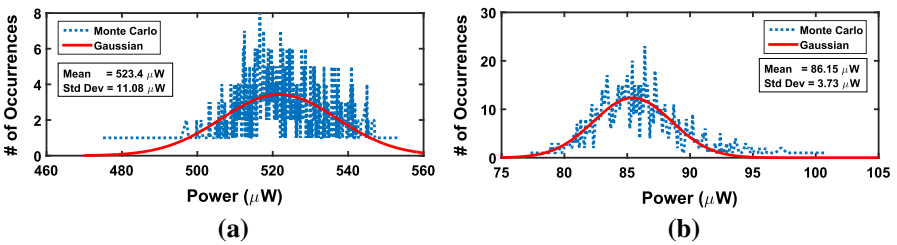

Fig. 5 1000 Monte Carlo simulations for process variation and mismatch with mean power variation for **a** 3-stage comparator, **b** proposed reconfigurable with 2-stage comparator

Table 4 Performance comparison of various comparators at 180 nm process at 1.8 V with ±10% supply variation

Comparators	Max. sampling frequency (GS/s)	Average power @500 MHz (µW)	Voltage gain (dB)
CMOS-LTE [9]	1	560	60
Comparator with active load [14]	0.5	172	80
Double-tail dynamic comparator [3]	1.8	160	–
3-Stage dynamic comparator	2.4	554	100
Proposed reconfigurable with 2-stage	2.4	83.15	100

The significant amount of power is reduced by bypassing the preamplifier stage in cascaded connection using an analog switch that controls the input signal. The proposed 2-stage comparator can operate faster and consume low power while using the reconfigurable technique; we can use 2-stage of comparator along with preamplifier. The simulated parameter for the proposed 2-/3-stage comparator is shown in Table 4.

3.2 PVT Variation for Performance and Comparison

The impact of the process, voltage, and temperature (PVT) variations on the circuit performance is an important measure for the stable circuit performance. The effect of PVT variations on the comparator response time is shown in Fig. 6. The response time of different considered circuits at the different process corners which are slow–slow (SS), fast–fast (FF), slow–fast (SF), fast–slow (FS), and typical–typical (TT) is shown in Fig. 6a. The results show that the response time of the proposed 2-stage comparator is less as compared to all other considered circuits for various process corners. The supply voltage of the design can vary from its fixed ideal value with day-to-day operation and environmental conditions. Moreover, the supply voltage is responsible for the saturation current, which is indirectly responsible for the signal propagation delay. Figure 6b shows the circuit response time with supply variation for circuit design and observes that the response time decreases with increasing supply voltage for all the considered comparators. The result shows that the effect of supply variation on the response time of proposed 2-stage comparator is less as compared to all other considered circuits. The response time sensitivity with supply voltage is less for proposed 2-stage comparator as compared to a comparator with active load and 3-stage comparator.

The temperature variation also affects the circuit performance mostly as a linear scaling effect at 180 nm silicon process. We have simulated the response behavior for the proposed circuit with the different operating temperatures at 1.8 V supply voltage and TT process corner, as shown in Fig. 6c. The result shows that the response time increases with the increasing operating temperature. The change in response time with temperature for the proposed 2-stage comparator is less as compared to the CMOS-LTE and 3-stage comparator.

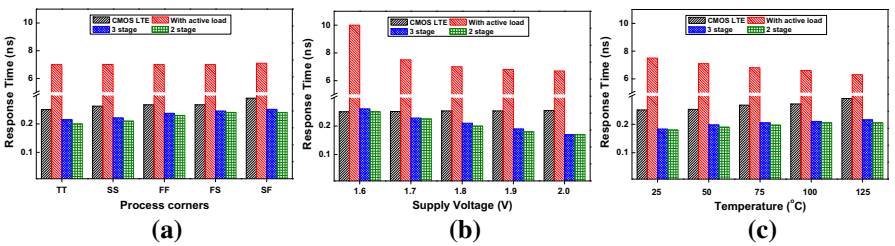

Fig. 6 Effect on comparator response time with the PVT variations. **a** Response time with process variation, **b** response time with supply variation, **c** response time with temperature variation

4 Conclusion

In this paper, a power-efficient, high-resolution reconfigurable comparator is designed using SCL 180 nm CMOS technology at the supply voltage of 1.8 V. We present a runtime reconfigurable differential amplifier circuit design for low-power application operates at 2.4 GS/s and significantly reduce the active power in the circuit by using the configurable technique. The proposed architecture is divided into two steps of algorithm implementation depending on the analog input to the circuit. In comparison with previous state of the art, the proposed architecture results are better and 83.2% power efficient compared to the 3-stage comparator. This reconfigurable technique with proposed dynamic latch-based comparator gives very high speed conversion with low power consumption; hence, it is very useful in flash-type ADC application. The power-hungry preamplifier stage is bypassed in the multistage comparator for the higher input signal ($\geq V_{\text{th}}$) which results in huge power saving and not requires any kind of extra processing blocks. The results of the proposed circuit claim that the use of the reconfigurable technique will have the option for power-saving mode.

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