Separation of electron and hole trapping components of PBTI in SiON nMOS transistors

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ABSTRACT

In nMOS transistors the impact of positive bias temperature instability (PBTI) on the device performance is typically considered negligible and has thus been barely studied in the past. However, an accurate description of this phenomena requires and in depth understanding of the physical origin being responsible for the change of the device characteristics over time. For the assessment of PBTI in nanoscale SiON nMOS transistors we make use of the time-dependent defect spectroscopy (TDDS) and examine the device performance degradation at the single-defect level. Contrary to what is visible in large-area devices, our investigations clearly reveal that charge trapping at both electron and hole traps contributes to the overall drift of the threshold voltage in these devices. Furthermore we observe that hole traps account for around 20% of the total threshold voltage drift. To evaluate the impact of single-defects on the device performance we characterize the charge trapping kinetics of a number of defects, which can be explained by employing a two-state defect model. In our approach we observe charge trapping due to defect/channel interaction for electron traps and defect/gate interaction for hole traps. The extracted trap levels and trap depths clearly reveal that the electrically active electron traps reside closer to the SiON/Si interface while the hole traps are located closer to the poly-Si/SiON interface. Finally, the extracted trap parameters are fully consistent with defect candidates for electron and hole trapping from DFT calculations.

1. Introduction

The fast progress in microelectronics has resulted in a continuation of device scaling into the nano-meter regime. Next to the device geometry, the gate insulator layer used in metal-oxide semiconductor transistors (MOSFETs) has been scaled as well. In order to investigate the reliable operation of MOS devices, different measurement methods like stress-IV measurements [1], on-the-fly measurements [2], measure-stress-measure (MSM) experiments [3] and noise measurements [4] are among others often applied. Many of the experiments aim at investigating the so-called bias temperature instability (BTI), which manifests itself as a drift of the threshold voltage over time [3,5]. In general BTI can be classified into positive BTI (PBTI) and negative BTI (NBTI), where the terms positive and negative refer to the sign of the gate bias. The origin of the observed drift of the threshold voltage lies in charging and discharging events of defects located at the semiconductor/insulator interface or of defects located inside the oxide. Next to charge trapping at existing defects, new defects can become created during device operation even at nominal bias conditions. In large-area MOSFETs, a number of such defects exists and their interaction with the carrier reservoirs, i.e. the channel and/or the gate, results in a continuous drift of the threshold voltage over time when MSM measurements are performed [6]. However, in nanoscale devices where only a handful of defects are present, charge transitions of individual defects are discrete steps in the corresponding measurement data revealing the physical origin of charge trapping more closely [3,7]. This makes it possible to elaborately study the contributions of electron and hole traps. In large-area nMOS devices, however, the individual contributions canceled out each other, and thus only a very weak average impact of BTI on the device threshold voltage can be observed.

So far, a large number of single-defect studies have been performed considering NBTI in devices employing SiON or SiO$_2$ as gate insulator [3,8–16]. However, only little attention has been paid to PBTI in nMOS device since in pMOS devices the active defect density is approximately 10 times larger than in nMOS [7], BTI is typically considered more important for pMOS transistors. Nevertheless, for CMOS applications BTI of both device types is of significant importance, and the understanding of the physical origin of charge trapping in these devices is vital for further optimization of devices and circuits. Furthermore, it appears to be reasonable to assume the same defects are present in nMOS and pMOS devices and are triggered in a different way due to different positions of the Fermi levels in the channel and gate. As a consequence, after studying the response of these defects under as many different bias and temperature conditions as possible is important to

improve our understanding of their behavior. Critical questions in this regard are the magnitude of the trap density, the impact of a defect on the overall device performance, and also the trap polarity, trap distribution and the trap levels. The most accurate way to answer these questions is by performing a detailed single-defect study employing nanoscale nMOS devices to provide the missing information.

2. Experimental

In this work, planar SiON n-channel MOSFETs with W = 90 nm, L = 70 nm, and an EOT = 2.2 nm are studied using time-dependent defect spectroscopy (TDDS). The devices under test (DUTs) are stressed at constant gate voltages varying between $V_G^s \in [1.6\,V, 3.0\,V]$, whereas the drain-source voltage is held at $V_{DS}^s = 0$ V during stress to prevent any hot-carrier degradation related effects. After each stress cycle, a recovery gate voltage in the range of $V_G^r \in [0.3\,V, 1.2\,V]$ is applied to the gate while the drain-source current at $V_{DS}^r = 100$ mV is recorded at the same time. Afterwards, the recorded source current is converted to a threshold voltage shift and the recovery behavior is analyzed [17,18]. In contrast to large-area devices, the recovery in nanoscale transistors after PBTI stress proceeds in a discrete manner, see Fig. 1. The recovery traces are typically given in terms of an equivalent shift of the threshold voltage ΔV_{th}, which is obtained from the measured drain current using an initial $I_D(V_G)$ curve. To achieve highest measurement resolution for single charge transitions of $\Delta V_{th} < 1$ mV an optimized defect probing instrument [5] has been used. This enables to observe a number of electron emission events (Fig. 1 (left)), but quite remarkably also a significant number of hole traps with steps in the opposite (positive) direction, see Fig. 1 (middle). In contrast, no electron emission events are visible in the recovery traces measured on pMOS devices of similar geometry, see Fig. 1 (right). While the lack of observable electron trapping in pMOS devices may be due to the higher noise level, the presence of electron and hole trapping in nMOS devices signifies an important difference between NBTI and PBTI.

3. Defect distribution function

To study the relative contribution of electron and hole trapping to the total threshold voltage shift ΔV_{th}, the complementary cumulative distribution functions (CCDFs) of the step heights of 79 nMOS transistors of the same technology is evaluated, see Fig. 2. The shown CCDF can be approximated by a bi-modal exponential distribution as

$$1 - \mathrm{CDF} = A_1 e^{-\frac{\Delta V_{th}}{\eta_1}} + A_2 e^{-\frac{\Delta V_{th}}{\eta_2}}, \tag{1}$$

with $A_{1,\,2} = N_{T1,\,2} \times n_T/n_d$ being the product of the trap number per device N_T and the ratio between the overall number of traps n_T and the number of devices n_d. $\eta_{1,2}$ denotes the mean contribution of a single
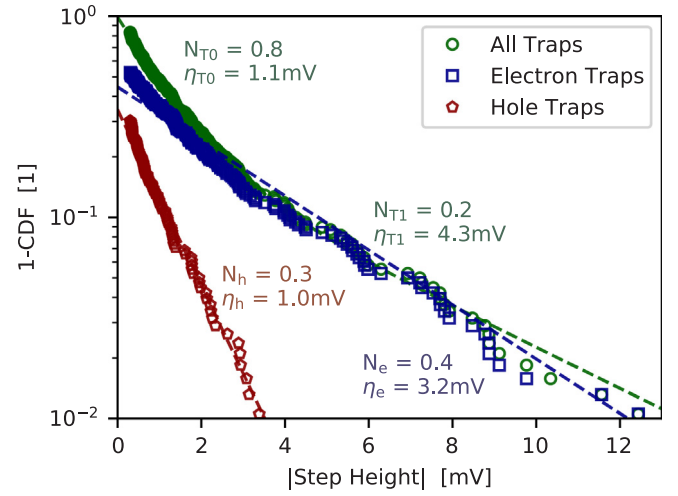

Fig. 2. The step height distribution of planar n-channel MOSFETs. The distribution function of all steps appears to be bi-modal. The bi-modal distribution can be separated into two (nearly) exponential distributions attributed to hole and electron traps.

charge capture/emission event [6,15,16,19]. In the following, the bi-modality of the CCDF is separated into two (nearly) uni-modal distributions, which can be attributed to hole and electron traps. The resulting partial distributions show that on average hole traps have smaller step heights than electron traps indicating that they are further away from the channel. Considering the trap density, a remarkable number of 106 defects (38%) are identified as hole traps among a total of 266 traps.

The absolute contribution of hole trapping to the total threshold voltage shift ΔV_{th} is calculated by

$$r_h = \frac{\sum_i^{N_h} |d_{h_i}|}{\sum_i^{N_h} |d_{h_i}| + \sum_i^{N_e} |d_{e_i}|}, \tag{2}$$

with the step heights of the single hole/electron emission events d_{h_i} and d_{e_i}, respectively, and is analyzed in Fig. 3. It can be observed that hole trapping decreases the total ΔV_{th} by about 22% for the bias and temperature conditions used here, while the fraction of hole traps is around 40%. These finding suggests that hole trapping plays an important role in the context of PBTI.

Of further interest is that the significantly smaller step heights for hole traps compared to electron traps observed from the CCDFs, give rise to the assumption that hole traps might be located at a larger distance from the channel than electron traps. To settle this question the
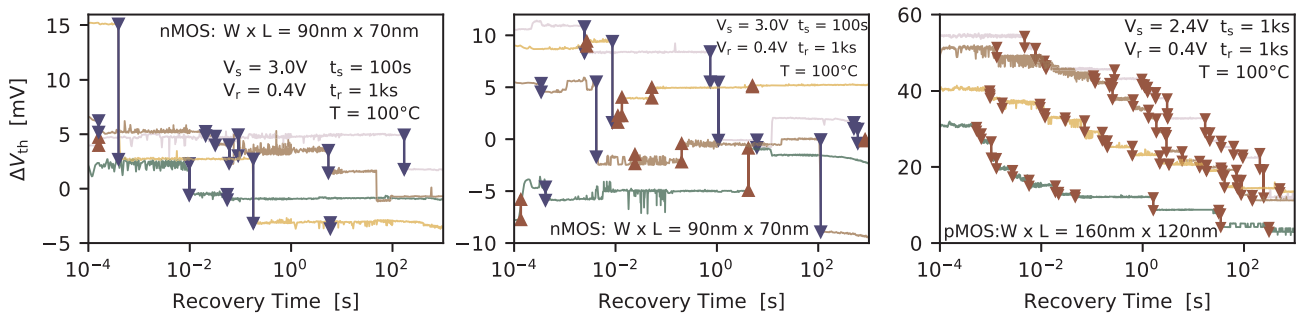

Fig. 1. Selected recovery traces of several planar n-channel MOSFETs recorded after PBTI stress clearly show (left) electron emission events (blue) with negative steps and also (middle) hole emission events (red) with positive steps. (Right) For comparison, the recovery traces of nanoscale planar p-channel MOSFETs (right) show many more steps and noise, which is due to the higher trap density compared to their n-channel counterparts. Note that the discrete steps originating from noise and RTN are not marked in the traces. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)
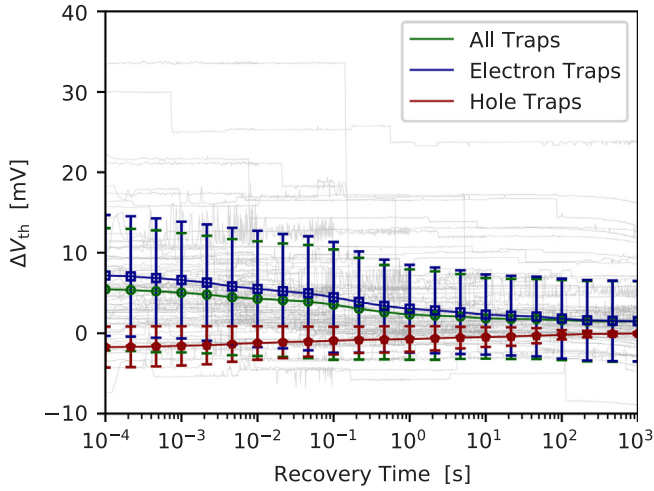
Fig. 3. The average recovery behavior for nMOS transistors (light grey) which are used to create the CCDFs of Fig. 2. The major contribution to the threshold voltage shift originates from electron traps, but there is a sizable reduction of about 20% due to hole trapping to PBTI.

charge trapping kinetics of a number of hole and electron traps are evaluated next.

4. Single defects

In order to study the bias and temperature dependence of the charge capture and emission times, of single-defects we employ the TDDS [9]. Using TDDS the charge capture and emission times can be extracted under various bias conditions from a number of defects. To extract the charge emission time, stress ($V_{DS} = 0\,V$, $V_G = V_G^s$) and recovery ($V_{DS} = 0.1\,V$, $V_G = V_G^r$) cycles are repeatedly applied, and the recovery behavior is measured. During one measurement series, typically 100 traces are recorded at the same bias and temperature. Afterwards the discrete steps of the ΔV_{th} transients are extracted and plotted as a distribution of the emission time versus their step heights (τ_e, d). Such graphs are called spectral maps, see Fig. 4 (bottom).

After collecting all emission events from repeated stress/recovery measurements at constant biases and temperature, the single charge emission events form clusters in the spectral maps. Each cluster serves
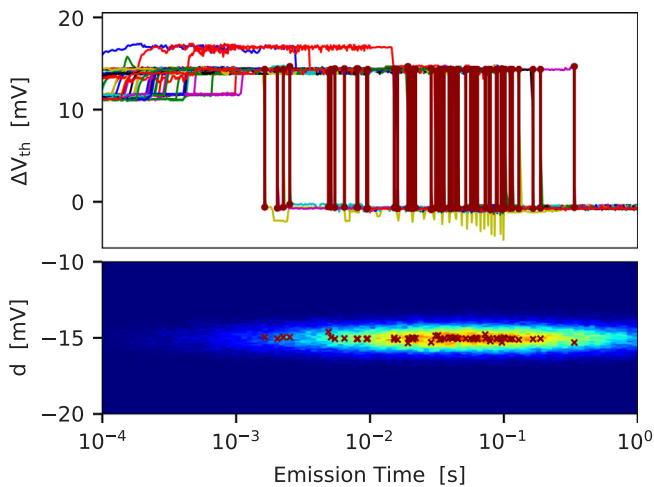

Fig. 4. By repeatedly applying stress and monitoring the recovery behavior afterwards, the charge transition events of a single defect can be recorded. These steps are extracted and binned into a histogram, called the spectral map. The charge emission time is given by the mean time of all emission events at a given bias and temperature.
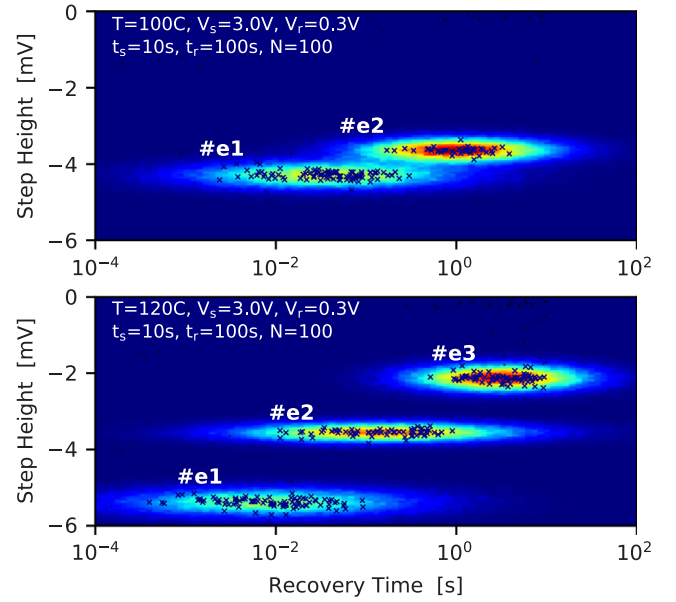

Fig. 5. The spectral maps for one device at two different temperatures demonstrate the temperature dependence of several properties of particular defects represented by the clusters. For this device three electron traps with negative step heights can be observed.

as a fingerprint for one individual defect. The intensity of a cluster is directly proportional to the number of emission events contributing to it. Furthermore, the number of capture and emission events is correlated because the charge has to be captured during stress phase first for emission to occur. Thus, the higher the ratio between the stress time and the average capture time of the defect is, the larger the probability of the defect to capture a charge during stress becomes. Finally, the vertical positions of the clusters in the spectral maps reflect the contribution of the single defects to total ΔV_{th} at certain bias conditions and temperatures. From the spectral maps the emission time is calculated as the average of all single emission events of a certain defect.

In one of the DUTs we identified three electron traps, i.e. traps with negative step heights (Fig. 5). As can be seen, the defects #e1 and #e2 reduce their emission time by approximately 50% while defect #e3 moves into the measurement window defined by the recovery time $t_r = 10\,s$. On another device we observed two hole traps with a positive step height (Fig. 6). Similarly to the electron traps, the hole trap emission time also decreases with higher temperature. This observation confirms previous findings that both electron and hole trapping are temperature-activated processes [9,15,16,20].

Also in agreement with reports on NBTI on pMOS transistors, the probability of a defect to capture a charge during stress increases with higher stress voltage and stress time. This allows the extraction of the characteristic capture time for a hole/electron defect using the relation

$$k_e/k = A(1 - e^{-t/\tau_c}), \tag{3}$$

with the number of traces k and the number of emission events k_e [3,7,9].

5. Results

In the following we evaluate the trap depth and trap levels of our defects. Previous reports have demonstrated that there is a direct correlation between the average contribution of traps to ΔV_{th} and the trap depth ($\eta \propto x_T$) [15,16,21]. However, from TDDS experiments it has been observed that defects can change their contribution to the threshold voltage shift when the device electrostatics at which the recovery is recorded changes [15,16,22]. As such, the step height alone is not a reliable indicator for the trap depth. To achieve an accurate estimate for
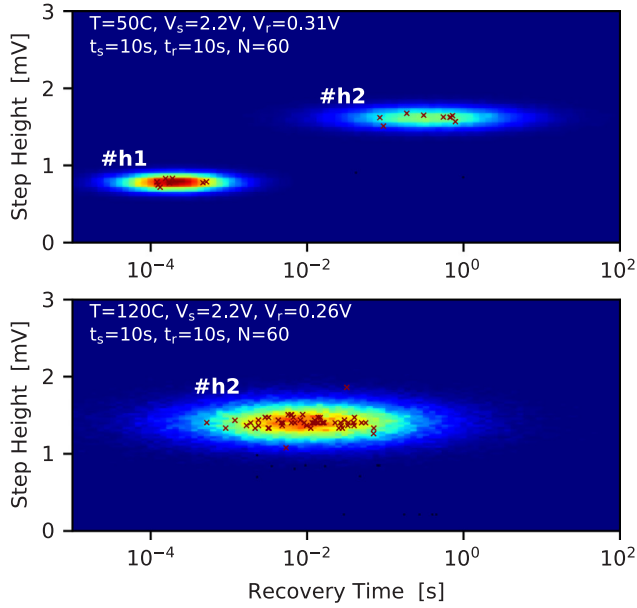
Fig. 6. Similarly to the electron traps, the two hole traps #h1 and #h2 with positive step heights move towards lower emission times with increasing temperature. Defect #h1 is shifted out of the measurement window when the device temperature is increased by 70 °C.
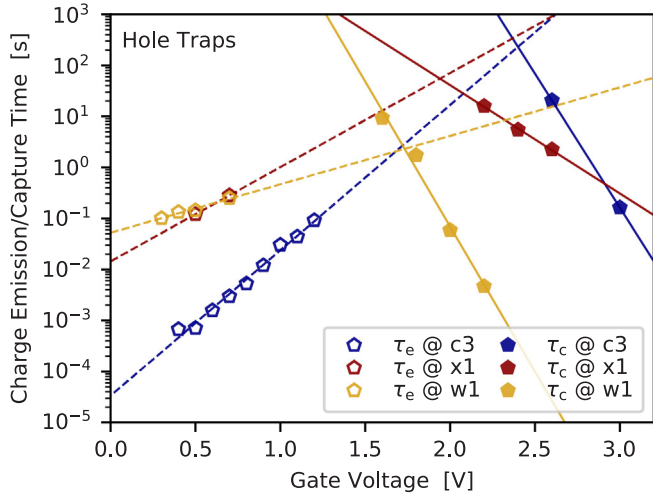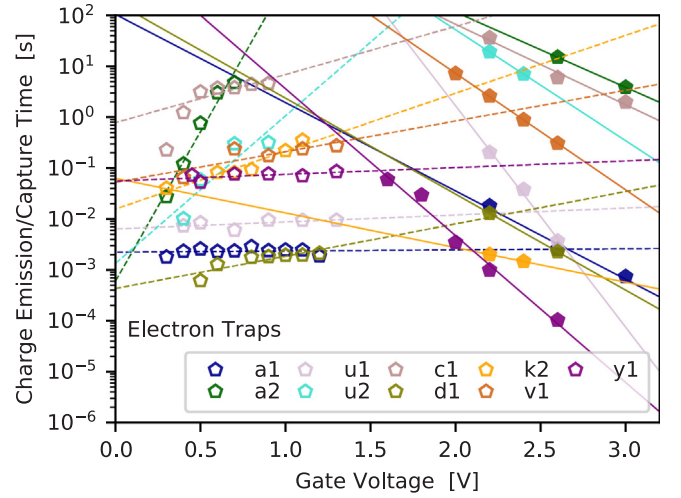

Fig. 7. All measured charge emission and capture times from hole traps (symbols). The charge transition times are fitted using a two-state NMP trapping model (lines).

the trap position inside the band diagram we evaluate the charge trapping kinetics of three hole traps (Fig. 7) and nine electron traps (Fig. 8) extracted from our extensive measurements. To explain the charge capture and emission time characteristics we employ a two-state NMP defect model [23–26]. Considering this model the charge capture and emission time can be expressed by

$$\frac{1}{\tau_{c,e}} = k_{c,e}^0 \exp\left(-\frac{\Delta E_{c,e}}{k_B T}\right), \tag{4}$$

with the prefactor $k_{c,e}^0$ and the energy barrier $\Delta E_{c,e}$ for charge capture and emission. A fundamental fact is that if the trap level equals the Fermi level of the respective carrier reservoir for charge trapping, i.e. $E_t = E_F$, the charge capture time equals the charge emission time. With the above expression at hand, the trap position can be estimated by [26].

Fig. 8. Charge emission (open symbols) and capture times from electron traps (filled symbols). The measured behavior can be nicely described by the two-state model over a wide bias range.

$$d = -\frac{k_B T}{q_0} t_{ox} \frac{\partial}{\partial V_G}(\ln \tau_c - \ln \tau_e), \tag{5}$$

with the oxide thickness t_{ox} and q_0 the elementary charge. Furthermore, the trap level can be calculated using [26]

$$E_T = E_F + q_0 \frac{d}{t_{ox}} V_{Gi}, \tag{6}$$

where V_{Gi} denotes the gate bias of the intersection point of the charge transition rates, e.g. $V_{Gi} = V_G$ where $\tau_c = \tau_e$. It has to be noted that a two-state trapping model has been recently used to provide a consistent explanation for charge trapping in various technologies [26,27].

The estimated trap positions and trap levels for the analyzed traps are collected in the band diagram in Fig. 9. A necessary condition for a defect to contribute to ΔV_{th} is that the defect must be energetically located in the so called active energy region (AER) for charge trapping. In general, defects below the Fermi level of a certain carrier reservoir, e.g. the Fermi level of the channel and the poly-gate in our MOSFETs,
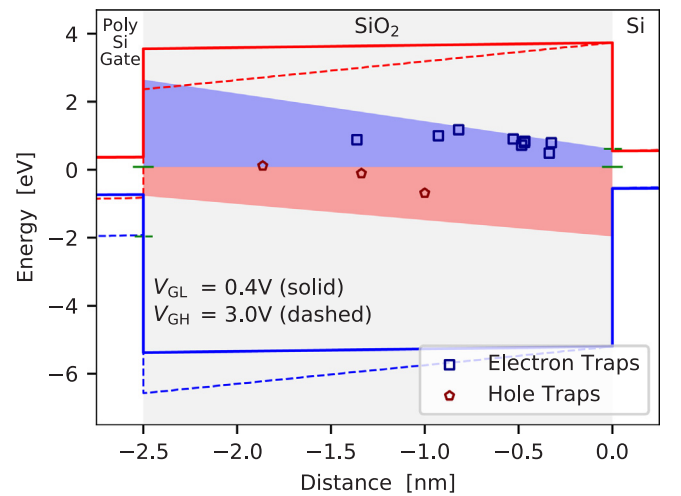
Fig. 9. The band diagram shows the trap positions and trap levels extracted for single electron and hole traps. Also shown are the active energy regions (AERs) for charge transitions between the defects and the channel (blue) and for charge transitions between the defects and the poly-gate (red). All identified traps are located in one of the AERs confirming the accuracy of our study. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

are charged and become uncharged once they are shifted above the Fermi level, provided that the bias is applied for a longer time larger than the charge capture and emission time of the respective defect. Thus, the bias used for the MSM measurements determines the energetic area spanned by the AER for charge exchange between the channel and the defects, but also between the poly-gate and the defects. As can be seen in Fig. 9 the trap levels of the evaluated defects lie all inside the AERs. While the positions of the electron traps are found to be closer to the channel, the hole traps tend to reside more closely to the poly-gate. Note that, in accordance with the defect model, the spatial position is mainly determined by the gate bias dependence of the charge capture time. The observation that hole traps with smaller step heights are found to be located at a larger distance from the channel is also fully consistent with the smaller average step height extracted from the CCDF of step heights.

Finally it is worth mentioning that the trap levels of our study are in good agreement with DFT calculations suggesting that the oxygen vacancy is a potential trap candidate for electron trapping [28,29], while hydrogen-related defects could be responsible for hole trapping [30,31].

6. Conclusion

By studying PBTI in SiON nMOS devices at the single-defect level we have observed electron traps in addition to a sizable number hole traps. Furthermore, we observe a bi-modal exponential step height distribution one mode corresponding to electron traps and the second one to hole traps. Our study reveals that at the used bias conditions about 40% of the observed defects are hole traps, which are responsible for about 20% of the overall device degradation. The involvement of both electron and hole traps is a significant difference to the NBTI case. To extract trap parameters, we study the charge trapping kinetics of a number of hole and electron traps, which we explain using a two-state model. The obtained trap parameters indicate that hole traps reside more likely in the middle of the insulator, while electron traps are more likely located near the channel. Finally, the calculated trap positions and trap levels for charge trapping in nMOS transistors, and are fully consistent with trap levels for electron traps and hole traps extracted from DFT calculations.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

References

[1] E. Bury, R. Degraeve, M.J. Cho, B. Kaczer, W. Goes, T. Grasser, N. Horiguchi, G. Groeseneken, Study of (correlated) trap sites in SILC, BTI and RTN in SiON and HKMG devices, Proc. Intl. Symp. on Physical and Failure Analysis of Integrated Circuits, 2014, pp. 250–253.

[2] M. Denais, C. Parthasarathy, G. Ribes, Y. Rey-Tauriac, N. Revil, A. Bravaix, V. Huard, F. Perrier, On-the-fly characterization of NBTI in ultra–thin gate oxide pMOSFET's, Proc. Intl. Electron Devices Meeting (IEDM), 2004, pp. 109–112.

[3] T. Grasser, H. Reisinger, P.-J. Wagner, B. Kaczer, The time dependent defect spectroscopy for the characterization of border traps in metal-oxide-semiconductor transistors, Phys. Rev. B 82 (24) (2010) 245318.

[4] A.P. van der Wel, E.A.M. Klumperink, S.L.J. Gierkink, R.F. Wassenaar, H. Wallinga, MOSFET 1/f noise measurement under switched bias conditions, IEEE Electron Device Lett. 21 (1) (2000) 43–46.

[5] M. Waltl, Ultra-low noise defect probing instrument for defect spectroscopy of MOS transistors, IEEE Trans. Dev. Mat. Rel. 20 (2020) 242–250.

[6] B. Kaczer, P.J. Roussel, T. Grasser, G. Groeseneken, Statistics of multiple trapped charges in the gate oxide of deeply scaled MOSFET devices – application to NBTI, IEEE Electron Device Lett. 31 (5) (2010) 411–413.

[7] M. Waltl, W. Goes, K. Rott, H. Reisinger, T. Grasser, A single-trap study of PBTI in SiON nMOS transistors: similarities and differences to the NBTI/pMOS case, Proc. Intl. Rel. Phys. Symp. (IRPS), 2014, pp. XT18.1–XT18.5.

[8] R. Wang, S. Guo, Z. Zhang, J. Zou, D. Mao, R. Huang, Complex random telegraph noise (RTN): what do we understand? Proc. Intl. Symp. on Physical and Failure Analysis of Integrated Circuits, 2018, pp. 1–7.

[9] T. Grasser, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, B. Kaczer, The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability, Proc. Intl. Rel. Phys. Symp. (IRPS), 2010, pp. 16–25.

[10] B. Kaczer, T. Grasser, J. Martin-Martinez, E. Simoen, M. Aoulaiche, Ph.J. Roussel, G. Groeseneken, NBTI from the perspective of defect states with widely distributed time scales, Proc. Intl. Rel. Phys. Symp. (IRPS), 2009, pp. 55–60.

[11] H. Reisinger, U. Brunner, W. Heinrigs, W. Gustin, C. Schlunder, A comparison of fast methods for measuring NBTI degradation, IEEE Trans. Dev. Mat. Rel. 7 (4) (2007) 531–539.

[12] J.P. Campbell, J. Qin, K.P. Cheung, L.C. Yu, J.S. Suehle, A. Oates, K. Sheng, Random telegraph noise in highly scaled nMOSFETs, Proc. Intl. Rel. Phys. Symp. (IRPS), 2009, pp. 382–388.

[13] T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, Y. Hayashi, New analysis methods for comprehensive understanding of Random Telegraph Noise, Proc. Intl. Electron Devices Meeting (IEDM), 2009, pp. 1–4.

[14] D. Veksler, G. Bersuker, L. Vandelli, A. Padovani, L. Larcher, A. Muraviev, B. Chakrabarti, E. Vogel, D.C. Gilmer, P.D. Kirsch, Random telegraph noise (RTN) in scaled RRAM devices, Proc. Intl. Rel. Phys. Symp. (IRPS), 2013, pp. MY.10.1–MY.10.4.

[15] M. Toledano-Luque, B. Kaczer, E. Simoen, Ph.J. Roussel, A. Veloso, T. Grasser, G. Groeseneken, Temperature and voltage dependences of the capture and emission times of individual traps in high-k dielectrics, Microelectron. Eng. 88 (7) (2011) 1243–1246.

[16] M. Toledano-Luque, B. Kaczer, Ph.J. Roussel, J. Franco, L.A. Ragnarsson, T. Grasser, G. Groeseneken, Depth localization of positive charge trapped in silicon oxynitride field effect transistors after positive and negative gate bias temperature stress, Appl.Phys.Lett 98 (18) (2011) 183506.

[17] M. Waltl, P.-J. Wagner, H. Reisinger, K. Rott, T. Grasser, Advanced data analysis algorithms for the time–dependent defect spectroscopy of NBTI, Proc. Intl. Integrated Reliability Workshop (IIRW), 2012, pp. 74–79.

[18] B. Ullmann, K. Puschkarsky, M. Waltl, H. Reisinger, Tibor Grasser, Evaluation of advanced MOSFET threshold voltage drift measurement techniques, IEEE Trans. Dev. Mat. Rel. 19 (2) (2019) 358–362.

[19] B. Kaczer, T. Grasser, P.J. Roussel, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simoen, G. Groeseneken, H. Reisinger, Origin of NBTI variability in deeply scaled pFETs, Proc. Intl. Rel. Phys. Symp. (IRPS), 2010, pp. 26–32.

[20] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, C. Schlunder, Analysis of NBTI degradation- and recovery-behavior based on ultra fast VT–measurements, Proc. Intl. Rel. Phys. Symp. (IRPS), 2006, pp. 448–453.

[21] A. Ghetti, C.M. Compagnoni, F. Biancardi, A.L. Lacaita, S. Beltrami, L. Chiavarone, A.S. Spinelli, A. Visconti, Scaling trends for random telegraph noise in deca-nanometer flash memories, Proc. Intl. Electron Devices Meeting (IEDM), 2008, pp. 1–4.

[22] A. Asenov, R. Balasubramaniam, A.R. Brown, J.H. Davies, RTS amplitudes in de-cananometer MOSFETs: 3-D simulation study, IEEE Trans. Electron Devices 50 (3) (2003) 839–845.

[23] K.S. Ralls, W.J. Skocpol, L.D. Jackel, R.E. Howard, L.A. Fetter, R.W. Epworth, D.M. Tennant, Discrete resistance switching in submicrometer silicon inversion layers: individual interface traps and low-frequency $\left(\frac{1}{f}\right)$ noise, Phys. Rev. Lett. 52 (1984) 228–231.

[24] M.J. Kirton, M.J. Uren, Noise in solid-state microstructures: a new perspective on individual defects, interface states and low-frequency (1/f) noise, Adv.Phys 38 (4) (1989) 367–486.

[25] T. Nagumo, K. Takeuchi, T. Hase, Y. Hayashi, Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps, Proc. Intl. Electron Devices Meeting (IEDM), 2010, pp. 628–631.

[26] B. Stampfer, F. Schanovsky, T. Grasser, M. Waltl, Semi-automated extraction of the distribution of single defects for nMOS transistors, MDPI Micromach. 11 (2020) 1–11.

[27] Gerhard Rzepa, J. Franco, Barry J. O'Sullivan, A. Subirats, Marko Simicic, Geert Hellings, P. Weckx, Markus Jech, Theresia Knobloch, Michael Waltl, Philippe J. Roussel, D. Linten, Ben Kaczer, Tibor Grasser, Comphy – a compact-physics framework for unified modeling of BTI, Microelectron. Reliab. 85 (1) (2018) 49–65.

[28] A.-M. El-Sayed, M.B. Watkins, V.V. Afanas'ev, A.L. Shluger, Nature of intrinsic and extrinsic electron trapping in SiO^{-2}, Phys. Rev. B 89 (2014).

[29] A.V. Kimmel, P.V. Sushko, A.L. Shluger, G. Bersuker, Positive and negative oxygen vacancies in amorphous silica, ECS Trans. 19 (2009) 2–17.

[30] T. Grasser, K Rott, H. Reisinger, M. Waltl, P.-J. Wagner, F. Schanovsky, W. Goes, G. Pobegen, B. Kaczer, Hydrogen-related volatile defects as the possible cause for the recoverable component of NBTI, Proc. Intl. Electron Devices Meeting (IEDM), 2013.

[31] T. Grasser, W. Goes, Y. Wimmer, F. Schanovsky, G. Rzepa, M. Waltl, K. Rott, H. Reisinger, V.V. Afanas'ev, A. Stesmans, A.-M. El-Sayed, A.L. Shluger, On the microscopic structure of hole traps in pMOSFETs, Proc. Intl. Electron Devices Meeting (IEDM), 2014.