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Emerging CMOS Compatible Magnetic Memories and Logic

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***Abstract* —As scaling of electronic semiconductor devices - the main driving force behind an outstanding increase of computing power of modern electronic circuits - displays signs of saturation, the main focus of engineering research in microelectronics shifts towards finding new computing paradigms. The future solutions must be scalable and energy efficient while delivering high computational performance, superior to that of CMOS-based circuits. In order to benefit from the outstanding potential of highly advanced silicon processing technology, the emerging solutions must be CMOS compatible. Emerging nonvolatile memories, including magnetoresistive memories, satisfy the necessary requirements: Purely electrically addressable magnetoresistive random access memories yield all aforementioned conditions. They possess a simple structure, require fewer extra masks for fabrication, and offer endurance and speed superior to those of flash memory. Fast operation of magnetoresistive memories makes them a viable contender to static random access memory and flash memory for embedded applications in Systems on Chip. Having nonvolatile memory very close to CMOS removes the necessity of the energy-intensive data transfer from the main memory to the CPU and offers a prospect of data processing in the nonvolatile segment, where the same elements are used to store and to process the information. This opens perspectives for conceptually new low power and high-performance computing paradigms based on logic-in-memory and in-memory computing.**

***Index Terms*—Digital spintronics, spin-transfer torque (STT), spin-orbit torque (SOT), magnetoresistive random access memory (MRAM), in-memory computing**

I. Introduction

THE continuous miniaturization of metal-oxide-semiconductor field effect transistors is slowing down. Even though single devices with a gate length of a few nanometers were demonstrated [1], their control, reliability, fabrication costs, and the integration of several tens of billions of these devices will result in an unbearable hurdle. In addition, a growing consumption of stand-by power due to increased leakages and dynamic power due to slow V_{DD} scaling result in rapidly increasing heat generation.

An attractive path to mitigate the undesired trend of increasing power dissipation, especially at a stand-by mode, is to introduce nonvolatility in the circuits. Nonvolatility is the ability to retain the data, when the power supply is turned off. Introduction of nonvolatility enables standby power-free integrated circuits. Apart from stand-alone applications as well as critical program and data storage devices, nonvolatility is particularly promising for use in the main computer memory as it eliminates the need for data refreshment cycles in conventional CMOS-based dynamic random-access memory (DRAM) [2]. In addition, if the memory is embedded on chip, it removes one of the bottlenecks of the Von Neumann computing architecture, namely the lengthy and energy consuming procedure of data exchange between the memory and the CPU. However, in order to compete with traditional memories, including nonvolatile flash, emerging nonvolatile memories must offer fast switching time, high integration density supported by good scalability, long retention time, high endurance, and low power consumption. They must also possess a simple structure to reduce fabrication costs. An important requirement is that emerging memories must be compatible with CMOS technology to benefit from the advantages provided by the well-developed CMOS fabrication technology.

CMOS operation is intrinsically based on the electron charge. As the downscaling of charge-based CMOS is saturating, another intrinsic characteristic of the electron, the electron spin, attracts attention as a possible candidate for complementing or even replacing the charge degree of freedom in future microelectronic devices [3], [4], [5]. The electron spin is characterized by the two possible spin projections on a reference axis and therefore possesses the property necessary for digital information. Indeed, magnetic hard disk drives (HDD) employ the electron spin or, to be more precise, the magnetization orientation to store the data. However, HDDs require magnetic fields created in magnetic heads in order to read and write the information. As they are not operated by electric currents, they are not CMOS compatible. In order to create a purely electrically manipulated magnetic memory, an efficient coupling between the electric current or field and the magnetization must be achieved. The discovery of the giant magnetoresistance (GMR) effect facilitated a reliable, purely electrical read operation of the information encoded in the magnetization orientation [6], [7]. The emerging generation of storage devices with even higher density is based on the unique properties of magnetic tunnel junctions (MTJs), a sandwich of two ferromagnetic layers separated by a thin tunnel barrier. The tunneling current through the MTJ structure strongly depends on the relative orientation of the magnetization in the ferromagnetic contacts. The difference in the MTJ resistivity

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reaches a factor of seven [8] in structures with in-plane magnetization and a factor of three [9] in MTJs with the magnetizations perpendicular to the layers, at room temperature. An efficient way of converting the magnetization orientation into an electrical resistance allows using MTJs for data storage. As the typical resistance of an MTJ is similar to one of a MOSFET, no extra amplifiers are required for the converted signal. Thus, MTJ-based magnetoresistive random access memory (MRAM) is compatible with CMOS circuits.

II. Spin-Transfer Torque MRAM

Although a very fast magnetization switching induced by magnetic fields has been achieved, MRAM writing induced by a magnetic field is not fully compatible with scaling. The magnetic field is generated by an electric current passing through write lines next to the cell. For downscaling, the wires' cross section must be reduced, which makes higher current densities necessary to achieve the same field [10]. Therefore, a purely electrical way of MRAM information writing without magnetic field must be implemented.

The spin-transfer torque (STT) effect [11], [12] has been proven to be perfectly suited for purely electrical data writing. By passing the current through an MTJ, electrons become spin-polarized along the magnetization of the fixed layer. When they enter the free layer (FL), they become aligned with the magnetization of the free layer almost immediately. Since the total angular momentum is conserved, the change in the electron spin is transferred to the magnetization, which results in a torque acting on the FL magnetization. If the current is strong enough to overcome the damping, this torque causes magnetization switching. STT-MRAM is considered a perfect candidate for future universal memory applications. It is fast (5ns), possesses high endurance (10^{12}), and has a simple structure. It is compatible with CMOS technology and can be straightforwardly embedded in circuits [10]. It is particularly promising for stand-alone as well as for embedded applications as a replacement of conventional volatile CMOS-based and nonvolatile flash memory in Systems on Chip (SoC). For embedded applications, a successful implementation of 8Mb 1T-1MTJ STT-MRAM on a 28nm CMOS logic platform [13] was demonstrated. Recently, 128Mb embedded MRAM with 14ns write speed was reported [14]. An embedded MRAM solution compatible with 22FFL FinFET Intel's technology is available [15].

One critical aspect of the presently used STT-MRAM technology is a quite high switching current density, due to the fact that one has to overcome the energy barrier separating the two stable memory states. The barrier must be large - at least sixty times the thermal energy - to negate the errors due to undesired thermally agitated magnetization switching in big (1Gb) memory arrays at long (10 years) retention time. It turns out that in in-plane magnetized structures the barrier which must be overcome at STT switching is higher than the thermal barrier. After the current is applied, the magnetization starts precessing around the magnetic easy axis. At the same time, while precessing, the magnetization deviates from one of its stable states further and further due to the STT. Therefore, during the switching the magnetization gets out-of-plane. This demagnetization energy has to be expended in addition to the thermal barrier energy. As the system must be pushed over this rage barrier by STT, the reduction of the switching current and the current density is challenging.

Several plausible approaches to address these issues are currently pursued. They include the use of composite free recording layers [16], decoupling the write and read current paths as discussed later, controlling magnetization by voltage, and employing new materials with improved properties and characteristics. However, replacement of the in-plane magnetization orientation in MTJs with perpendicular magnetization is the path adopted by industry.

In perpendicular MTJs (p-MTJ), the magnetization is already out-of-plane. The large demagnetizing energy penalty one has to pay while writing an in-plane structure does not exist for switching perpendicular structures. p-MTJs with the thermal barrier equal to the switching barrier allow to reduce the switching current. In addition, p-MTJs are better suited for high-density memory. A critical technological step was the discovery of an interface-induced perpendicular anisotropy at the CoFeB/MgO interface [17] with thin perpendicularly magnetized CoFeB layers.

In order to further reduce the switching current density and, at the same time, to preserve the large thermal barrier, one has to reduce the Gilbert damping and increase the spin current polarization. An interface-induced p-MTJ structure with a composite MgO/CoFeB/Ta/CoFeB/MgO free layer with two MgO interfaces [18] allows boosting the thermal barrier, while reducing the Gilbert damping. To scale the diameter of the MTJ beyond 10nm, the use of shape anisotropy was suggested [19]. It has been shown that the thermal stability can be boosted for small diameters without sacrificing the tunneling magnetoresistance (TMR) and without any need for new materials, as FeB for the ferromagnetic free layer and MgO for the tunnel barrier were used.

A large TMR ratio is required for fast reliable reading in MRAM. In addition, the middle reference resistance to which the low and high resistance MTJ states are compared must be well separated from either of them. However, with downscaling it becomes increasingly difficult to control the bit-to-bit resistance. Resistance variation results in sacrificing the read error margin. Therefore, obtaining a large TMR is needed to continue scaling the devices down.

Advanced STT-MRAM is faster than flash memory and is suitable for last-level caches. However, STT-MRAM loses the power consumption competition to SRAM [20]. A new technological solution is thus required to use MRAM in higher level caches.

III. Spin-Orbit Torque MRAM

Among the newly discovered physical phenomena suitable for next-generation MRAM is the spin-orbit torque (SOT) assisted switching of a ferromagnetic layer at room temperature in heavy metal/ferromagnetic [21] or topological insulator/ferromagnetic [22], [23] bilayers. In SOT-MRAM cells the MTJ's free layer is grown on a material with a large spin Hall angle/SOT. The SOT is generated by passing the current through this material. The switching current is injected in-plane along the heavy metal/ferromagnetic bilayer. Although the current density is quite large, the current does not flow through the MTJ. Even then, the high value of the switching

current is still a problem, and its reduction is the pressing issue for SOT-MRAM development. Topological insulators (TIs) are promising materials for reducing the switching current as they are characterized by a large efficiency of charge to spin conversion. The electrical conductivity of TIs, however, is usually too low for power-efficient applications. Recently, BiSe [22] and BiSb [23] TIs were reported as suitable candidates for emerging SOT-MRAM. They possess a charge to spin conversion efficiency of 18.8 and 52, respectively, and large conductivities allowing the reduction of the switching current by two orders of magnitude as compared to tungsten-based SOT-MRAM.

Despite the progress in developing and prototyping SOT-MRAM, there is one important issue which has not been convincingly resolved so far. Namely, a static magnetic field is still required to guarantee deterministic SOT switching of a perpendicularly magnetized free layer. In SOT-MRAM prototypes on 300mm wafers an additional cobalt magnet was incorporated to provide such a field [24]. The approaches are based on cell mirror symmetry breaking [25] with respect to the plane formed by the normal vector to the free layer and the current direction. In this way, the two left and right in-plane magnetization orientations perpendicular to the current become non-equivalent, and the magnetization relaxes deterministically to the opposite stable states from these orientations. The symmetry can be perturbed by modifying the shape of the dielectric [26] or the free layer [27], by controlling the crystal symmetry of the metal layer [28], and by biasing the free layer via an exchange coupling to an antiferromagnet [29] or to an in-plane ferromagnet [30], [31], [32]. Interestingly, the latter experiments ignited the interest towards surprisingly little explored SOTs in ferromagnetic materials.

Approaches based on the breaking of the cell symmetry demand a considerable adaptation in the fabrication process and may compromise the large scale integration of memory cells. Recently, a magnetic field free switching was reported in a structure of stacked heavy metal lines with opposite Hall angles [33]. This finding is exciting as it is compatible with a CMOS fabrication process. Another promising approach is based on a purely electrical dynamic way to induce the required magnetic field by means of two orthogonal current pulses [34]. This demonstrates that SOT-induced switching is an area of active fundamental research promising novel exciting discoveries.

IV. Spin-based Logic

The introduction of nonvolatility in CMOS circuits reduces the power consumption by half, with an outstanding 90% reduction for specific logic-in-memory circuits [35]. Placing the actual computation into the nonvolatile domain results in a non-conventional in-memory computing architecture. Any two MTJ-based cells can perform a conditional switching of a target MTJ depending on the state of the source MTJ, an operation called material implication (IMP). IMP completed with the FALSE operation covers the whole space of all Boolean operations. A compact IMP-based full adder realization involving only six 1T-1MTJ cells and 27 subsequent FALSE and IMP operations can be realized [36]. Recently, a massively parallel NOT operation based on the IMP implementation was proposed [37].

Another option for non-volatile computing is to proceed along a more conventional path with memory and computing units separated. Both elements are implemented in the magnetic domain and are nonvolatile. The idea of combining MTJs with a common free layer enables the realization of a nonvolatile magnetic flip-flop [38]. The processing unit consists of an STT-based nonvolatile majority gate and nonvolatile magnetic flip-flops used as memory registers in a nonvolatile processing environment [38]. Recently, a substantial progress in fabricating such devices was reported [39].

The availability of high-capacity nonvolatile memory enables new logic-in-memory and computing-in-memory architectures for future artificial intelligence and cognitive computing. Nonvolatile MTJs are suitable for neural network realizations as they can be considered a current-driven programmable resistor, a memristor. MTJ-based neural networks featuring nonvolatile synapses allow for high-speed pattern recognition with a reduction in gate count of about 70% and a 99% improvement in speed as compared to their CMOS counterparts [35]. All-spin binary neuromorphic computing systems with probabilistic inference and online learning can enable a new generation of state-compressed and low-power computing platforms [40]. Neuromorphic computing is becoming a reality, with the first self-learning chips already in production.

V. Conclusion

We are witnessing the beginning of nonvolatile MRAM entering into the stand-alone and, especially, embedded memory market, as all major foundries announced the start of production of embedded STT-MRAM based on advanced silicon-on-insulator FinFET technology nodes. It will result in an exponential expansion of the MRAM market with a momentous impact on information storage and processing in the near future. In addition, a successful adoption of nonvolatility in microelectronic circuits and systems by developing various logic-in-memory and in-memory processing architectures promises a disruptive impact on cloud computing and edge applications by introducing new concepts in ultralow-power high-performance computing.

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