Anomalous Instabilities in CVD-MoS_2 FETs Suppressed by High-Quality Al_2O_3 Encapsulation

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Introduction: MoS_2 is a promising 2D semiconductor for next-generation nanoelectronics. Recent studies report MoS_2 FETs with near-ideal SS close to 60 mV/dec [1] and high I_{on}/I_{off} ratios [2] up to $\sim 10^{10}$. However, due to a large number of defects in the channel and gate insulator [3] these devices often display hysteresis [3, 4] and bias-temperature instabilities (BTI) of the I_D-V_G characteristics [3]. Thus, possible stability limitations of MoS_2 FETs have to be addressed prior to bringing them to the commercial market. Here we assess the application potential of single-layer (1L) MoS_2 FETs in digital electronics and thermally assisted memories [5] by studying the effect of Al_2O_3 encapsulation on their stability with respect to high temperatures, hysteresis and BTI.

Devices: Our devices are 1L MoS_2 FETs [2, 6] with the MoS_2 channel grown by CVD at 850°C directly on SiO_2(25 nm)/p^{++}-Si substrates [6]. After detailed measurements on bare devices (Fig. 1a), a high-quality 15 nm thick Al_2O_3 encapsulation layer (Fig. 1b) was grown by atomic layer deposition (ALD) at 300°C [2, 7]. By analyzing the variability of tens of encapsulated MoS_2 FETs (Fig. 1c), we classify them into Type I (~60 %) with excellent I_{on}/I_{off} ratios up to 10^{10} (Fig. 1d), Type II (~20 %) with I_{on}/I_{off} ratios of $10^6 - 10^7$ and Type III (~20 %) with poor performance.

Results and Discussions: In Fig. 2a we compare the I_D-V_G characteristics of three types of our MoS_2 FETs after Al_2O_3 encapsulation. Annealing of all bare devices at 300°C introduces a negative drift of V_{th} likely linked to the creation of S vacancies in MoS_2 by chemical reaction with residual H_2 [8, 9]. In Type I devices (Fig. 2b) this drift is completely suppressed by encapsulation which leads to record-high I_{on}/I_{off} ratios of 10^{10} and indicates the high quality of Al_2O_3. In Type II devices (Fig. 2c) the V_{th} drift is only partially compensated, which can be due to MoS_2 grain boundaries which catalyze the creation of S vacancies [10]. Finally, in Type III devices (Fig. 2d) encapsulation causes a positive V_{th} drift due to n-doping of MoS_2 by donor impurities which may be still locally present in Al_2O_3 [11].

In Fig. 3a we show the I_D-V_G characteristics of two bare MoS_2 FETs with similar hysteresis width ΔV_H versus reverse sweep time $1/t_{sw}$ dependences (Fig. 3b). At 25°C a small clockwise hysteresis due to charge trapping by oxide traps in SiO_2 is observed. At 165°C we see a switching of the hysteresis, which becomes counterclockwise near V_{th} and remains clockwise far above V_{th}. We speculate that this can be due to the interplay between the substitution of S vacanices by O^{-2} ions migrating from SiO_2 at negative V_G [12], and charge trapping by SiO_2 defects at positive V_G. This would be consistent with the presence of hysteresis switching only in bare MoS_2 FETs (Fig. 3c) and its complete suppression in Type I devices after Al_2O_3 encapsulation (Fig. 3d), which likely protects the MoS_2 channel from reaction-induced creation of S vacancies and also suppresses irreversible negative drift of V_{th}.

In Fig. 4a we show the I_D-V_G characteristics of a typical Type I and two Type II devices. A more negative V_{th} and a smaller I_{on} in Type II devices points towards an excess number of S vacancies [9] and suggests the presence of grain boundaries [10]. As a result, in Type II devices hysteresis switching at 165°C and irreversible negative drift of V_{th} are present also after Al_2O_3 encapsulation (Fig. 4b), which is in contrast to Type I devices (Fig. 4c). Furthermore, in devices with more negative V_{th} hysteresis switching is more pronounced (Fig. 4d) which can also suggest that the role of S vacancies is important. In contrast to bare MoS_2 FETs (Fig. 3b), in encapsulated Type II devices hysteresis switching starts only at slow sweeps. Thus, we suggest that creation of S vacancies near grain boundaries [10] in encapsulated Type II devices is a slow process as compared to reaction of S with residual H_2 [8] in bare devices.

We finally analyze negative BTI (NBTI) at 25°C on the same Type I device after 300°C annealing (Fig. 5) and after Al_2O_3 encapsulation (Fig. 6). In annealed bare channel devices we observe smaller NBTI drifts and fast over-recovery starting from $t_s = 100$ s. Thus we speculate that long stressing at -20 V is enough to activate migration of O^{-2} ions from SiO_2 [12] and subsequent substitution of S vacancies created by annealing already at 25°C. This takes place during the stress, which partially suppresses an NBTI shift of V_{th} caused by oxide defects, and also during recovery. The latter accelerates the recovery and finally makes V_{th} more positive than it was before the stress. After Al_2O_3 encapsulation (Fig. 6) creation of S vacancies in Type I devices is suppressed and thus we observe only a normal NBTI recovery related to SiO_2 defects, which is nicely consistent with the absense of hysteresis switching (Fig. 3d).

Conclusions: We studied the impact of Al_2O_3 encapsulation on the functionality and stability of 1L CVD-MoS_2 FETs. We found that bare channel devices exhibit thermally enhanced hysteresis switching which might be exploited for memory applications. Subsequent high-quality Al_2O_3 encapsulation suppresses this memory behavior and results in I_{on}/I_{off} ratios up to 10^{10}, low variability, and excellent thermal stability of the channel. Our results are relevant for the further development of both MoS_2-based thermally assisted memories and high-performance MoS_2 FETs.

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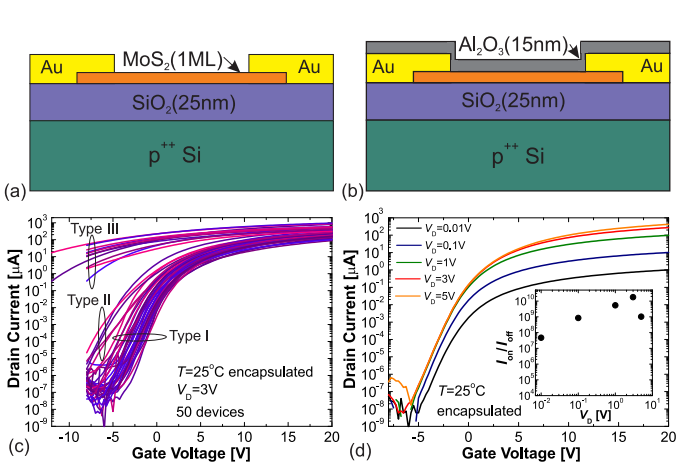

Fig. 1: Schematic layout of our MoS_2 FETs before (a) and after (b) encapsulation. (c) I_D-V_G characteristics of our 50 Al_2O_3 encapsulated MoS_2 FETs and one of the best (Type I) devices with on/off current ratios up to 10^{10} (d).

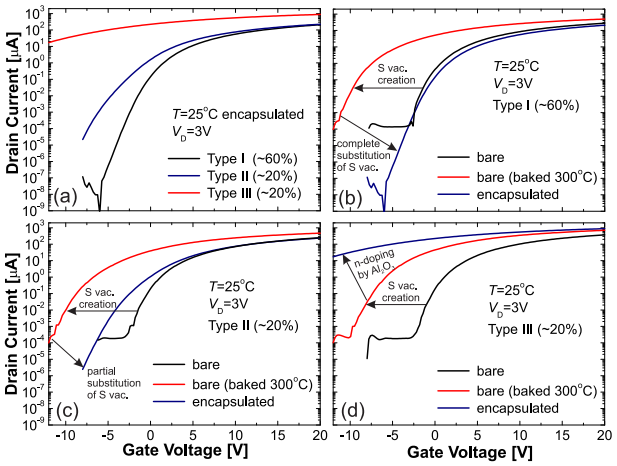

Fig. 2: (a) I_D-V_G characteristics of three typical MoS_2 FETs measured after Al_2O_3 encapsulation. Different impact of Al_2O_3 is observed for the devices of Type I (b), Type II (c) and Type III (d).

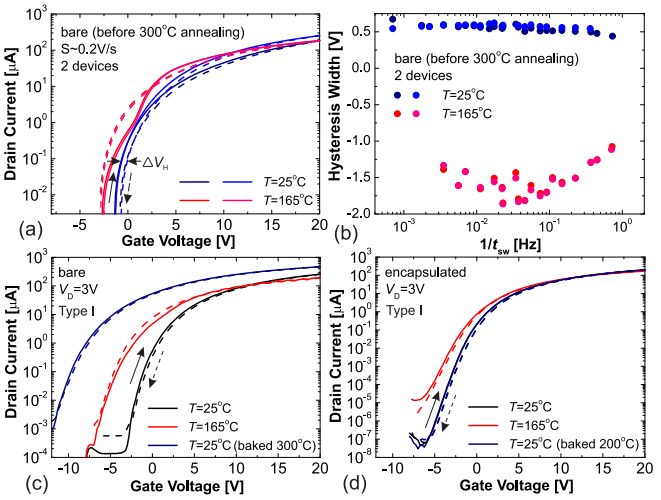

Fig. 3: (a) I_D-V_G characteristics of two nearly identical bare MoS_2 FETs at 25°C and 165°C. Hysteresis switching is observed at higher temperature. (b) The corresponding $\Delta V_H(1/t_{sw})$ dependences. I_D-V_G characteristics of the same Type I device before (c) and after (d) encapsulation measured at 25°C, at 165°C and at 25°C after annealing. High-quality Al_2O_3 enhances thermal stability of MoS_2 and suppresses hysteresis switching at 165°C.

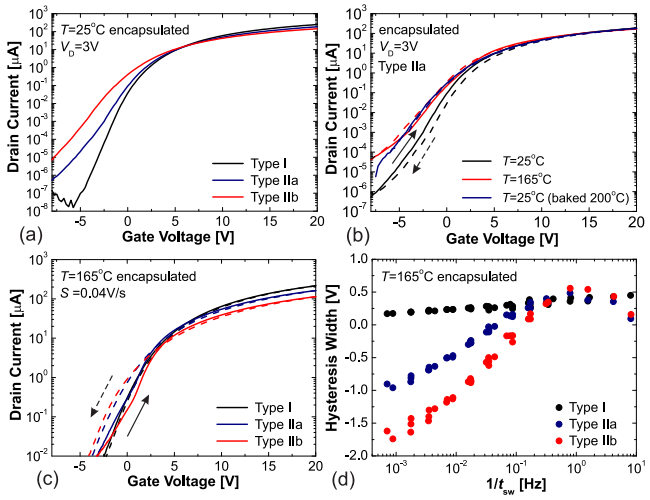

Fig. 4: (a) I_D-V_G characteristics of 3 encapsulated MoS_2 FETs. Type II devices with a more negative V_{th} exhibit an irreversible drift after annealing (b). (c) In contrast to Type I devices, in their Type II counterparts hysteresis switching is present for slow sweeps even after Al_2O_3 encapsulation. (d) The $\Delta V_H(1/t_{sw})$ dependences show that in the Type IIb device with the most negative V_{th} hysteresis switching is stronger.

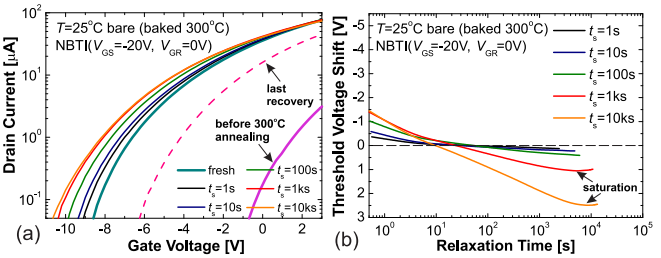

Fig. 5: (a) Transformation of the I_D-V_G characteristics of annealled bare channel MoS_2 FETs after subsequent NBTI stresses. (b) Strong over-recovery is observed, which could suggest that substitution of S vacancies by O^{-2} ions diffusing from SiO_2 is overlaid on charge trapping in SiO_2.

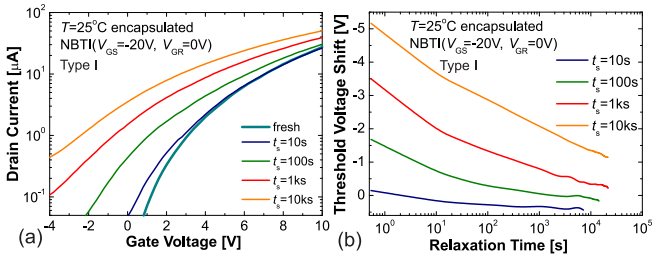

Fig. 6: (a) Transformation of the I_D-V_G characteristics of encapsulated MoS_2 FETs after subsequent NBTI stresses. (b) Normal NBTI recovery is consistent with charge trapping by oxide traps in SiO_2. The measurements were performed for the same device as in Fig. 5.