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Tunneling Effects in NH3 Annealed 4H-SiC Trench MOSFETs

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Abstract. The interface between the gate oxide and silicon carbide (SiC) has a strong influence on the performance and reliability of SiC MOSFETs and thus, requires special attention. In order to reduce charge trapping at the interface, post oxidation anneals (POAs) are conventionally applied. However, these anneals do not only influence the device performance, such as mobility and on-resistance, but also the gate oxide reliability. We study the oxide tunneling mechanisms of NH3 annealed 4H-SiC trench MOSFET test structures and compare them to devices which received a NO POA. We show that 3 different mechanisms, namely trap assisted tunneling (TAT), Fowler-Nordheim (FN) tunneling and charge trapping are found for NH3 annealed MOS structures whereas only FN-tunneling is observed in NO annealed devices.The tunneling barrier suggest a trap level with an effective activation energy of $382\,meV$ to enable TAT.

Introduction

Silicon carbide (SiC) is an attractive wide bandgap material for high power electronics because of its outstanding material properties [1]. However, the channel mobility of state-of-the-art silicon carbide (SiC) MOSFETs stays still below the reported limits of bulk SiC [2, 3]. In order to improve device performance, post oxidation annealing (POA) in various gas ambients is applied, e.g. nitric oxide (NO) or ammonia (NH3). At the moment, NO is the preferred annealing gas in industry because it offers a good balance between MOSFET performance and reliability [4, 5, 6]. Recent studies suggest that NH3 POA further improves the device performance and reduces charge trapping compared to POA in NO [7]. In this work we study the gate oxide reliability of NH3 annealed 4H-SiC trench MOSFET test structures by measuring the temperature and bias dependence of gate oxide tunneling. As we will show, NH3 annealed structures show a trap enhanced tunneling mechanism and Fowler-Nordheim (FN) tunneling whereas only the latter is observed in standard NO treated devices.

Experimental

N-channel trench MOSFET test structures were fabricated on commercial n-doped Si-face 4H-SiC substrates with an industrial process. The conductive channel only forms on one side of the trench along the a-plane ($(11\bar{2}0)$ crystal plane). The gate oxide was deposited by chemical vapor deposition (CVD) and the SiC/SiO2 interface annealed with either NO (time $t_1 > 100\,min$, temperature $T_1 > 1000°C$) or NH3 (t_1, $T_2 \approx T_1$). To validate our conclusions, we added data of MOSFETs which received N2 POA (t_1, T_1). According to [8], N2 POA does not passivate the interface with nitrogen. A cross-section of the studied devices can be found in [9].

In MOS devices with thicker oxides ($> 5\,nm$), as is the case for the studied test structures, FN-tunneling through a triangular barrier of the conduction band is the dominant tunneling mechanism at higher gate voltages [10]. The barrier height between SiC and SiO2 depends on the polytype and additionally on the crystal face [1]. For 4H-SiC Si-face/SiO2 interfaces (trench bottom), Kimoto and Cooper [1] report typical barrier heights of $2.7 - 2.8\,eV$, which equals the expected

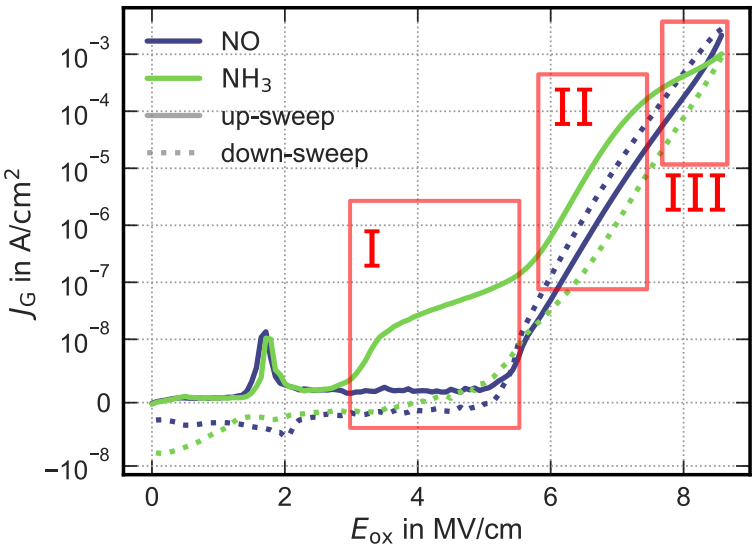

Fig. 1: Gate oxide tunneling characteristics for NO and NH3 annealed MOSFET. The tunneling current of the NH3 samples consists of three different regions whereas the NO samples only show FN tunneling.

SiC/SiO2 conduction band offset. According to [11], trapping may reduce this barrier. We measured standard $I_G(V_G)$-curves with $0\,MV/cm \leq E_{ox} \leq 8.5\,MV/cm$ at various temperatures in the range $100\,K \leq T \leq 473\,K$. Since the gate current notably changes with every sweep, a new device was used at every temperature. The measured data are compared to theoretical FN curves calculated with the textbook formula [10]

$$J = \frac{q^2 E_{ox}^2}{16\pi^2 \overline{h} \Phi_{ox}} \exp\left(\frac{-4\sqrt{2m^*}(q\Phi_{ox})^{3/2}}{3\overline{h}E_{ox}}\right) \tag{1}$$

where q is the elementary charge, E_{ox} the oxide electric field, Φ_{ox} the barrier height (expected to be 2.7-2.8 eV for SiC/SiO2[1]), m^* the effective electron mass (0.39 times the electron mass [12]) and $\overline{h}$ the reduced Planck constant. The barrier height of the tested devices was extracted from the measurements in the appropriate voltage range using the formula above and compared to the expected barrier from literature. Additionally, the maximum sweep voltage was varied to study gate current hysteresis related to trapping.

The temperature dependence of TAT was evaluated for an oxide electric field of $5\,MV/cm$ using an Arrhenius plot. From the slope of the resulting curve, the effective activation energy of a trap candidate is extracted.

Results and Discussion

Fig. 1 shows the gate current characteristics for the studied test structures. The NO sample shows gate oxide tunneling starting form $E_{ox} \gtrsim 5\,MV/cm$. This is in good agreement with literature values from [1] where tunneling is reported to start from 5.5-6 MV/cm for 4H-SiC (0001) and from 4.0-4.5 MV/cm on for 4H-SiC $(000\overline{1})$. The observed tunneling curve is in good agreement with the calculated FN characteristics (not shown). With approximately 2.7 eV, the extracted barrier height for NO is in good agreement with literature values of 2.7-2.8eV [1, 11]. Therefore, we conclude that FN tunneling is the dominant gate oxide tunneling mechanism in NO annealed trench MOSFETs. In contrast, the tunneling behavior of NH3 annealed devices can be divided into three different regions (Fig. 1). In the range 2.5-3 MV/cm to approximately 5.5 MV/cm (Fig. 1/region I) an increased gate

current is observed compared to NO reference samples. In region II (5.5-7 MV/cm) the tunneling current is comparable to FN tunneling in the NO samples. Region III (7-8MV/cm) shows a reduction of the slope of the gate current.

In order to determine the dominant tunneling mechanisms in region I and II, the temperature dependence was studied. As can be seen in Fig. 2, region I shows a strong temperature dependence for $T > 200\,K$ whereas it is significantly smaller in region II. Band-to-band tunneling is only weakly dependent on temperature whereas trap assisted tunneling [13] and the Poole Frenkel effect (PFE) [14] generally show a strong temperature dependence. In both cases, traps are involved in the tunneling effect. In order to distinguish between the two tunneling or leakage mechanisms, the Poole-Frenkel plot (PF plot) was studied (not shown). According to [14], the PFE should result in a straight line in PF plot. For the NH3 annealed sample this is not the case. Additionally, [15] reports that the PFE only plays a minor role in oxides with a wide band gap. Therefore, we assign region I to TAT rather than to the PFE and region II to FN tunneling. Additionally, region II can be well fitted with a calculated FN curve with a barrier height of approximately $2.8\,eV$. This is in excellent agreement with literature values cited above.

In order to determine the tunneling barrier for TAT, an Arrhenius plot was used, see Fig. 3. From the slope, an activation energy of $382 \pm 17\,meV$ was extracted. One possible trap candidate to cause this tunneling behavior might be the intrinsic electron trap in SiO2 described in [16]. This trap level is located approximately $3.2\,eV$ below the SiO2 conduction band minimum [16], which is $0.4\,eV$ below the 4H-SiC conduction band minimum. On the other hand, it is well known that NH3 POA leads to an increased amount of nitrogen (N) (cf. [8] for XPS results) and hydrogen (H) in the oxide compared to an anneal in NO only, which also need to be considered to enable TAT. Therefore, if either N or H were responsible for the observation, any kind of NH3 containing POA must show TAT. However, the tunneling behavior of MOSFETs which received a combined POA in NO followed by a subsequent NH3 POA (NO+NH3) (not shown) only show FN tunneling without any TAT-like behavior at room temperature [17], even though these samples also show nitrogen incorporated throughout the oxide [8]. Thus, N and H in the oxide are unlikely causes of TAT in the NH3 annealed devices. By comparing differently annealed MOSFETs, it is rather assumed that NO POA in any form (NO only or NO+NH3) might be able to at least partially anneal the responsible trap level so that TAT is not observed in these devices. To test if the intrinsic electron trap is indeed a suitable candidate to explain the tunneling

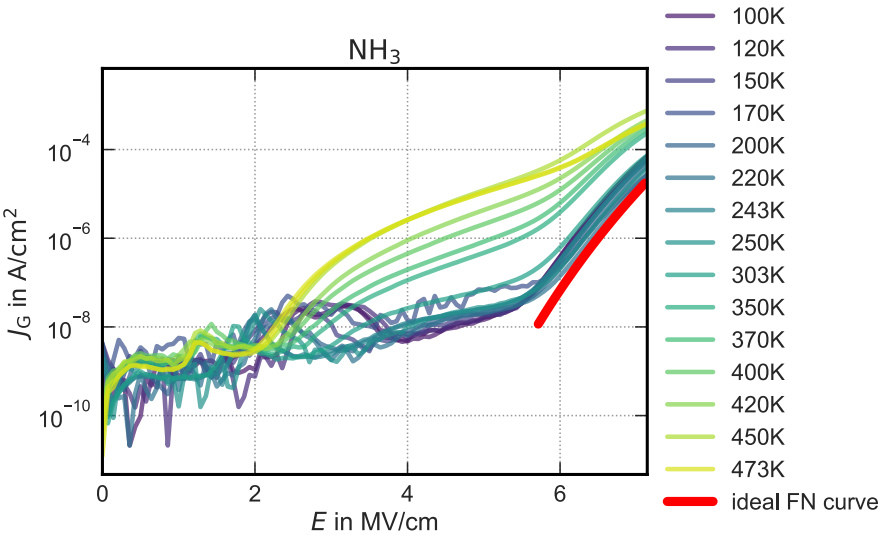

Fig. 2: Gate current density vs. oxide electric field measured at different temperatures (up-sweep). Between 2 MV/cm and 6 MV/cm a strong temperature dependence of the tunneling current is observed.

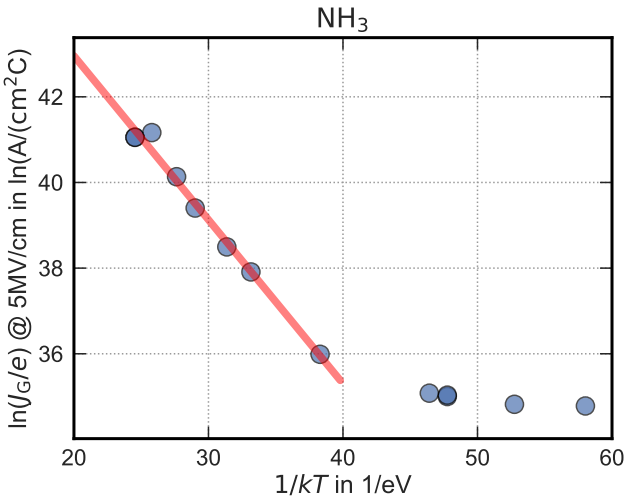

Fig. 3: Arrhenius plot of the TAT-current density at $5\,MV/cm$.The slope of the straight line gives an effective activation energy of $382 \pm 17\,meV$.

behavior, MOSFETs with an inert anneal in nitrogen (N2) were studied. N2 POA only densifies the oxide compared to a not annealed oxide and does not lead to any nitridation of the interface [8]. Therefore, the intrinsic electron trap should not have been passivated. However, it is not known to what amount a different oxide density might affect the trap energy. The tunneling behavior of these samples is shown in Fig. 4. A comparison with the ideal FN curve shows that the observed tunneling behavior cannot be explained with this tunneling mechanism. Even if considering an influence of fixed oxide charges by parallel shifting of the ideal FN curve along the x-axis, fitting of the measurement data is not possible. In contrast to NO and similar to NH3 annealed devices (cf. Fig. 5, $4.29\,MV$-curve), a hysteresis in the gate current is observed, indicating the involvement of charge trapping in the tunneling behavior. However, a less pronounced temperature dependence is observed than for the NH3 annealed samples. On one hand this could be interpreted as that no TAT is found, i.e. the intrinsic electron trap not being the cause for TAT. On the other hand, since N2 annealed samples suffer from fixed oxide charges and significantly more trapping than any of the other annealed test structures, it is possible that TAT might be covered by other trapping effects. This would still leave the intrinsic electron trap as a possible trap candidate. Therefore, the above model can neither be proved nor disproved without detailed simulation of the observed tunneling currents.

This theory is supported by tunneling measurements using MOSFETs with an inert anneal in nitrogen (N2). These samples show a similar tunneling behavior at different temperatures as is observed for the NH3 annealed structures (Fig. 4). However, the PF plot is not clear. It would be theoretically possible to fit the measured data to PFE with a certain error, however, the plausibility cannot be checked because the optical dielectric constants for this process is unknown. In region III, a ledge is observed in the tunneling current of NH3 annealed devices. Furthermore, an additional gate current hysteresis is seen in the initial V_G-sweep as soon as the maximum gate voltage enters this region. Fig. 5 shows the tunneling current for different $E_{ox,max}$. In the TAT region, hysteresis is observed because part of the tunneling charges are trapped at the trap level. In region II, the FN-region, no hysteresis is observed. As soon as region III is entered, an additional hysteresis component adds up, which means that charge carriers are trapped in the oxide. Therefore, the third region is attributed to charge trapping in the oxide. Since both, NH3 and NO+NH3 POA lead to this behavior and both processes lead to an increased amount of nitrogen throughout the whole SiO2 and not only at the interface as is the case for NO [8], we assume that trapping might take place at nitrogen sites. However, the impact of hydrogen from NH3 cannot be totally excluded in region III because the amount of hydrogen is difficult to determine.

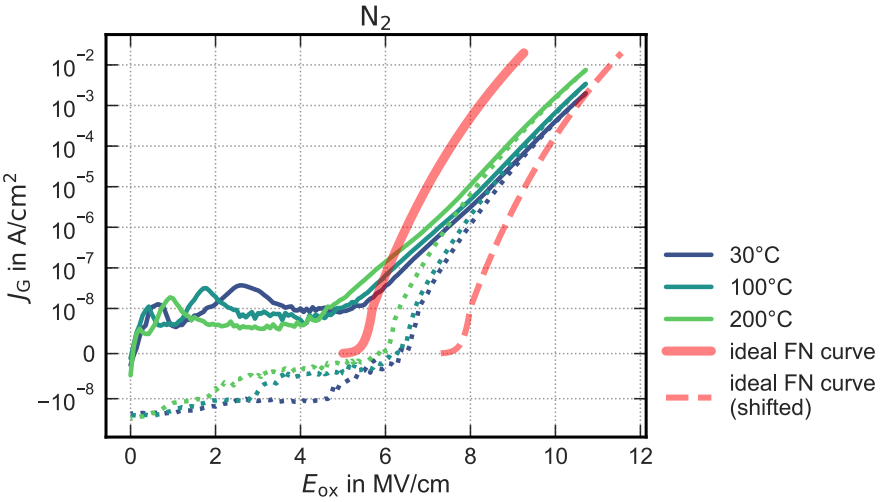

Fig. 4: Gate leakage current density vs. oxide electric field of an N2 annealed MOSFET measured at different temperatures. The observed behavior cannot be explained with FN tunneling, even not when considering fixed oxide charges (shifted FN curve). Furthermore, it shows only a relatively weak temperature dependence. Therefore, it is not clear if TAT takes place.

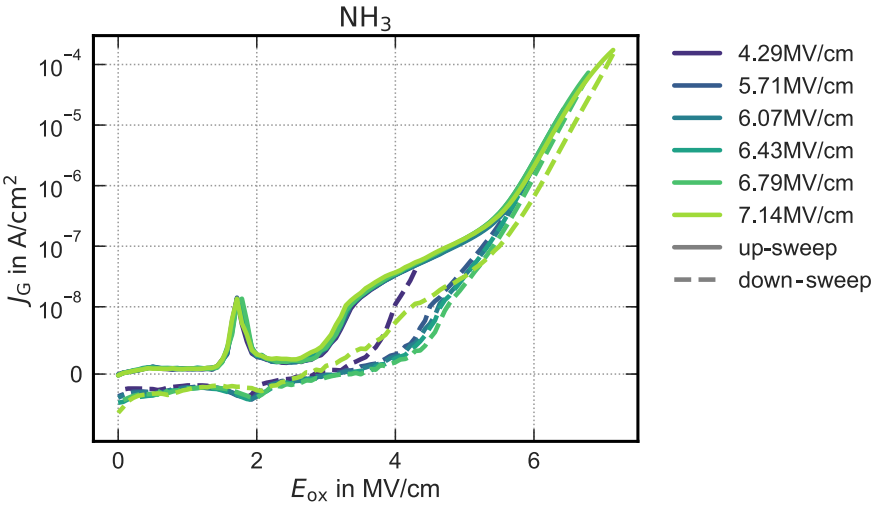

Fig. 5: Gate current hysteresis for several gate voltage sweeps with various end points. In the TAT-region, hysteresis is observed due to charges staying in the traps enabling tunneling. In the FN-region, no hysteresis is observed. As soon as region III is entered ($> 7\,MV/cm$), an additional hysteresis component adds up, indicating charge trapping in the oxide.

Summary

We found different gate oxide tunneling mechanisms for NH3 annealed MOSFETs compared to those with NO POA. The latter only show Fowler-Nordheim tunneling starting from approximately $5\,MV/cm$ whereas NH3 annealed MOSFETs show three different tunneling regions. The tunneling current in region I (2.5-5.5 MV/cm) is most likely caused by trap assisted tunneling. Region II (5.5-7 MV/cm) is assigned to FN tunneling and region III ($E_{ox} > 7\,MV/cm$) to charge trapping. For both processes, a FN tunneling barrier of 2.7-2.8 eV was determined which is in good agreement with literature. For TAT, a barrier of $382 \pm 17\,meV$ was extracted. By comparing the tunneling behavior of differently annealed MOSFETs to each other, it appears that NO POA might lead to a reduction of the trap density of this trap level or a change of activation energy whereas the NH3 anneal does not so that these samples show more TAT. Furthermore, we showed that NH3 containing POA leads to

trapping in the oxide for high electric fields. In contrast to region I, where N and H could be excluded as possible cause, trapping in region III might be related to the additional incorporation of nitrogen or hydrogen throughout the oxide in comparison to NO POA.

Acknowledgment

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