CV Stretch-Out Correction after Bias Temperature Stress: Work-function Dependence of Donor-/Acceptor-like Traps, Fixed Charges, and Fast States

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***Abstract*— Capacitance-voltage (CV) measurements on MOS structures are inherently difficult to analyze due to the so-called stretch-out, which results from defects becoming charged during the slow sweep and shifts the CV curve to lower or higher voltages without otherwise changing its shape. This stretch-out dramatically interferes which the actual target of the measurement, the extraction of the contribution of traps to the frequency-dependent small signal capacitance, potentially resulting in enormous spurious contributions to the extracted defect densities. Assuming that the slow states responsible for this stretch-out are normally distributed in energy, we suggest a simple correction algorithm and demonstrate its applicability using experimental NBTI/PBTI data on nMOS/pMOS devices to evaluate the creation of the various defect types as well as their work-function dependence.**

I. Introduction

There has been a decade-long discussion on the types of defects/charges created during BTI stress [1–8]. For their analysis, mostly changes in the threshold voltage, ΔV_{th}, have been recorded, which do not allow separating the various contributions suspected to be present. These components have been either grouped into fast and slow states [9], permanent and recoverable [10–12], or, interface and border traps [13]. Complementary measurements like charge pumping [14] and capacitance-voltage (CV) [15] have been used to determine the density of fast interface states, which are, however, difficult to correlate with ΔV_{th} data, since ΔV_{th} measurements are typically taken at a single readout bias with highly optimized readout-times in the microseconds range [16–18].

While CV measurements are inherently slow, they contain a massive amount of information on the involved defect levels throughout the silicon bandgap. Unfortunately, CV measurements are notoriously difficult to interpret due to the stretch-out caused by slow traps charging and discharging during the slow V_{G} sweep [19]. This stretch-out can dramatically interfere with the actual target of the measurement, the response of traps to the faster AC small signal applied at each V_{G}. In particular, it can result in spurious defect densities, which are often even negative, thereby completely obfuscating the true defect density of states.

Here we propose the *normal distribution stretch-out correction* (ND-SoC) algorithm to interpret CV data. We will show how the parameters of this broad distribution of slow states responsible for the stretch-out can be determined to allow the simultaneous estimation of the densities of slow donor-like states ($N_{\mathrm{s}}^{\mathrm{D}}$), slow acceptor-like states ($N_{\mathrm{s}}^{\mathrm{A}}$), fixed positive charges (N_{s}^{+}), as well as fast interface states (N_{f}).

As an application of the ND-SoC algorithm we investigate the response of pMOS/nMOS transistors to NBTI/PBTI stress and extract $N_{\mathrm{s}}^{\mathrm{D}}$, $N_{\mathrm{s}}^{\mathrm{A}}$, N_{s}^{+}, and N_{f} for different E_{ox} and CV frequencies to determine the dominant contributions. In addition, we vary the gate work-function. Since reliability is very sensitive to changes in the gate metals [20], we use devices with n^{++} and p^{++} poly-Si doping to vary the work-function. For simplicity, we investigate SiO_2 devices with $t_{\mathrm{ox}} = 5\,\mathrm{nm}$, as BTI in optimized high-κ devices has been shown to be dominated by the SiO_2/Si interfacial layer [21, 22], with the exception of an electron trapping contribution originating from many materials used as a high-κ layer which is particularly relevant for PBTI [23, 24].

For testing purposes, an implementation of the ND-SoC algorithm has been made available via a compact online tool [25] which contains various TCAD and experimental examples. In addition, pre- and post-stress CV curves can be uploaded and analyzed.

II. CV Stretch-Out Correction

Based on available knowledge of the bias temperature instability, we assume that the stretch-out can be approximately described by a broad normal distribution of slow states in energy. As a consequence of a gate-bias change to an MOS structure, the surface potential φ_{s} and the oxide field change. Thereby, the energetic distance of defects from the Fermi-level in the channel is modified, which determines which defects can change their occupancy and contribute to the CV signal. Consequently, to first order, a distribution of trap levels should be described as a function of the surface potential rather than the gate voltage V_{G}. Unfortunately, the surface potential is not easily accessible experimentally, particularly for more complicated structures with high-κ gate stacks or scaled insulators with poly silicon gates, as e.g. the voltage drop in the gate is not considered in the frequently employed Berglund method [26], which was derived for metal gates. For practical reasons, we will therefore approximate the energy dependence by a gate voltage dependence. Using V_{G} instead of φ_{s} is a reasonable approximation in depletion where $\varphi_{\mathrm{s}} \propto \gamma V_{\mathrm{G}}$ and the density can be easily corrected for $\gamma \neq 1$, while it leads to a distortion of the density-of-states when φ_{s} approaches the bandedges. Still, due to the "pinning" of the surface potential, CV measurements become insensitive towards the band-edges, reducing the importance of this error. We will

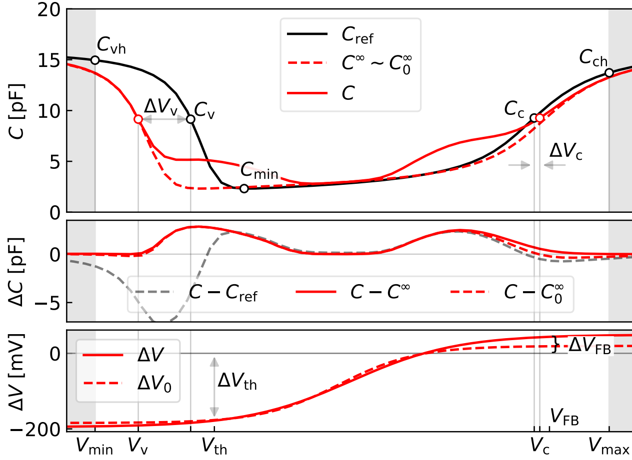

Fig. 1. ND-SoC algorithm to construct a stretched-out CV using a normally distributed density of slow traps. Shown are TCAD results for a pMOSFET with $t_{ox} = 5\,\text{nm}$ and $A = 50\,\mu\text{m} \times 50\,\mu\text{m}$, affected by a relatively high $N_{it} = 5\times10^{11}\,\text{cm}^{-3}$ and $N_{ot} = 10^{11}\,\text{cm}^{-3}$.

therefore approximate the stretch-out as

$$\Delta V(V_G, \mathbf{p}) = \Delta V_{min} + F(V_G, V_m, \sigma)(\Delta V_{max} - \Delta V_{min}) \ , \quad (1)$$

which depends on the set of parameters $\mathbf{p} = (V_m, \sigma, \Delta V_{min}, \Delta V_{max})$. Here, F is the CDF of the normal distribution with mean V_m and variance σ^2 while ΔV_{min} and ΔV_{max} describe the minimum and maximum values of ΔV. To avoid the awkward error-function in the CDF of the normal distribution, we approximate the normal distribution by a logistic distribution [27, 28], which for our purposes is indistinguishable from the normal distribution with respect to the experimental error and use

$$F(x, \mu, \sigma) \approx \left(1 + e^{\pi(\mu - x)/(\sigma\sqrt{3})}\right)^{-1} \ . \quad (2)$$

Using $\Delta V(V_G, \mathbf{p})$ from (1), the initial pre-stress measurement C_{ref} can be stretched to give C^∞, which is the hypothetical capacitance obtained for $f \to \infty$ where traps are too slow to follow the CV AC signal but are still fast enough to follow the slow CV sweep to change their occupancy and contribute to the stretch-out ΔV. In addition, the frequency dependence of the inversion capacitance is neglected in C^∞. C^∞ can then be used to calculate $\Delta C = C - C^\infty$ and $D_f = \Delta C/qA$, see Fig. 1, with q the elementary charge and A the device area. Empirically we found that

$$\mathbf{p}_0 = \begin{bmatrix} V_m \\ \sigma \\ \Delta V_{min} \\ \Delta V_{max} \end{bmatrix} = \begin{bmatrix} (V_c + V_v)/2 \\ (V_c - V_v)/5 \\ \Delta V_v \\ \Delta V_c \end{bmatrix} \quad (3)$$

is an excellent initial guess for $\mathbf{p}$ to stretch-out C_{ref}, with the meaning of the parameters explained in Fig. 1. Still, $\mathbf{p}_0$ can result in spurious negative D_f close to the band edges.

We now try to improve our stretch-out correction by minimizing the negative D_f while also minimizing the positive D_f, the optimum $\mathbf{p}$ can be found. For this, we split ΔC into its positive and negative parts, $\Delta C^+ = \max(\Delta C, 0)$ and $\Delta C^- = \max(-\Delta C, -\Delta C_{min}) + \Delta C_{min}$, with ΔC_{min} being on the order of the measurement resolution, e.g. 10 fF. Note that in equilibrium measurements, ΔC^- must be zero and any deviation from that is therefore a spurious result. By restricting ΔC^- to $\Delta C^- < -\Delta C_{min}$, the band $[-\Delta C_{min} \ldots 0]$ is removed from ΔC^- to account for measurement noise. We also restrict the calculation of the score function to the range V_{min} and V_{max}, see Fig. 1, which are obtained at

$$C_{ref}(V_{min}) = C_{min} + (\max(C_{ref}) - C_{min}) \times h_v \quad (4)$$
$$C_{ref}(V_{max}) = C_{min} + (\max(C_{ref}) - C_{min}) \times h_c \quad (5)$$

where a value of $h_v = h_c = 9/10$ proved to work well. During the optimization we consider the numerical integrals $I^+(\mathbf{p}) = \int \Delta C^+ dV_G$ and $I^-(\mathbf{p}) = \int \Delta C^- dV_G$ and aim to adjust $\mathbf{p}$ in such a way that I^- is minimized. The reason why we only minimize I^- rather than require it to be zero is that the noise present in experimental data would otherwise lead to spurious solutions with artificially blown-up D_f when the optimizer tries to enforce $I^- = 0$ at all costs. From all possible values of $\mathbf{p}$ which minimize I^- we chose that which also minimizes I^+. Mathematically, this is expressed via the score function

$$s = ||(I^+, 10^\alpha \times I^-)||_2 \ , \quad (6)$$

using an L_2 norm with a suitably chosen α which enforces the primary criterion of minimizing negative ΔC. Values in the range $[4 \ldots 10]$ have been found to work well, were a default value of 10 has been used for all the figures. Intuitively speaking, the ND-SoC algorithm "pushes" ΔC up barely enough to minimize I^- while also keeping I^+ small.

Assuming that during stress predominantly donor-like slow-states are created, ΔV_{min} and ΔV_{max} can be converted to defect densities:

	$\Delta V_{max} < 0$	$\Delta V_{max} > 0$
N_s^D	$-C'_{ox}(\Delta V_{max} - \Delta V_{min})/q$	$-C'_{ox}\Delta V_{min}/q$
N_s^A	0	$+C'_{ox}\Delta V_{max}/q$
N_s^+	$-C'_{ox}\Delta V_{max}/q$	0

where $C'_{ox} = t_{ox}/\varepsilon$ is the oxide capacitance per area. The concentration of fast states N_f is obtained by integration of D_f, that is, $N_f = \int D_f dV_G$. Note that the slow densities are *effective* densities and contain only the states that can contribute to the CV measurement and that their true distribution is certainly broader and larger. Also, only net charges enter the stretch-out ΔV, so if donor- and acceptor-like charges partially compensate each other, only their *net* contribution can be detected. As a consequence, the extracted densities must be considered lower bounds.

The ND-SoC algorithm is evaluated in Fig. 2 against TCAD data with fast P_b-centers [29] only and then in Fig. 3 for a combination of P_b-centers and slower oxide traps. For both data sets, the original D_f that entered the simulation can be accurately reconstructed, even though the stretch-out function is only a crude approximation of the P_b-center distribution. This is because D_f is very sensitive to the stretch-out only close to the band edges while the precise shape of ΔV does not matter that much in depletion where the CV curve is flat. In particular, the extracted D_f was found to be insensitive to whether a normal, logistic, or uniform distribution was used, provided that ΔV close to the band edges was correctly

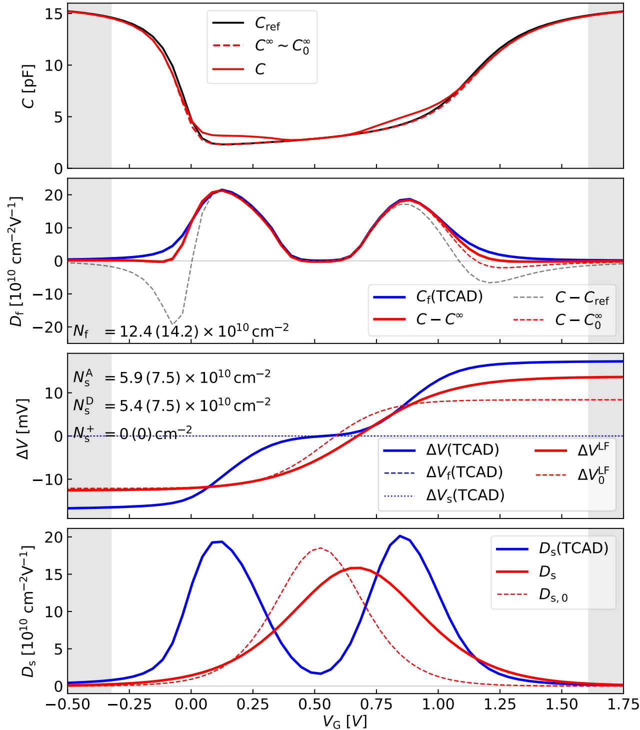

Fig. 2. Application of the ND-SoC algorithm to a pMOS obtained from TCAD simulations with a typical density of fast states associated with amphoteric P_b-centers with $N_f = 15 \times 10^{10}\,\mathrm{cm}^{-2}$. The extracted defect concentrations are given in the text, with TCAD reference values in parentheses. The top panel shows the initial (C_{ref}), the stretched-out initial (C_0^∞) and optimized curves (C^∞), as well as the TCAD-simulated impact of the defects on the CV curve (C), with the latter three being visually indistinguishable. This is the most challenging scenario since the single-hump stretch-out distribution has to capture both humps, which does not look overly satisfactory in the lower two panels. Still, the extracted $N_f = 12.9 \times 10^{10}\,\mathrm{cm}^{-2}$ agrees very well with the TCAD data.

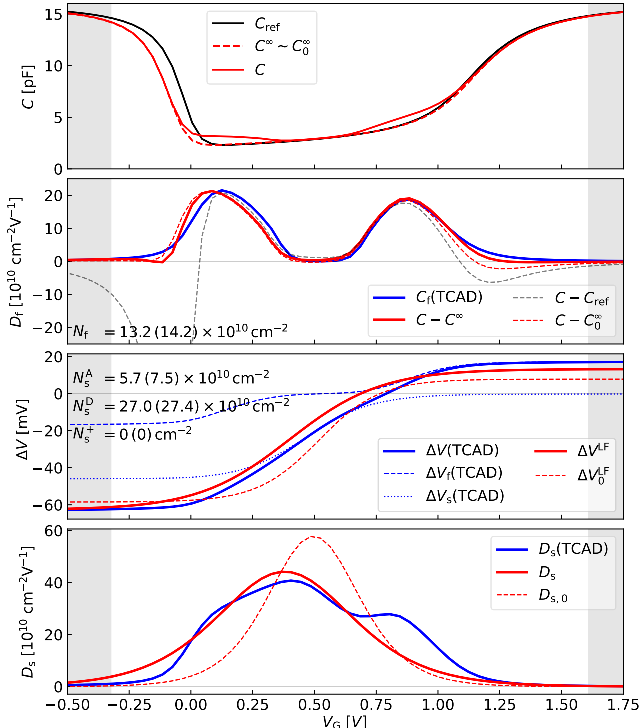

Fig. 3. Same as Fig. 2, but with added slow states with $N_s = 20 \times 10^{10}\,\mathrm{cm}^{-2}$. Again, good agreement is obtained for N_f, N_s^{D}, and N_s^{A}.

approximated (not shown). Additional TCAD examples are available in the ND-SoC online tool [25].

III. Experimental

The bias temperature instability has been under scrutiny for more than half a century [30, 31] and yet, still many open questions exist, in particular regarding which defect types are activated, created, or transformed during stress [7]. Based on the realization that the degradation recovers quickly once the stress voltage is removed [1], during the past 15 years a strong focus has been put on ultra-fast measurement schemes to capture this recoverable component [16–18]. While a lot of progress has been made, these ultra-fast measurement schemes have the disadvantage of sensing ΔV_{th} close to the valence band in pMOSFETs, while in nMOSFETs ΔV_{th} is sensed close to the conduction band. This has led to a lot of confusion whether BTI is relevant on SiO_2/Si nMOSFETs [32, 33], as there NBTI is typically small while PBTI appears completely negligible [4], and how the physical degradation mechanisms are related to what is known for pMOSFETs.

In the following, we will apply ND-SoC CV measurements to evaluate the relationship between NBTI/PBTI in nMOS/pMOSFETs. In addition, we use both n^{++} and p^{++} poly-Si gates since pMOSFETs typically employ p^{++} poly-Si gates while n^{++} gates are typically used for nMOSFETs. This implies that in pMOSFETs the Fermi-level at the gate side will be close to the valence band while it will be close to the conduction band in nMOSFETs. Due to the typically employed high doping of the poly-Si gate, the Fermi-level will remain virtually pinned for all V_G, as implied in Fig. 4.

As NBTI has been shown to depend on the oxide field and the carrier concentrations inside the channel [4], we carefully determine the required gate voltages to result in the same E_{ox} for all transistor types to obtain comparable stress and recovery conditions. The rationale here is that at the same E_{ox}, the carrier concentrations inside the channel will also be the same for all transistor types. As a consequence, at least to first order, similar degradation should be expected. Also, if the degradation is controlled by the channel, as is assumed in many BTI models, no impact of the work function is to be expected, provided V_G is adjusted accordingly to keep E_{ox} constant.

To avoid additional complexities caused by differences in the pMOS/nMOS device designs, we investigate plain SiO_2 capacitors with injection rings to be able to record the inversion response. By using relatively thick SiO_2, we minimize distortions caused by gate leakage currents. The capacitors were fabricated in a standard gate first flow and received a junction/poly dopant activation step prior to the forming gas anneal (FGA). Note that other than a conventional FGA, the capacitors were not particularly optimized for BTI.

Initial CV measurements were taken on all devices and were used to calibrate TCAD models. Based on the TCAD models, the required stress voltages for $E_{\mathrm{ox}} = \pm 6\,\mathrm{MV/cm}$ and $\pm 7.5\,\mathrm{MV/cm}$ were determined, while the recovery voltages were determined to give E_F at midgap. The resulting *active energy regions* (AERs), which are the regions of the oxide

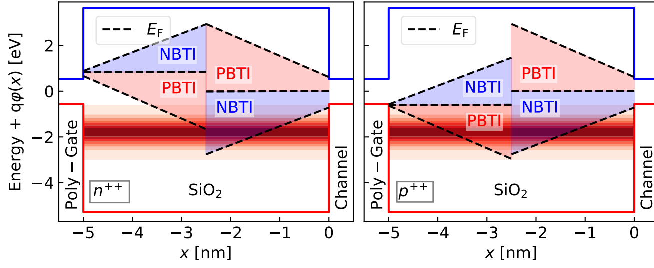

Fig. 4. Active energy regions are the same for nMOS and pMOS, but different for n^{++} (**left**) and p^{++} poly-Si gates (**right**). E_F is shown at midgap and $\pm 7.5\,\mathrm{MV/cm}$. Shown in red is also a guess for a typical donor-like defect band [24, 34].

where traps can change their occupancy by interacting with the channel or the gate, are shown in Fig. 4. Note that the AERs are identical for nMOS and pMOS but depend on the poly-Si doping, which basically pins E_F at the gate side to either the conduction or valence bands. The devices were stressed at the desired E_ox for 10 ks and recovered at midgap for 10 ks ($T = 125°\mathrm{C}$), each phase interrupted 9 times for multi-frequency CV measurements. With these slow measurements (about 9 min delay each), our results relate mostly to the slowly recoverable ("permanent") degradation.

IV. Results

The N_s^D, N_s^A, N_s^+, and N_f were extracted using the methodology above for different E_ox and CV frequencies and are shown in Fig. 5. For all channel/poly doping combinations, degradation is dominated by slow donor-like states, N_s^D, followed by fast states N_f and in some case acceptor-like traps N_s^A. We found that NBTI in our samples is insensitive to the gate Fermi-level while PBTI is extremely sensitive, up to a point that PBTI can be nearly completely eliminated. In more detail, we observe the following:

- **pMOS/NBTI** results predominantly in slow donor-like traps N_s^D and only little fixed positive charges N_s^+, meaning that ΔV_th is strongly readout-voltage dependent [35, 36] and ΔV_FB is very small. In addition, fast states are created with $N_\mathrm{f}(4\,\mathrm{kHz}) \approx N_\mathrm{s}^\mathrm{D}/3$ at $7.5\,\mathrm{MV/cm}$ and $N_\mathrm{s}^\mathrm{D}/2$ at $6\,\mathrm{MV/cm}$, which decreases by 50% at 100 kHz. This clearly suggests that N_f consists of at least two different kinds of traps, with a dominant contribution of oxide traps [7]. This is also supported by the correlation between N_f and N_s^D, which is excellent during stress but partially breaks down during recovery, see Fig. 6. Degradation seems to be controlled by the *channel* Fermi-level $E_\mathrm{F,channel}$, as there is little impact of the gate Fermi-level, $E_\mathrm{F,gate}$.
- **nMOS/NBTI** is fairly similar to pMOS/NBTI, with a somewhat larger number of N_s^D, N_s^A, and N_f created. Whether the difference in magnitude is a consequence of small inaccuracies in the TCAD simulations used to determine V_G to achieve constant E_ox or of a more fundamental nature remains to be clarified. The main difference from the application point of view is that ΔV_th is measured close to the conduction band in nMOSFETs,

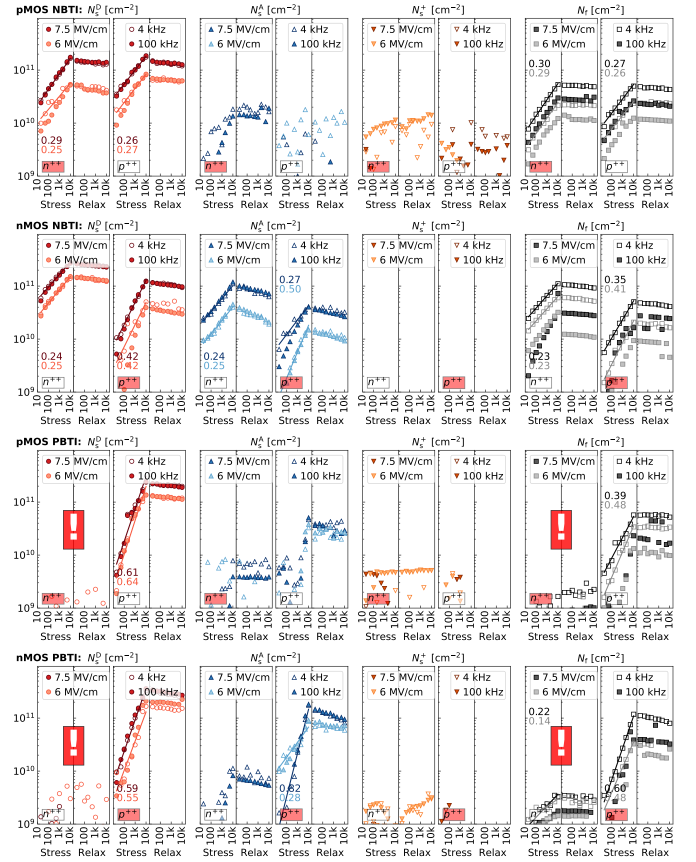

Fig. 5. Extracted slow donor states (N_s^D), acceptor states (N_s^A), fixed charges (N_s^+), and fast states (N_f) for the various combinations of nMOS/pMOS, NBTI/PBTI, and n^{++} and p^{++} poly-Si gates (the non-standard poly-gate dopings are marked with red labels). Open symbols are at 4 kHz, closed symbols at 100 kHz, darker colors at $7.5\,\mathrm{MV/cm}$, brighter colors at $6\,\mathrm{MV/cm}$. BTI creates mostly donor-like slow states, a small amount of fixed positive charges, and some acceptor-like states and fast states. Only the fast states N_f show a dependence on the CV frequency. To first-order, at the same E_ox, BTI responses should be (roughly) the same for channel-controlled degradation. Dramatic deviations are marked by red exclamation marks: during PBTI, in both n- and pMOS, the creation of N_s^D and N_f is clearly controlled by the gate Fermi-level.

where only a small fraction of N_s^D is positively charged and thus able to contribute to the stretch-out ΔV. As a consequence, the measured $\Delta V_\mathrm{th} = \Delta V(V_\mathrm{th})$ is dominated by N_s^A and N_f and therefore significantly smaller than for pMOS/NBTI, despite $N_\mathrm{s,nMOS}^\mathrm{D} \approx N_\mathrm{s,pMOS}^\mathrm{D}$ ($\Delta V_\mathrm{FB,nMOS} \approx \Delta V_\mathrm{th,pMOS}$). One noteworthy difference is that the correlation between N_f and N_s^D is maintained during both stress and recovery, indicating the existence of a dominant defect type, see Fig. 6. The observed D_it profiles are also fairly consistent with pMOS/NBTI, see Fig. 7.

- **pMOS/PBTI** strongly depends on $E_\mathrm{F,gate}$: For $E_\mathrm{F,gate}$ close to the conduction band, virtually no degradation is observed. On the other hand, for the typically used p^{++} poly-Si/pMOS devices, $E_\mathrm{F,gate}$ will be close to the valence band, and a very large degradation is observed with power-law exponents larger than those typically seen for NBTI, consistent with previous observations [37]. Again, degradation is then dominated by N_s^D, followed by N_s^A and N_f.

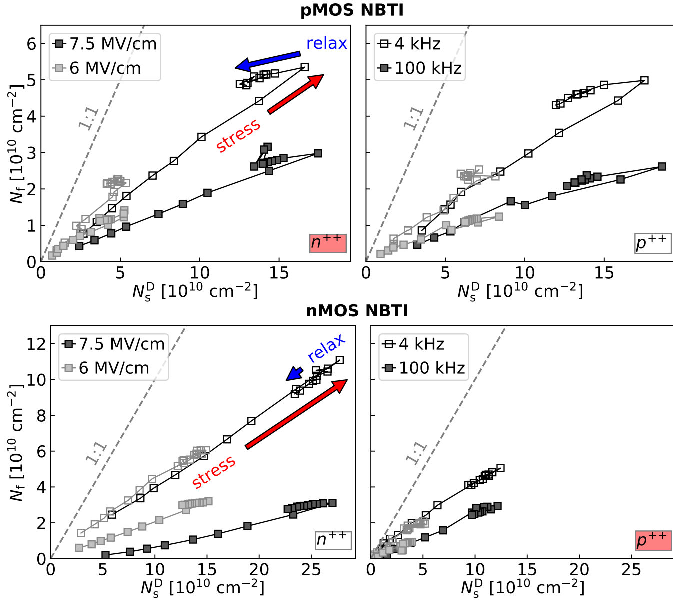

Fig. 6. Correlation between fast and slow donor states, N_f and N_s^D for NBTI in pMOS/nMOS (Same colors/symbols as in Fig. 5). The correlation is excellent during stress, while during pMOS recovery some of the correlation is lost at 4 kHz (open symbols), indicating the presence of two different trap types.

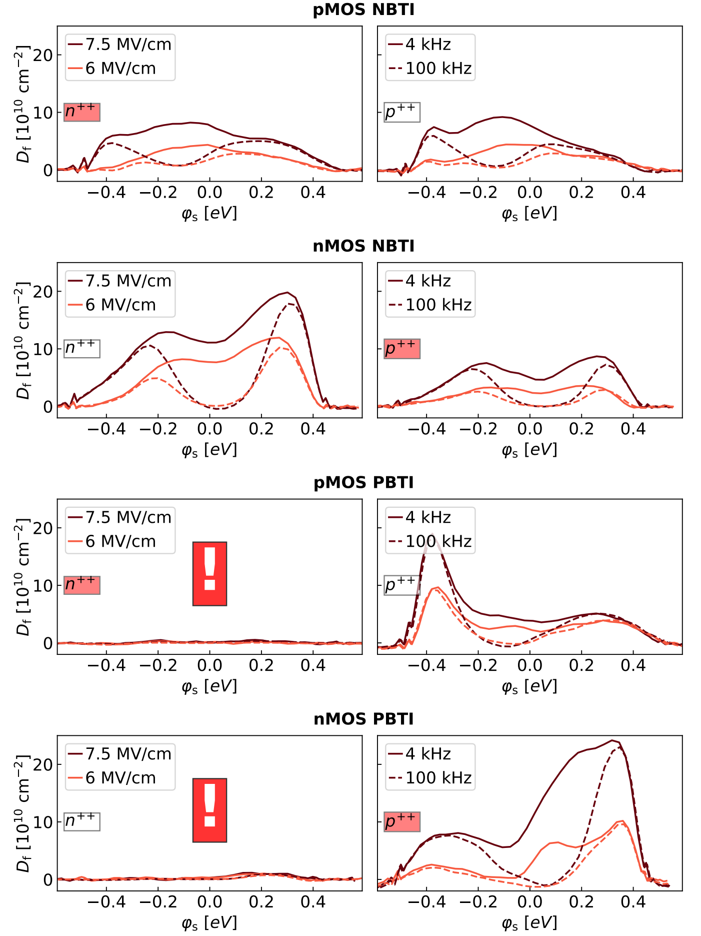

Fig. 7. Extracted density of fast states for the various combinations of channel and poly-gate doping for two E_ox (dark is 7.5 MV/cm, brighter 6 MV/cm) and two CV frequencies (solid is 4 kHz, dashed 100 kHz). While the NBTI profiles show some similarity, the absence of degradation for PBTI on n^{++} poly-Si gates is striking. Also, the PBTI profiles appear flipped for n^{++} and p^{++} poly-Si gates.

- **nMOS/PBTI** is again very similar to pMOS/PBTI, showing the same asymmetry with respect to $E_\mathrm{F,gate}$. For the typically used n^{++} poly-Si/nMOS devices, virtually no degradation is observed, consistent with previous observations [4]. Quite intriguingly, although similar in magnitude, the observed D_it profiles between nMOS and pMOS are much more different than those observed NBTI, see Fig. 7.

V. Discussion & Conclusions

We have suggested a normal distribution stretch-out correction (ND-SoC) algorithm, and applied it to consistently investigate the creation of slow donor- and acceptor-like defects, fixed positive charges, and fast states during bias temperature stress. We investigated the hypothesis that BTI degradation is the response of the same defects to different active energy regions (AERs) inside the oxide. These AERs at the channel side are determined by the difference of E_ox during stress and recovery, which was chosen approximately identical for nMOS and pMOSFETs for n^{++} and p^{++} poly-Si gate doping. As a consequence, to first-order, the NBTI response is similar for nMOS/pMOS independently of $E_\mathrm{F,gate}$ and thus appears to be controlled by the channel. PBTI, on the other hand, is very sensitive to $E_\mathrm{F,gate}$ and can be dramatically reduced by choosing $E_\mathrm{F,gate}$ close to E_c, which corresponds to the standard nMOS case.

Our results demonstrate that as long as the same $E_\mathrm{F,channel}$ and $E_\mathrm{F,gate}$ are guaranteed during stress and recovery, nMOS and pMOS device degradation is of the same order of magnitude and that previously observed differences [4] were primarily caused by different work-functions and monitoring of the Fermi-level dependent ΔV_th rather than the underlying responsible defects. Still, subtle differences exist, e.g. the partially lost correlation between N_f and N_s^D during recovery in the nMOS/NBTI case (independently of $E_\mathrm{F,gate}$), the different D_f profiles observed after NBTI, and most notably, the flipped D_it profiles observed for PBTI, all of which will require further investigation.

Acknowledgments

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References

[1] S. Rangan, N. Mielke, and E. Yeh, “Universal Recovery Behavior of Negative Bias Temperature Instability,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2003, pp. 341–344.

[2] M.-F. Li, G. Chen, C. Shen, X. Wang, H. Yu, Y.-C. Yeo, and D. Kwong, “Dynamic Bias-Temperature Instability in Ultrathin SiO_2 and HfO_2 Metal-Oxide-Semiconductor Field Effect Transistors and Its Impact on Device Lifetime,” *Jap.J.Appl.Phys.*, vol. 43, no. 11B, pp. 7807–7814, 2004.

[3] M. Houssa, M. Aoulaiche, J. Autran, C. Parthasarathy, N. Revil, and E. Vincent, “Modeling Negative Bias Temperature Instabilities in Hole Channel Metal-Oxide-Semiconductor Field Effect Transistors with Ultrathin Gate Oxide Layers,” *J.Appl.Phys.*, vol. 95, no. 5, pp. 2786–2791, 2004.

[4] V. Huard, M. Denais, and C. Parthasarathy, “NBTI Degradation: From Physical Mechanisms to Modelling,” *Microelectronics Reliability*, vol. 46, no. 1, pp. 1–23, 2006.

[5] S. Mahapatra, M. Alam, P. Kumar, T. Dalei, and D. Saha, “Mechanism of Negative Bias Temperature Instability in CMOS Devices: Degradation, Recovery and Impact of Nitrogen,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2004, pp. 105–108.

[6] M. Duan, J. Zhang, Z. Ji, W. Zhang, B. Kaczer, S. De Gendt, and G. Groeseneken, “Defect Loss: A New Concept for Reliability of MOSFETs,” *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 480–482, 2012.

[7] T. Grasser, B. Stampfer, M. Waltl, G. Rzepa, K. Rupp, F. Schanovsky, G. Pobegen, K. Puschkarsky, H. Reisinger, B. O’Sullivan, and B. Kaczer, “Characterization and Physical Modeling of the Temporal Evolution of Near-Interfacial States Resulting from NBTI/PBTI Stress in nMOS/pMOS Transistors,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, Apr. 2018, pp. 2A.2.1–2A.2.10.

[8] J. Stathis, S. Mahapatra, and T. Grasser, “Controversial Issues in Negative Bias Temperature Instability,” *Microelectronics Reliability*, vol. 81, pp. 244–251, 2018.

[9] C. Shen, M.-F. Li, X. Wang, H. Yu, Y. Feng, A.-L. Lim, Y. Yeo, D. Chan, and D. Kwong, “Negative U Traps in HfO_2 Gate Dielectrics and Frequency Dependence of Dynamic BTI in MOSFETs,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2004, pp. 733–736.

[10] A. Haggag, G. Anderson, S. Parihar, D. Burnett, G. Abeln, J. Higman, and M. Moosa, “Understanding SRAM High-Temperature-Operating-Life NBTI: Statistics and Permanent vs Recoverable Damage,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2007, pp. 452–456.

[11] T. Aichinger, S. Puchner, M. Nelhiebel, T. Grasser, and H. Hutter, “Impact of Hydrogen on Recoverable and Permanent Damage following Negative Bias Temperature Stress,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2010, pp. 1063–1068.

[12] T. Grasser, M. Waltl, Y. Wimmer, W. Goes, R. Kosik, G. Rzepa, H. Reisinger, G. Pobegen, A. El-Sayed, A. Shluger, and B. Kaczer, “Gate-Sided Hydrogen Release as the Origin of “Permanent” NBTI Degradation: From Single Defects to Lifetimes,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, Dec. 2015.

[13] D. Fleetwood, ““Border Traps” in MOS Devices,” *IEEE Trans.Nucl.Sci.*, vol. 39, no. 2, pp. 269–271, Apr 1992.

[14] G. Groeseneken, H. Maes, N. Beltran, and R. de Keersmaecker, “A reliable approach to charge-pumping measurements in MOS transistors,” *IEEE Trans.Electron Devices*, vol. 31, no. 1, pp. 42–53, 1984.

[15] E. Nicollian and J. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.

[16] H. Reisinger, O. Blank, W. Heinrigs, A. Mühlhoff, W. Gustin, and C. Schlünder, “Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultra Fast V_{th}-Measurements,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2006, pp. 448–453.

[17] A. Islam, E. N. Kumar, H. Das, S. Purawat, V. Maheta, H. Aono, E. Murakami, S. Mahapatra, and M. Alam, “Theory and Practice of On-the-fly and Ultra-fast V_T Measurements for NBTI Degradation: Challenges and Opportunities,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2007, pp. 1–4.

[18] G. Du, D. Ang, Y. Hu, and S. W. C. Ng, “Physical Framework for NBTI: Insight from Ultra-Fast Switching Measurement of NBTI Recovery,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2008, pp. 735–736.

[19] J. R. Brews, “Correcting Interface-State Errors in MOS Doping Profile Determinations,” *Journal of Applied Physics*, vol. 44, no. 7, pp. 3228–3231, July 1973. [Online]. Available: https://doi.org/10.1063/1.1662738

[20] P. Srinivasan, R. Ranjan, S. Cimino, A. Zainuddin, B. Kannan, L. Pantisano, I. Mahmud, G. Dilliway, and T. Nigam, “Understanding gate metal work function (mWF) impact on device reliability — A holistic approach,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, Mar. 2018.

[21] S. Pae, M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, M. Hattendorf, J. Hicks, J. Kavalieros, K. Kuhn, M. Kuhn, J. Maiz, M. Metz, K. Mistry, C. Prasad, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, J. Thomas, C. Wiegand, and J. Wiedemer, “BTI Reliability of 45 nm High-K + Metal-Gate Process Technology,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*. IEEE, Apr. 2008.

[22] S. Novak, C. Parker, D. Becher, M. Liu, M. Agostinelli, M. Chahal, P. Packan, P. Nayak, S. Ramey, and S. Natarajan, “Transistor Aging and Reliability in 14nm Tri-Gate Technology,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2015, pp. 2F.2.1–2F.2.5.

[23] L. Vandelli, L. Larcher, D. Veksler, A. Padovani, G. Bersuker, and K. Matthews, “A Charge-Trapping Model for the Fast Component of Positive Bias Temperature Instability (PBTI) in High-κ Gate-Stacks,” *IEEE Trans.Electron Devices*, vol. 61, no. 7, pp. 2287–2293, July 2014. [Online]. Available: https://doi.org/10.1109/ted.2014.2323085

[24] G. Rzepa, J. Franco, B. O’Sullivan, A. Subirats, M. Simicic, G. Hellings, P. Weckx, M. Jech, T. Knobloch, M. Waltl, P. Roussel, D. Linten, B. Kaczer, and T. Grasser, “Comphy — A Compact-Physics Framework for Unified Modeling of BTI,” *Microelectronics Reliability*, vol. 85, pp. 49–65, 2018.

[25] https://cv.iue.tuwien.ac.at, 2020.

[26] C. Berglund, “Surface States at Steam-Grown Silicon-Silicon Dioxide Interfaces,” *IEEE Trans.Electron Devices*, vol. ED-13, no. 10, pp. 701–705, Oct. 1966. [Online]. Available: https://doi.org/10.1109/ted.1966.15827

[27] A. Haggag, W. McMahon, K. Hess, K. Cheng, J. Lee, and J. Lyding, “High-Performance Chip Reliability from Short-Time-Tests,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2001, pp. 271–279.

[28] T. Grasser, “The Capture/Emission Time Map Approach to the Bias Temperature Instability,” in *Bias Temperature Instability for Devices and Circuits*, T. Grasser, Ed. Springer, New York, 2014, pp. 447–484.

[29] L. Ragnarsson and P. Lundgren, “Electrical Characterization of P_b Centers in (100)Si/SiO_2 Structures: The Influence of Surface Potential on Passivation During Post Metallization Anneal,” *J.Appl.Phys.*, vol. 88, no. 2, pp. 938–942, 2000.

[30] Y. Miura and Y. Matukura, “Investigation of Silicon-Silicon Dioxide Interface Using MOS Structure,” *Jap.J.Appl.Phys.*, vol. 5, p. 180, 1966.

[31] D. Schroder and J. Babcock, “Negative Bias Temperature Instability: Road to Cross in Deep Submicron Silicon Semiconductor Manufacturing,” *J.Appl.Phys.*, vol. 94, no. 1, pp. 1–18, 2003.

[32] T. Aichinger, M. Nelhiebel, and T. Grasser, “A Combined Study of p- and n-Channel MOS Devices to Investigate the Energetic Distribution of Oxide Traps after NBTI,” *IEEE Trans.Electron Devices*, vol. 56, no. 12, pp. 3018–3026, 2009.

[33] G. Pobegen, T. Aichinger, T. Grasser, and M. Nelhiebel, “Impact of Gate Poly Doping and Oxide Thickness on the N- and PBTI in MOSFETs,” *Microelectronics Reliability*, vol. 51, pp. 1530–1534, 2011.

[34] W. Goes, Y. Wimmer, A.-M. El-Sayed, G. Rzepa, M. Jech, A. Shluger, and T. Grasser, “Identification of Oxide Defects in Semiconductor Devices: A Systematic Approach Linking DFT to Rate Equations and Experimental Evidence,” *Microelectronics Reliability*, vol. 82, pp. 1–35, 2018.

[35] J. Zhang, Z. Ji, M. Chang, B. Kaczer, and G. Groeseneken, “Real V_{th} Instability of pMOSFETs Under Practical Operation Conditions,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2007, pp. 817–820.

[36] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, “A Two-Stage Model for Negative Bias Temperature Instability,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2009, pp. 33–44.

[37] K. Rott, H. Reisinger, S. Aresu, C. Schlünder, K. Kölpin, W. Gustin, and T. Grasser, “New Insights on the PBTI Phenomena in SiON pMOSFETs,” *Microelectronics Reliability*, vol. 52, no. 9–10, pp. 1891–1894, 2012.