Impact of High-Aspect-Ratio Etching Damage on Selective Epitaxial Silicon Growth in 3D NAND Flash Memory

Tobias Reiter, Xaver Klemenschits, and Lado Filipovic
Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Vienna, Austria

***Abstract*—A physical process model for inductive plasma dry etching is presented and applied to simulate vertical channel hole etching, a critical fabrication step in modern 3D NAND flash memory. A specialized advection algorithm is subsequently applied to simulate the selective epitaxial growth (SEG) of silicon on the bottom source line. The induced etching damage on the bottom silicon substrate, which is included in the etching model, is shown to heavily reduce the quality of the SEG. The removal of this damaged layer is shown to result in highly crystalline epitaxially grown silicon.**

***Index Terms*—Plasma Etching; Plasma-induced damage; Process Simulation; Selective Epitaxial Growth; 3D NAND;**

I. Introduction

Modern three-dimensional flash memory (3D NAND) employs a large number of stacked control gates and insulating layers, comprised of alternating silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) films, leading to recent increase in storage size to up to 1.33 TB [1] on a single die [2]. The rapid scaling drives new challenges in the etching of these stacks to meet the demands of further increasing memory capacity by adding more stacked layers, thereby dramatically increasing aspect-ratios of the feature sizes. The specific challenge is the dry etching of high-aspect-ratio (HAR) channel holes through these stacks using high energy plasmas. The plasma can often introduce damage in the silicon layers by implanted ions in the silicon substrate forming the source line [3]. This heavily impacts the subsequent selective epitaxial silicon growth (SEG) of the source contact, severely decreasing its quality and leading to the formation of voids. Recent research has shown that removing the damaged silicon layer using a post etch plasma treatment can effectively remove impurities, leading to well formed SEG silicon on the bottom [4]. We propose a physical process model which is capable of simulating the channel hole dry etch process including the resulting source material damage through ion implantation, leading to undesirable voids in the source contact after SEG. The model uses a level set powered topography simulator in combination with top-down Monte Carlo ray tracing to accurately describe the surface kinetics for multiple materials and 3D geometries, combined and implemented in the ViennaTools software ecosystem [5].

II. Model

A. Surface Kinetics

To analyze the surface kinetics which describe the etching process, a model based on the theory of active surface sites is used [6]. Three different types of particle species are considered: (1) A reactive etchant forming volatile etch products which dissociate thermally and thus etch the substrate; (2) A passivating species which forms protective polymer layers on the surface; And (3) energetic ions which physically sputter the film.

B. Flux Calculation

The fluxes are calculated using a top-down Monte Carlo ray tracing approach, where a large number of particles are launched from a source plane and traced in order to find the point of surface impact. The ion sputter yield efficiencies on the point of impact are dependent on the ion energy E, as well as the incident angle α between the ion particle and the surface normal. The initial energy for each ion particle is assigned based on the process used. In general, the ion sputter yield efficiency upon impact on the surface can be expressed as

$$Y = A(\sqrt{E} - \sqrt{E_{th}})f(\alpha), \tag{1}$$

where A is a process-dependent constant, E_{th} is the minimum energy ions must have to etch the substrate referred to as threshold energy, and $f(\alpha)$ a function of the incident angle. If the energy is below the threshold, the ion is reflected specularly, until it reaches a point with a larger incident angle or it leaves the simulation domain. Polymer and etchant particles, on the other hand, reflect diffusely with varying sticking probabilities at each discretized surface point, which is captured in $f(\alpha)$.

C. Selective Epitaxial Growth

Selective epitaxial growth of silicon is simulated using the rates proposed in [7], with the Stencil-Local-Lax-Friedrichs (SLLF) numerical integration scheme, applied to the level set advection as described in [8].

D. Ion Damage

To model the damaged layer in the silicon substrate, induced by the etching process, the energy of traced ions is recorded on the substrate surface. Since the highest ion energies occur at normal incidence, the recorded energies can be used to approximate the ion damage in the material directly below the surface. For each surface point, the impinging ion energy E

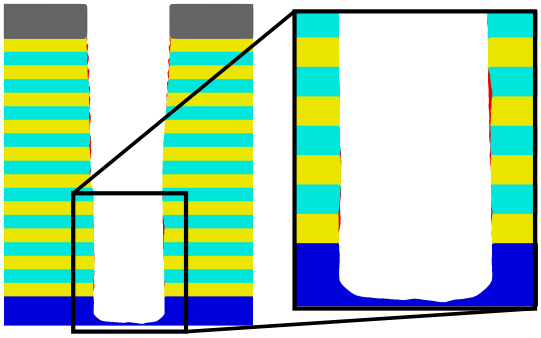

Fig. 1. Final 2D profile slice of the HAR via etching simulation. The alternating SiO_2/Si_3N_4 layers (yellow/cyan) are etched down to a bottom Si layer (blue). The thin sidewall layers (red) represent the deposited polymer formed during the etching process.

is assumed to decrease through the substrate due to scattering, following an exponential attenuation given by

$$E(d) = E_i e^{-d/\lambda}, \tag{2}$$

where E_i is the initial ion energy upon surface impact and d is the normal distance to the surface inside the material, equivalent to the penetration depth. Given the observed thickness of the damaged layer d_{th} in [4] and the threshold energy for ion enhanced etching E_{th}, the attenuation length λ is determined as

$$\lambda = d_{th} / \ln\left(\frac{E_i}{E_{th}}\right). \tag{3}$$

Next, an ion damage coefficient $D(d)$ is defined and stored for each surface point of the geometry. The coefficient is proportional to the ion energy at a depth d in the substrate:

$$D(d) \propto E(d) - E_{th}. \tag{4}$$

In order for silicon to grow epitaxially, the material must not be damaged and hence, the ion damage coefficient at the surface has to fulfill

$$D \leq 0. \tag{5}$$

To remove the damaged layer in a post etch treatment process simulation, the surface is etched using low energy ions, until the damage coefficient at the bottom surface drops below 0.

III. Plasma Chemistry

Etching is modeled as a fluorocarbon based etch process, including Ar and O_2 as inhibitor, as is commonly used for the etching SiO_2/Si_3N_4 layers. The fluorocarbon radicals CF_x^+ together with Ar^+ act as ion bombardment, while the O_2 forms a passivation layer on the substrate. Corresponding parameters are extracted from [9]. For the post etch treatment, the gas chemistry as presented in [4] was used.

IV. Results

The geometric profile of the stacked sheets after the etching simulations is shown in Figure 1. On the sidewall one can observe small residuals of the passivation layer in red.

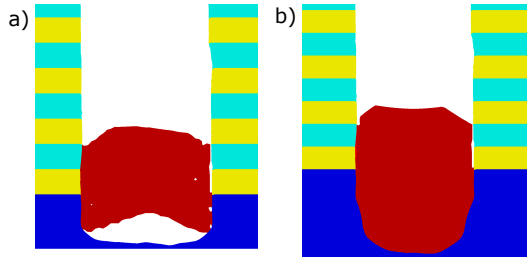

Fig. 2. Results for the selective epitaxial growth of silicon (red) after the etching process, on the bottom of the trench. In (a) a damaged layer on the surface is covering parts of the Si layer (blue, on the bottom), hence leading to an ill-formed SEG. In (b) the damaged layer is removed and the SEG covers the entire bottom, leaving no voids.

Next, SEG of silicon on the bottom of the channel hole is carried out with the resulting profiles depicted in Figure 2. When the damaged layer is present on the silicon substrate a large void is observed, leading to an ill-formed contact to the silicon source line (Figure 2a). Such defects will heavily impact the bottom select gate characteristics and reduce the overall quality of the memory stack. However, when the silicon substrate is cleaned prior to SEG, the desired SEG growth is obtained with the grown layer providing full contact with the silicon source line, shown in Figure 2b.

V. Conclusion

A physical process model is applied to simulate vertical channel hole etching in 3D NAND flash memory layers. The model is able to simulate damage induced by ion-enhanced etching with high energy ions which my implant in the source line material, heavily affecting the quality of the subsequent silicon SEG. Therefore, the proposed model allows to analyze the physical behavior of the etch process in order to optimize the fabrication conditions during channel hole etching and the post etch treatment fabrication steps. Due to the physical nature of the presented model, relevant physical effects and behaviors are incorporated appropriately and thus the model serves as a basis for the understanding of source contact formation in 3D NAND memory cells.

Acknowledgment

This work was supported in part by the Austrian Research Promotion Agency FFG (Bridge Young Scientists) under Project 878662 ”Process-Aware Structure Emulation for Device-Technology Co-Optimization”.

References

[1] Y. Li, IEEE J. Solid-State Circuits 12, 2020, pp. 56-65
[2] H. Kim, S. Ahn, Y. G. Shin, K. Lee, E. Jung, IEEE Int. Memory Workshop (IMW), 2017, pp. 1-4
[3] Yabumoto N *et al.*, Jpn. J. Appl. Phys. 20, 1981, pp. 893–900
[4] Liuyang Luo *et al.*, Semicond. Sci. Technol. 34, 2019, pp. 095004-1 – 095004-5
[5] https://github.com/ViennaTools
[6] Magna A.L., Garozzo G, J. Electrochem. Soc. 150, 2003, pp. 178-185
[7] S. Barraud *et al.*, IEDM Tech. Dig., 2018, pp. 21.3.1-21.3.4
[8] A. Toifl *et al.*, IEEE Access 8, 2020, pp. 115406–115422
[9] E. Gogolides, P. Vauvert, G. Kokkoris, G. Turban, A.G. Boudouvis, J. Appl. Phys. 88, 2000, pp. 5570–5584