Deterministic spin-orbit switching scheme for an array of perpendicular MRAM cells suitable for large scale integration

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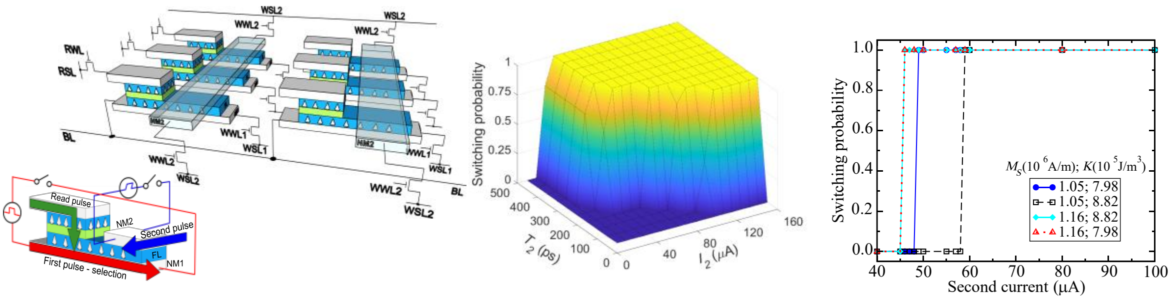
Spin-orbit torque (SOT) MRAM is a viable nonvolatile memory candidate outperforming spin-transfer torque MRAM for ultra-fast operation. However, deterministic SOT switching of a perpendicularly magnetized free layer requires an external magnetic field. Several field-free schemes have been proposed at the cost of more complex cell stack fabrication [1]. In this work we consider an alternative field-free scheme, in which a purely electrical control of the switching process is realized by applying current pulses to two orthogonal heavy metal wires [2]. The additional non-magnetic heavy metal wire (NM2) slightly increases the complexity of the cell, but its integration is straightforwardly possible by routing it through several cells in an array, cf. Fig.1(a). This requires a low current pulse through the NM2 wire to prevent disturbing non-selected cells. Based on micromagnetic simulations, we show that, after a pre-selection of the cell, the current pulse through the additional NM2 wire can be significantly reduced without loss of switching performance. Fig.1(b) shows the switching probability as a function of the second current pulse amplitude and duration. For sub-500ps operation, the minimum current is about four times lower than the nominal critical current (30µA/120µA). Decreasing the second current below the critical value is important, because it makes the corresponding torque weaker, thus not disturbing the magnetization of non-selected cells. Considering the impact of parameter variations, the minimum current to yield deterministic switching for a ±5% variation of the saturation magnetization and anisotropy constant is reported in Fig.1(c). To guarantee deterministic switching across the whole parameter variation space, the applied current has to be somewhat increased. Nevertheless, it remains lower than the critical current for all parameter combinations. This allows the integration of the cells in a crossbar architecture with the switching remaining robust, while the writing power is reduced.



(a) (b) (c)

Figure 1: (a) Crossbar memory cell array with two-current pulse switching. (b) Switching probability map for the second pulse current and width. (c) Switching probability as a function of the current of the second pulse considering material parameter variations.

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[1] K. Garello *et al.*, Proc. 2019 Symp. On VLSI Circuits (2019), T194-T195.

[2] R. L. de Orio *et al.*, IEEE J. Electron Devices Soc. **9** (2021), 61-67.