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Impact of Defects in Semiconductor Transistors on Devices and Circuits

Michael Waltl

Christian Doppler Laboratory for Single-Defect Spectroscopy at the Institute for Microelectronics, TU Wien, Vienna, Austria, Europe
E-mail: waltl@iue.tuwien.ac.at, +43-1-58801-36050

Abstract

State-of-the-art semiconductor transistors manufactured on silicon wafers exhibit a characteristic length below several tens of nanometers. The advantage of such scaled transistors is an increased switching rate and higher density devices per unit area. However, severe performance issues have to be considered in nanoscale transistors and circuits made employing these devices.

The most prominent device performance issues are bias temperature instability (BTI) and hot-carrier degradation (HCD). When the effect of BTI is investigated, drifts of the device threshold voltage are typically measured and analyzed. Quite interestingly, a continuous drift of the threshold voltage is recorded when large-area transistors are tested. In the case of nanoscale transistors, discrete steps in the drain-source current can be observed. These steps correspond to a charge capture or emission event of a defect located either at the semiconductor/insulator interface or directly in the oxide. Thus, scaled devices offer a microscopic zoom mechanism and allow a detailed study of the charge trapping kinetics and physics of single defects.

Next to device reliability, charge trapping at single defects can also affect the performance of circuits. For instance, the variability between seemingly identical devices increases towards scaled technology nodes. In consequence, a larger variation in the signal propagation delay of logic inverter circuits can be observed. In this talk, we will discuss the challenges of single defect characterization and modeling the defects' trapping behavior. Finally, an overview of the consequences for integrated circuits employing nanoscale transistors will be presented.

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