

**OPEN ACCESS**

## Review—Modeling Methods for Analysis of Electromigration Degradation in Nano-Interconnects

To cite this article: H. Ceric *et al* 2021 *ECS J. Solid State Sci. Technol.* **10** 035003

View the [article online](#) for updates and enhancements.

### Discover the EL-CELL potentiostats

- Fully independent test channels with Pstat / GStat / EIS
- Optionally with integrated temperature controlled cell chamber
- Unique Connection Matrix: Switch between full-cell and half-cell control at runtime

[www.el-cell.com](http://www.el-cell.com) +49 (0) 40 79012 734 [sales@el-cell.com](mailto:sales@el-cell.com)





# Review—Modeling Methods for Analysis of Electromigration Degradation in Nano-Interconnects

H. Ceric,<sup>1,z</sup> S. Selberherr,<sup>1</sup> H. Zahedmanesh,<sup>2</sup> R. L. de Orio,<sup>1</sup> and K. Croes<sup>2</sup>

<sup>1</sup>Institute for Microelectronics, TU Wien, 1040 Wien, Austria

<sup>2</sup>imec, Leuven 3001, Belgium

Mitigation of the degradation for down-scaled interconnects requires an in-depth understanding of the failure mechanisms of electromigration and, therefore, the development of adequate simulation models based on this understanding. We present a novel concept for modeling of nano-interconnect structures, the effective domain method, which describes the impact of grain boundaries and grain distribution on the nano-interconnect reliability and how this impact changes with down-scaling of the interconnect width. Furthermore, a simple and numerically efficient approach for modeling of void growth and its influence on nano-interconnect resistivity is presented. Both novel approaches are studied on timely nano-interconnect layouts and discussed in comparison to experimental results. The simulations based on the novel modeling concept predict the reduction of interconnect lifetime with increased temperature and the reduced linewidth, as observed in experiments.

© 2021 The Author(s). Published on behalf of The Electrochemical Society by IOP Publishing Limited. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, <http://creativecommons.org/licenses/by/4.0/>), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2162-8777/abe7a9]



Manuscript submitted December 21, 2020; revised manuscript received February 8, 2021. Published March 4, 2021. *This paper is part of the JSS Focus Issue on Solid State Reviews.*

Supplementary material for this article is available [online](#)

The drastic reduction of nano-interconnects' linewidth toward 10 nm and below has a tremendous impact on the interconnect reliability.<sup>1,2</sup> This development has brought to the fore the crucial question, how far one can go with Cu as an interconnect metal, until one reaches a point where the reduction in electromigration (EM) reliability becomes unacceptable. Interconnect reliability is affected by degradation processes driven by EM, mechanical stresses, and thermal effects, which are inextricably interwoven on a physical fundamental level. The complexity of the reliability problem is further increased by the effect of the metallic microstructure.<sup>3</sup> Each degradation process includes the dynamics of native crystal point defects and extended defects, like grain boundaries (GBs) and dislocations, and their interaction with metal interfaces to surrounding layers. These interfaces are becoming more and more important as the technology moves toward interconnect linewidths of 10 nm and below due to the fact that a higher ratio of point defect migration is conducted along them.<sup>1,3</sup> Subsequently, interconnect reliability becomes more sensitive to the physical parameters defining point defect migration along the interfaces.

Improvement of the reliability for future Cu based interconnects can be obtained by the introduction of technology modifications. A significant improvement was achieved by introduction of CoWP capping layers which efficiently suppressed EM along interfaces.<sup>4</sup> Another possibility to influence EM behavior is to change the barrier layer which covers the bottom and side walls of the copper interconnect from a typically Ti or Ta based material to Ru, Co, or its alloys, etc.<sup>5,6</sup> Low-*k* materials have been introduced to ensure high performance of ICs, but, unfortunately, they have brought additional thermal and mechanical problems. Low mechanical strength of low-*k* materials does not offer as much restraint for the degradation driving forces as the silica-based interlevel dielectric. Another problem with low-*k* dielectrics is their poor thermal conductivity, which adds to the already severe thermal problems of ICs.<sup>7</sup> A significant portion of atomic migration takes place along GBs and, consequently, the geometrical distribution of GBs has an impact on the interconnect failure development. In order to suppress EM along GBs dilute Cu alloys have been successfully applied. A significant reduction of material transport along the GBs has been achieved by alloying Cu with Al<sup>8</sup> and Mn.<sup>9–11</sup> In order to predict interconnect failure behavior it is important to capture both the GB distribution and the physics of a single GB in a satisfactory manner.

Modeling the vacancy flux and mechanical stress in each single grain<sup>12</sup> and at the GBs is possible but it is a time-consuming venture, particularly if, for the sake of accuracy, one needs to include large portions of the interconnect layout in the simulation.

To reconcile these demands, we developed the *effective domain method*, which allows for a computationally optimal description of the impact of the GB network and interfaces on the interconnect reliability and also predicts, how this impact changes with decreasing interconnect linewidth. The level of modeling is chosen according to the predominant microstructural features of the studied interconnect line. For the regions of the interconnect line with a dense network of GBs, the averaged EM model parameters are used, while for the domains filled with a single grain or a number of larger grains detailed modeling is applied. The effective domain method is used in combination with state-of-the-art EM models<sup>13,14</sup> adequate to determine the site and the time of nucleation of intrinsic void in arbitrarily three-dimensional interconnect geometries. In addition to the effective domain method, we developed a simple but computationally efficient method for estimation of the void growth time up to the complete failure of the interconnect line. Choosing a simple three-dimensional geometry for reproducing the void shape we derive an analytical expression for the maximum void surface velocity. Both methods are used as practical tools to investigate how different reliability impact factors, like linewidth, microstructure, cap layer material, etc. influence nano-interconnect reliability and help finding an optimal way to improve it. In the next section, after providing a general modeling framework based on earlier publications, a novel, effective domain method, is introduced and discussed. Several nano-interconnect reliability study cases, utilizing the effective domain method, are presented.

## Theoretical Background

The proposed model uses the framework,<sup>13</sup> which represents a further development from the original work of Sarychev, Zithnikov et al.<sup>15</sup> According to this modeling approach, the lifetime of an interconnect structure,  $t_f$ , consists of a void nucleation time,  $t_N$ , and a void evolution time,  $t_E$ , corresponding to two failure development phases.

$$t_f = t_N + t_E \quad [1]$$

The modeling of the first phase demands the solution of the vacancy balance equation together with the Laplace equation, the heat-

<sup>z</sup>E-mail: [ceric@iue.tuwien.ac.at](mailto:ceric@iue.tuwien.ac.at)

transport equation, and the mechanical equations. The modeling of the second phase requires the solution of all equations from the first phase together with the models describing the evolving void surface.<sup>13</sup>

In this work the detailed modeling approach, i.e., the approach involving the full set of partial differential equations numerically solved for three-dimension structures,<sup>12,13</sup> is applied only for the first phase of the failure evolution. The detailed modeling of the first phase of the failure development is necessary, since it provides the framework within which a novel, effective domain method, for the description of metallic microstructure will be applied.

For the second phase we introduce and apply an approximate analytical approach. Our goal here is not to develop a new detailed physical model for void evolution, but an analytical approximation which allows for a fast estimation of the void growth time.

**Vacancy dynamics and mechanical effects.**—The central governing equations of EM models are the vacancy flux Eq. 2 and the vacancy balance Eq. 3.<sup>15</sup>

$$\vec{J}_v = D_{\text{eff}} \left( \frac{C_v}{kT} |Z_{\text{eff}}^* e| \rho \vec{j} + \frac{C_v}{kT} f \Omega \nabla p - \nabla C_v \right) \quad [2]$$

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G_{\text{eff}}(C_v) \quad [3]$$

$D_{\text{eff}}$  is the local diffusivity,  $C_v$  is the vacancy concentration,  $p$  is the hydrostatic stress,  $\rho$  is the interconnect resistivity,  $\vec{j}$  is the current density,  $\Omega$  is the atomic volume, and  $f$  is the atom-vacancy relaxation factor.  $G_{\text{eff}}$  is the Rosenberg-Ohring recombination term<sup>16</sup> and  $Z_{\text{eff}}^*$  is the effective valence.

The bulk effective valence,  $Z_{\text{bulk}}^*$ , and resistivity,  $\rho$ , are related on the fundamental physical level, because both parameters characterize different aspects of electron scattering in a current carrying metal.<sup>17,18</sup>

$$Z_{\text{bulk}}^*(T) = Z_d + Z_w(T) = Z_d + \frac{K}{\rho(T)} \quad [4]$$

$Z_d$  is the direct valence, which is assumed to be equal to the bare valence of Cu.  $K$  is the proportionality factor which has been fitted for  $Z_{\text{bulk}}^*$  for the thick interconnect, at the room temperature. Various advanced models can be used for modeling the interconnect resistivity.<sup>19</sup>

The values of  $D_{\text{eff}}$ ,  $G_{\text{eff}}$ , and  $Z_{\text{bulk}}^*$  depend on the features of a given microstructure, and they will be dealt with in the next section.

In order to reproduce realistic mechanical conditions all materials in the structure and their corresponding properties must be included in the overall modeling framework.

Both the void nucleation, as well as the void evolution model, are solved simultaneously with the equations of mechanics.<sup>13</sup>

$$\frac{\partial \varepsilon_{ij}^v}{\partial t} = \frac{1}{3} \Omega [(1-f) \nabla \cdot \vec{J}_v + f G_{\text{eff}}(C_v)] \delta_{ij} \quad [5]$$

$$\nabla \cdot \sigma = \mathbf{0}, \quad \sigma = \mathbf{E}(\varepsilon - \varepsilon^v - \varepsilon^{\text{th}}) \quad [6]$$

$\mathbf{E}$  is the the fourth-order elasticity tensor,  $\varepsilon^v$  is the volumetric strain component which rises due to EM, and  $\varepsilon^{\text{th}}$  represents the impact of thermal loads.

From the stress tensor,  $\sigma$ , the normal stresses at all interfaces and GBs can be obtained. The *void nucleation phase* ends, when one of the normal stresses surmounts the local critical stress threshold  $\sigma_{\text{crit}}$ , which is discussed in the next section. The time needed for critical stress threshold to be reached is the void nucleation time,  $t_E$ .

For the determination of the critical stress threshold the approach applied in a previous publication is used,<sup>20</sup> which is an adaptation

from the earlier work by Ch. S. Hau-Riege, S. P. Hau-Riege and A. P. Marathe.<sup>21</sup>

**Modeling of the microstructure.**—The microstructure of Cu interconnects generally depends on the technological process, the interconnect geometry, and the choice of surrounding materials. Different choices of materials for barrier and cap layers may influence properties of the microstructure.<sup>22</sup> There are several studies dealing with the impact of Cu microstructure on the EM failure behavior.<sup>23,24</sup> They describe how the GBs distribution and texture inside single grains influence the interconnect failure and the failure time distribution. For a complete modeling of the microstructure, besides a description of the grain crystallography, an appropriate understanding of the GB physics is a necessity. The following three aspects of GB physics must be considered:<sup>12</sup>

- (i) The GB as a fast diffusivity path.
- (ii) The GB as a site of vacancy production and annihilation.
- (iii) The GB as an obstacle to material transport.

There are three different methods to include the GB effect in EM models:

- (i) **The effective values approach:** The effective diffusivity, effective valence, and the source function (see (3)) are calculated by means of formulas which include interconnect dimensions, average grain size, and GBs orientations.<sup>20,25</sup>
- (ii) **The distributed order parameter approach:** The diffusivity is set according to a numerically generated microstructure.<sup>26</sup>
- (iii) **The detailed GB modeling approach:** Each GB is modeled as a two-dimensional domain with a detailed model describing vacancy transport inside the GB and vacancy exchange with neighboring grains.<sup>12</sup>

While all three approaches have their merit, for the practical realization of the effective domain method, the Method 1 and the Method 3 are the most appropriate and they will be discussed in detail.

In the case of typical microstructures for nano-interconnects, two additional aspects must be considered. First, the microstructure strongly depends on the interconnect width and second, due to the increased temperatures during operation, the microstructure may undergo transformations. Experimental SEM/FIB/EBSD<sup>27-31</sup> studies of interconnects' microstructure provide the grain size distribution and the crystal orientations inside grains. These studies show that the grain sizes inside Cu interconnects are distributed according to the lognormal distribution and tend to have several predominant crystal orientations.<sup>32</sup>

The effective values approach has been used for a long time to model the cumulative effect of different atomic transport paths on the overall diffusivity. The main advantage of this approach is its simplicity, because one basically needs only the geometrical dimensions of the interconnect line and some characteristics of microstructure to calculate an effective value of diffusivity and effective valence.

Let us assume that the grain size ( $l$ ) distribution in a nano-interconnect obeys a lognormal distribution with a probability density function

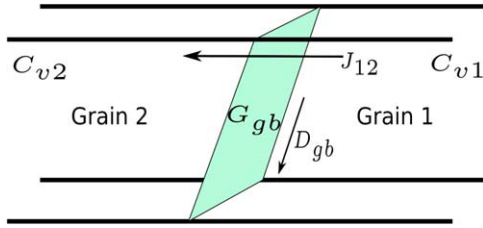
$$f(l) = \frac{1}{\sqrt{2\pi} \sigma l} \exp\left(-\frac{\ln^2(l/m)}{2\sigma^2}\right), \quad [7]$$

where  $m$  is the median and  $\sigma$  standard deviation. The average grain size (expected value) is given as

$$\langle l \rangle = E[l] = \int_0^\infty l f(l) dl = e^{\frac{\sigma^2}{2}} m. \quad [8]$$

According to Smith's theory<sup>33</sup>

$$\epsilon_p = \frac{2\delta_s}{\langle l \rangle}, \quad [9]$$



**Figure 1.** Schematic picture of the two-dimensional GB plane.

where  $\epsilon_p$  is the GB volume fraction and  $\delta_s$  the GB width. The volume fraction dependent effective values of the Rosenberg-Ohring term,  $G_{\text{eff}}$ , the effective valence,  $Z_{\text{eff}}^*$ , and the effective diffusivity,  $D_{\text{eff}}$ , are given by the following terms, respectively:<sup>20,34</sup>

$$G_{\text{eff}}(C_v) = -(C_{\text{eq}} - C_v) \left( \frac{1 - \epsilon_p}{\tau_{\text{bulk}}} + \frac{\epsilon_p}{\tau_{\text{gb}}} \right) \quad [10]$$

$$Z_{\text{eff}}^* = Z_{\text{bulk}}^*(1 - \epsilon_p) + Z_{\text{gb}}^*\epsilon_p \quad [11]$$

$$D_{\text{eff}} = D_{\text{bulk}} + D_{\text{lin}} \left( \frac{2}{w} + \frac{1}{h} \right) \delta_{\text{l-lin}} + D_{\text{cap}} \frac{\delta_{\text{l-cap}}}{h} + \epsilon_p D_{\text{gb}} \quad [12]$$

$h$  is the interconnect height and  $w$  is the interconnect width. Each of the transport paths is characterized by its diffusivity and its thickness: bulk ( $D_{\text{bulk}}$ ,  $h$ ), cap layer ( $D_{\text{cap}}$ ,  $\delta_{\text{l-cap}}$ ), and liner ( $D_{\text{lin}}$ ,  $\delta_{\text{l-lin}}$ ).

Equations 10, 11, and 12 can be directly used for parametrization of the vacancy dynamics model given by Eqs. 2 and 3, however, this type of ‘‘cumulative’’ microstructure description is inadequate to capture microstructural features important for nano-interconnect reliability.

The model which is able to capture all the relevant microstructural aspects requires a detailed description of vacancy dynamics at a

single GB as introduced in Ref. 12. For the implementation in the GB plane (Fig. 1), the model is described by the Rosenberg-Ohring term.

$$G_{\text{gb}} = -\frac{1}{\tau_{\text{gb}}} \left( C_v^{\text{eq}} - C_v^{\text{im}} \left( 1 - \frac{2\omega_R}{\omega_T(C_{v1} + C_{v2})} \right) \right) \quad [13]$$

and a segregation condition at the GB, which regulates vacancy transport from the Grain 1 to the Grain 2.

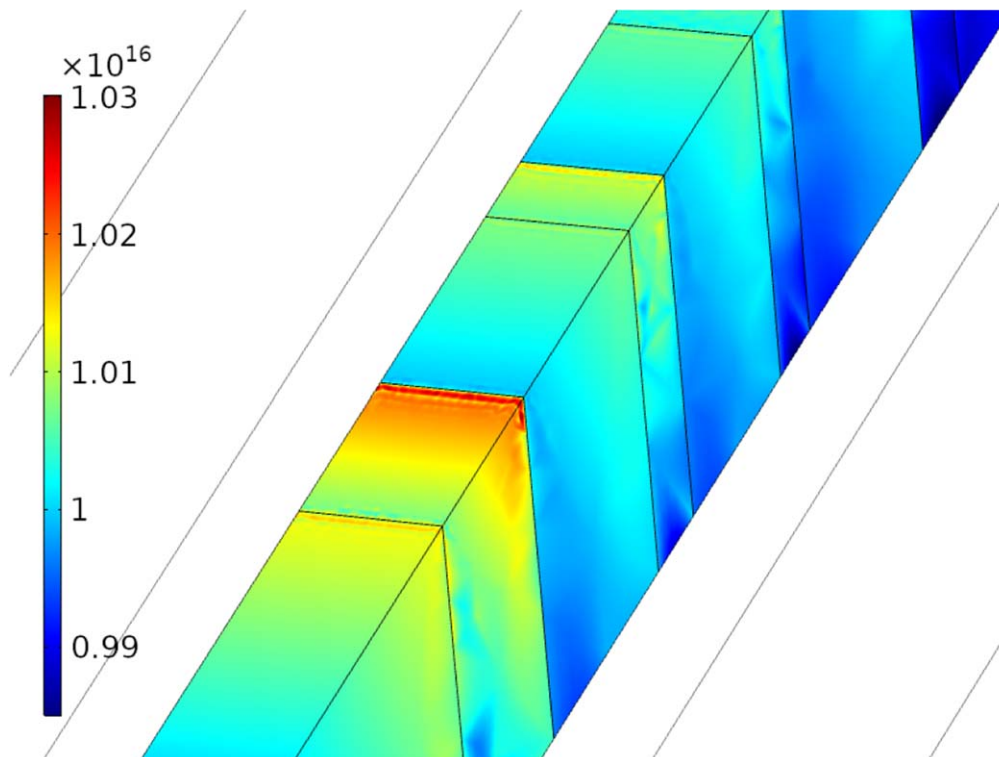
$$J_{12} = \omega_T(C_v^{\text{eq}} - C_v^{\text{im}})(C_{v1} - C_{v2}) \quad [14]$$

Here,  $C_{v1}$  and  $C_{v2}$  are the vacancy concentrations in Grain 1 and Grain 2, respectively,  $\omega_T$  is the vacancy trapping rate,  $\omega_R$  is the vacancy release rate,  $C_v^{\text{im}}$  is the concentration of vacancies trapped in the GB,  $C_v^{\text{eq}}$  is the equilibrium vacancy concentration, and  $\tau_{\text{gb}}$  is the vacancy recombination rate. The model is completed by setting the diffusivity  $D_{\text{GB}}$  in the GB plane. The detailed GB model, combined with the vacancy dynamics Eqs. 2 and 3, produces pile-ups of vacancies at triple points in three-dimensional microstructure, as shown in Fig. 2. The corresponding peaks of the mechanical stress are presented in Fig. 3.

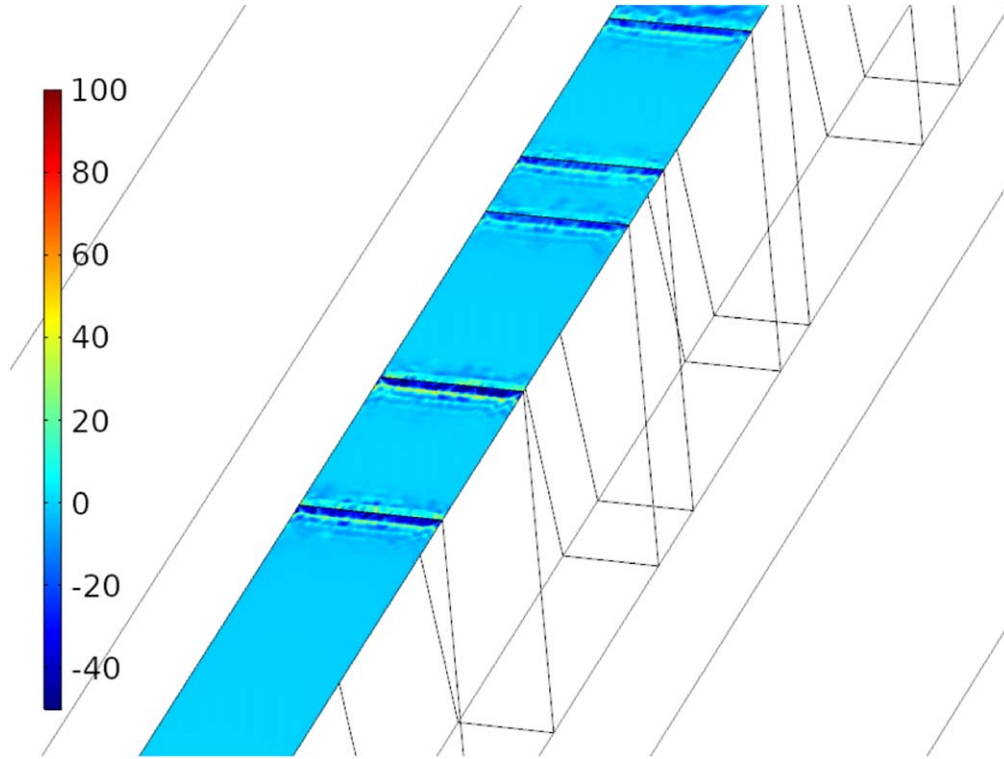
The detailed GB model can be applied at the surface of an arbitrary shape defining the GB between two adjacent grains. The only condition is an appropriate FEM discretization of this surface.

For the implementation of the effective domain method a combination of the effective values approach and the detailed GB model is utilized, as presented in the next section.

**The effective domain method.**—The main idea of the effective domain method is to capture the microstructural features of the metallic interconnect by an artificial, replacement microstructure which emulates the effect of the real microstructure in a satisfactory manner, e.g. the replacement microstructure reproduces the physics of GBs and its impact on the interconnect reliability. While detailed modeling of the microstructure is possible for interconnects



**Figure 2.** Increase of vacancy concentration ( $1 \text{ cm}^{-3}$ ) close to triple points along the capping layer. The locations of the peak vacancy concentrations correspond to the peaks of tensile stress.



**Figure 3.** Peaks of mechanical stress (MPa) close to triple points along the capping layer.

portions of moderate size, it becomes numerically demanding and cumbersome for interconnect dimensions relevant for practical engineering. Moreover, for a complete simulation approach the simultaneous consideration of the effect of the interfaces is necessary. Therefore, a new method is needed to cover the typical microstructures of the nano-interconnect.<sup>3,27</sup>

For the purpose of modeling, the interconnect metal is divided into *polycrystalline* and *large* grain domains. In the polycrystalline domains material transport is dominated by atomic migration along GBs (with the diffusivity  $D_{gb}$ ). The atomic migration along interfaces, and in particular along the metallic interface to the cap layer is inhibited by the tripple-point intersections of the GBs and the cap layer and thus, it can be generally neglected.<sup>8</sup> The effective diffusivity in this case becomes

$$D_{\text{eff}} = \epsilon_p D_{gb}. \quad [15]$$

We assume that large crystal domains contain 1–3 single grains and thus the atomic transport is dominated by the atomic transport along the interfaces, defined by the diffusivity along the cap layer ( $D_{\text{cap}}$ ) and the diffusivity along the liner ( $D_{\text{lin}}$ ). The effective diffusivity in the case of large grain domains is

$$D_{\text{eff}} = D_{\text{cap}} \frac{\delta_{\text{I-cap}}}{h} + D_{\text{lin}} \left( \frac{2}{w} + \frac{1}{h} \right) \delta_{\text{I-lin}} + D_{gb} \epsilon_s \langle \cos \theta \rangle, \quad [16]$$

where  $\epsilon_p$  and  $\epsilon_s$  are the GB volume ratios for the polycrystalline and the large grain domains, respectively.  $\langle \cos \theta \rangle$  is the average cosine between GBs and the current flow direction. In the case of a single grain domain  $D_{gb} = 0$ .

The material transport between the polycrystalline and the single grain domains is modeled by the *detailed grain boundary model* (see the previous section). In this approach the Rosenberg-Ohring term,  $G_{\text{eff}}$ , is assumed to be active only in the polycrystalline domains.

The geometrical constellation of the polycrystalline and the large grain domains is chosen according to the prevalent microstructure of

the interconnect metal. A couple of different constellations is displayed in Fig. 4. As we can see, the whole replacement microstructure of the effective domain method is defined by an array of the lengths of the polycrystalline domains ( $L_{p,1}, L_{p,2}, L_{p,3}, \dots$ ) and the large grain domains ( $L_{s,1}, L_{s,2}, L_{s,3}, \dots$ ). The  $L_p$  and  $L_s$  are stochastic variables which obey a lognormal distribution, because the grain size ( $l$ ) distribution is also lognormal.<sup>35</sup>

Besides  $L_p$  and  $L_s$ , for the configuration of the effective domain method a set of general parameters is needed, including diffusivities, interconnect dimensions, and transport path thicknesses ( $\delta_{\text{I-cap}}, \delta_{\text{I-lin}}, \delta_s$ ). Furthermore, for modeling the impact of the microstructure on the diffusivities, the GB volume ratios in the large grains,  $\epsilon_s$ , and polycrystalline domains,  $\epsilon_p$ , must be considered. The extraction of microstructure specific parameters is discussed in the next sections.

**Extraction of microstructural parameters from experiments and microstructure simulations.**—As a part of the usual interconnect reliability analysis, a graphical two-dimensional microstructure representation as in Fig. 5 can be extracted from EBSD grain maps<sup>36</sup> and also obtained by microstructure simulations.<sup>27</sup> Such a representation is the basis for the extraction of  $\epsilon_s$  and  $\langle \cos \theta \rangle$ , which are required for the evaluation of expression (16).

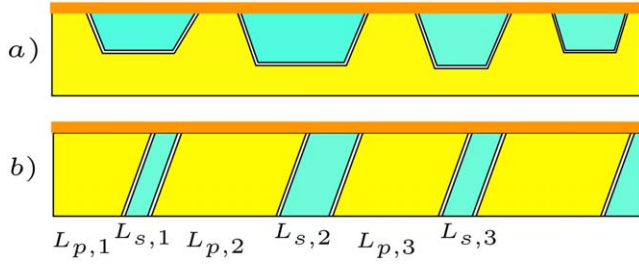
Assuming that the total length of all GBs, as determined from Fig. 5 for a segment of interconnect with length  $L$ , width  $w$ , and height  $h$ , is equal to  $S$ ,  $\epsilon_s$  is estimated according to Eq. 17.

$$\begin{aligned} \epsilon_s &= \frac{\text{Total GB volume}}{\text{Total interconnect volume}} \\ &= \frac{S \times w \times \delta_s}{L \times w \times h} = \frac{S \delta_s}{L h} \end{aligned} \quad [17]$$

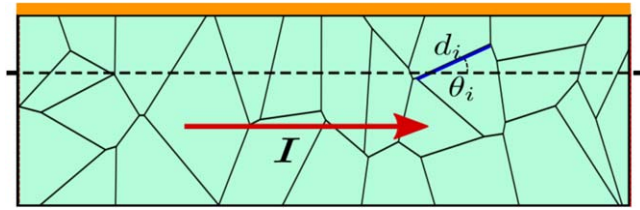
For the estimation of  $\langle \cos \theta \rangle$ ,  $N$  GBs are randomly sampled from Fig. 5. For each GB from the sampled collection, indexed by  $i$  with length  $d_i$ , the angle  $\theta_i$  to the current flow direction is determined.

After extracting  $N$ -tuples  $(d_i, \theta_i)$  corresponding to the  $N$  sampled GBs, the average cosine  $\langle \cos \theta \rangle$  is estimated as





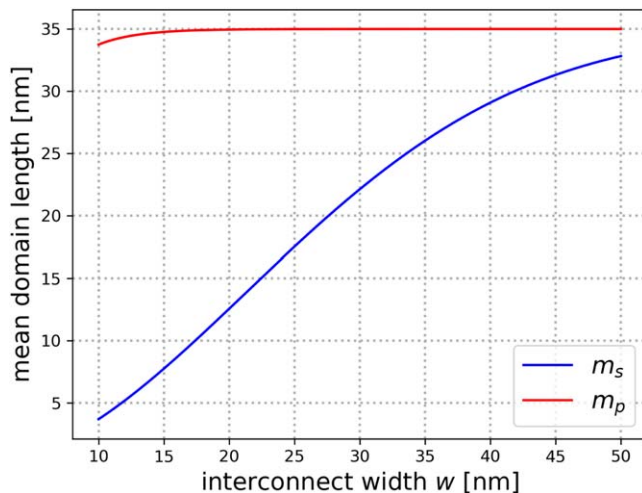
**Figure 4.** Effective domain method: The interconnect is divided in polycrystalline (yellow) and large grain domains (turquoise): (a) large grain domains embedded in a single polycrystalline domain, (b) alternate polycrystalline and large grain domains.



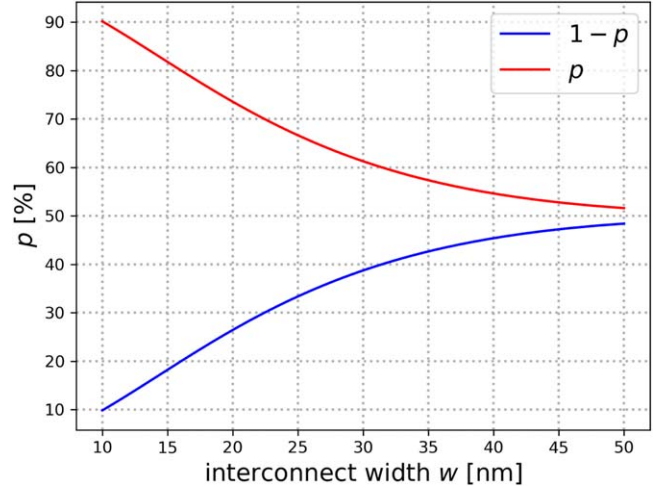
**Figure 5.** Sampling of  $d_i$  and  $\theta_i$  from the GB-network obtained from experimental imaging.

$$\langle \cos \theta \rangle = \frac{\sum_{i=1}^N d_i \cos \theta_i}{\sum_{i=1}^N d_i}. \quad [18]$$

**Microstructure behavior and interconnect width.**—The effective domain method allows for an efficient modeling of the impact of the decreasing interconnect width on the interconnect microstructure. When the interconnect width reduces, the mean grain size, the mean length of polycrystalline domains  $m_p$ , and also the mean length of the large grain domains  $m_s$  change. The deposition of an interconnect metal in trenches during the dual-damascene process and the subsequent transformation of the microstructure is a complex process involving process conditions (e.g. temperature), the geometry and the dimensions of trenches, and the surface properties of the trench bottom and of the sidewalls. Several modeling approaches have been used for the simulation of microstructures: the Monte Carlo model, the vertex or front-tracking model, the level set model,



**Figure 6.** Mean length of the polycrystalline and the large grain domains as a function of the interconnect linewidth.



**Figure 7.** The change of polycrystalline domain ratio,  $p$ , and large grain domain ratio,  $1 - p$ , as a function of the interconnect width.

and the phase-field model.<sup>32</sup> Owing to the explicit three-dimensional geometry of the trenches, three-dimensional simulation methods for analysis of realistic microstructures are necessary.

Generally speaking, for a given linear interconnect geometry, both the mean grain size,  $m$ , as well as the standard deviation,  $\sigma$ , of the grain size distribution, are functions of the interconnect width and interconnect height.

$$\begin{aligned} m &= F_1(h, w) \\ \sigma &= F_2(h, w) \end{aligned} \quad [19]$$

Thus, the corresponding mean values  $m_p$ ,  $m_s$  and the standard deviations  $\sigma_p$ ,  $\sigma_s$ , are functions of the interconnect dimensions. Previous analytical studies<sup>37</sup> have shown that two tendencies are observed for a thin metallic line. The first tendency is that both, the length of polycrystalline domains as well as the length of single crystal domains, decrease, but the ratio of polycrystalline in relation to single domains increases. The second tendency is that the mean grain size saturates for thicker interconnect lines.<sup>3</sup>

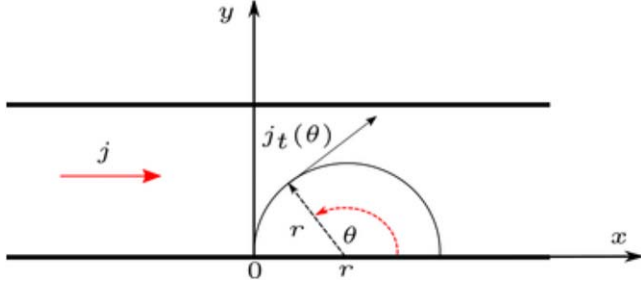
Let us assume that for an interconnect with the reference linewidth  $w_0$  the mean domain lengths are  $m_s^0$  and  $m_p^0$ . For modeling the functional dependence of  $m_p$  and  $m_s$  on a linewidth  $w$ , and in accordance to the abovementioned tendencies, we propose the following relationships:

$$\begin{aligned} m_s(w) &= m_s^0 \frac{1 - e^{-q(w/w_0)^2}}{1 - e^{-q}}, \\ m_p(w) &= m_p^0 \frac{1 - e^{-q(w/w_0)^2}}{1 - e^{-q}}, \quad \text{for } w \leq w_0 \end{aligned} \quad [20]$$

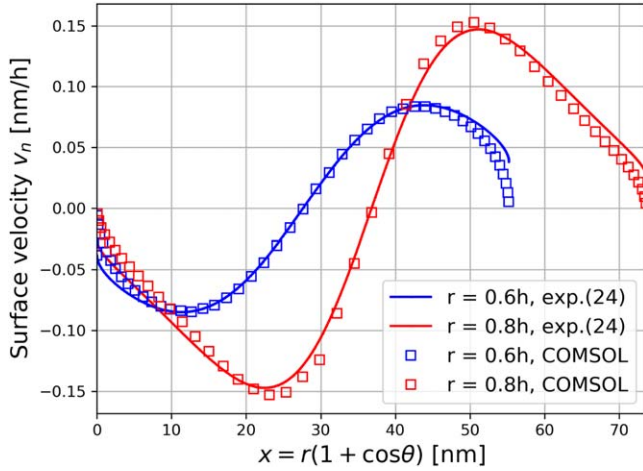
For the chosen numerical values,  $30 \text{ nm} \leq m_s^0, m_p^0 \leq 35 \text{ nm}$  for  $w = 50 \text{ nm}$ , the saturation behavior of the mean values is demonstrated in Fig. 6. The detailed method for the parameterization of (20), e.g. the determination of  $m_s^0, m_p^0$ , and  $q$  from experiments is out of the scope of this paper and is the subject of a future work. The ratio  $p$ ,

$$p = \frac{m_p}{m_s + m_p}, \quad [21]$$

behaves as presented in Fig. 7. This ratio is easily extracted from experiments and exceptionally useful for extended studies of the role of fast diffusivity paths and the extraction of the corresponding activation energies.<sup>8</sup>



**Figure 8.** Structure used in the derivation of Eq. 29.



**Figure 9.** Comparison between analytically calculated surface normal velocity (31) with FEM calculation performed in COMSOL Multiphysics<sup>38</sup> for 100 °C.

**Void evolution.**—In order to estimate the duration of the second phase of failure development, it is necessary to predict the void growth velocity. The normal velocity,  $v_n$ , of the void surface is calculated according to Ref. 13

$$v_n = \Omega(\vec{J}_v \cdot \vec{n} - \nabla \cdot \vec{J}_s). \quad [22]$$

From (22) it can be seen that the void surface evolves due to the vacancy transport in the normal direction,  $\vec{J}_v \cdot \vec{n}$ , and the divergence of the surface atomic flux,  $\nabla \cdot \vec{J}_s$ . The surface atomic flux itself,  $\vec{J}_s$ , rises due to the tangential component of the current density,  $\vec{j}_t$ , and the surface gradient of the chemical potential  $\mu_s$ .

$$\vec{J}_s = -\frac{D_s \delta_s}{kT\Omega} (|Z_s^* e| \rho \vec{j}_t + \nabla_s \mu_s) \quad [23]$$

$D_s$  is the surface diffusivity and  $\delta_s$  is the thickness of the diffusion layer. The surface chemical potential,  $\mu_s$ , is given as

$$\mu_s = \Omega(W_s - \gamma_s \kappa), \quad [24]$$

where  $\gamma_s$  is the surface energy,  $\kappa$  is the local curvature of the surface, and  $W_s = (\sigma : \epsilon)/2$  is the local elastic strain energy density.

From (22)–(24) follows that there are four components of the surface velocity: the elastic strain energy velocity component  $v_n^s$ , the electromigration velocity component  $v_n^e$ , the surface free energy velocity component  $v_n^f$ , and the vacancy absorption velocity component  $v_n^v$ .

The total velocity,  $v_n$ , is obtained as a sum of the four velocity components.

$$v_n = v_n^s + v_n^e + v_n^f + v_n^v \quad [25]$$

In this work we assume that the void possesses throughout its growth a half-cylinder shape and that the electromigration velocity component ( $v_n^e$ ) dominates over the other three velocity components.

$$v_n^e = \frac{D_s \delta_s \rho |Z_s^* e|}{kT} \nabla_s \vec{j}_t \quad [26]$$

The lower limit (the worst case) of the void evolution time,  $t_E$ , is obtained by assuming that the whole void of radius  $r$  grows with the maximum velocity at its surface,  $v_n^{\max}(r)$ .<sup>14</sup>

$$t_E = \int_{r_0}^{r_c} \frac{dr}{v_n^{\max}(r)} \quad [27]$$

Here, the critical void radius,  $r_c$ , is the solution of the equation

$$R_{\text{failure}} = R_{\text{total}}(r_c), \quad [28]$$

where the resistance function  $R_{\text{total}}(r)$  ( $r = a = b$ ) is derived in the next section, Eq. 34. The initial radius of a void,  $r_0$ , is estimated based on the local pressure distribution in the vicinity of the triple point where the void is assumed to emerge, as explained in Ref. 14.

Even if the overall simulation is three-dimensional, due to the assumption of a half-cylindrical void, the tangential component of the current density  $j_t(r, \theta)$  can be estimated for all void sizes and interconnect thicknesses  $h (= 2w)$

$$j_t(r, \theta) = \frac{j_0 h \sin \theta}{h - r \sin \theta} q(r). \quad [29]$$

Here  $j_0$  is the current density far away from the void surface (in a region unperturbed by the presence of a void) and the angle  $\theta$  determines the position on the void surface. Expression (29) is derived analytically, on the basis of Fig. 8.  $q(r)$  is an additional fitting function introduced to closely match the analytical surface velocity calculations with those calculated with COMSOL Multiphysics<sup>38</sup>

$$q(r) = \sum_{i=0}^n (-1)^i \left(\frac{r}{h}\right)^{2i}. \quad [30]$$

By substituting (29) in (26) the following expression is obtained:

$$v_n(r, \theta) = \frac{D_s \delta_s \rho |Z_s^* e|}{kTr} \frac{dj_t(r, \theta)}{d\theta} \quad [31]$$

The comparison of analytical surface normal velocity calculations (31) and COMSOL Multiphysics<sup>38</sup> FEM calculations for  $h = 2w = 46$  nm and a current density  $j = 1.0$  MA cm<sup>-2</sup> for two different void sizes ( $r_1 = 0.6h$  and  $r_2 = 0.8h$ ) is shown in Fig. 9.

Since we are interested in the worst case scenario, i.e., void growing with the maximum surface velocity, for the estimation of the void evolution time  $t_E$  in (27) the following expression is used:

$$v_n^{\max}(r) = \frac{D_s \delta_s \rho |Z_s^* e|}{kTr} \max_{0 \leq \theta \leq \pi} v_n(r, \theta) \quad [32]$$

**Resistance calculation.**—An increase of the interconnect resistance leads to interconnect failure. This resistance increase is caused by emergence, and subsequent growth, shape change, and movement of intrinsic voids. The evolving void surface can be modeled with different levels of accuracy, but more accurate modeling is more computationally demanding. For the sake of simplicity and speed of calculation, in this work we use three-dimensional void shapes with a simple geometrical basis, like a half-circle and a half-ellipse.

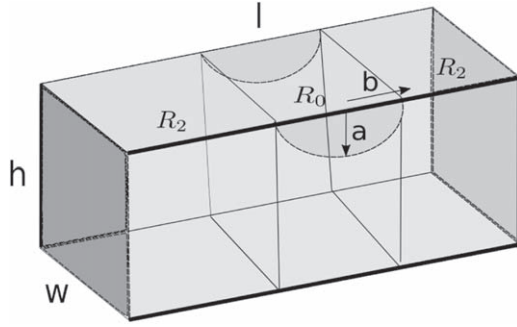


Figure 10. Structure used in the derivation of Eq. 33.

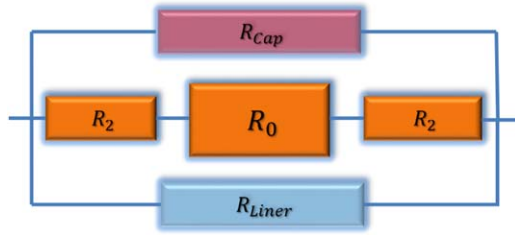


Figure 11. Replacement schema for a segment of an interconnect containing a cylindrical void. The resistances of the cap layer,  $R_{cap}$ , and the liner,  $R_{lin}$ , are included.

The resistance of an interconnect segment containing a cylindrical void with elliptical basis ( $2a$  and  $2b$  are the minor and major axes, Fig. 10) is

$$R_0(a, b) = \frac{a\rho}{bw} \left[ \pi \left( \frac{h}{s} - 1 \right) + \frac{2h}{s} \arctan \left( \frac{b}{s} \right) \right] \quad [33]$$

with  $s = (h^2 - b^2)^{1/2}$ .

The total resistance  $R_{total}(a, b)$  for a void placed in a straight interconnect line is calculated according to the equivalent circuit presented in Fig. 11.

$$\frac{1}{R_{total}(a, b)} = \frac{1}{R_{cap}} + \frac{1}{R_{lin}} + \frac{1}{R_{metal}(a, b)} \quad [34]$$

$$R_2(b) = \frac{\rho_{metal}(l - 2b)}{2wh} \quad [35]$$

$$R_{metal}(a, b) = 2R_2(b) + R_0(a, b) \quad [36]$$

With expressions (27) and (31), and the resistance calculations from the previous section, the dependence of the void growth time on the interconnect dimensions can be calculated. Figure 12 shows the resistance increase for an interconnect section  $1 \mu\text{m}$  long and  $23 \text{ nm}$  wide for three different temperatures and a current density  $j = 1.0 \text{ MA cm}^{-2}$ .

**Overall scheme.**—In order to estimate the interconnect lifetime ( $t_f$ ), both the void nucleation ( $t_N$ ), as well as the void evolution time ( $t_E$ ) must be estimated as accurately as possible. The complete simulation scheme utilized in this work is presented in Fig. 13. As we can see, the overall simulation procedure is divided into two parts: estimation of  $t_N$  (void nucleation time), which is performed by application of FEM, and the estimation of  $t_E$  (void evolution time), which is carried out analytically. The equation system which is solved in the FEM part of the simulation consists of Eqs. 2, 3, 5, and 6 together with the Laplace equation for the electric field (see Fig. 13). The solution of the Laplace equation provides the

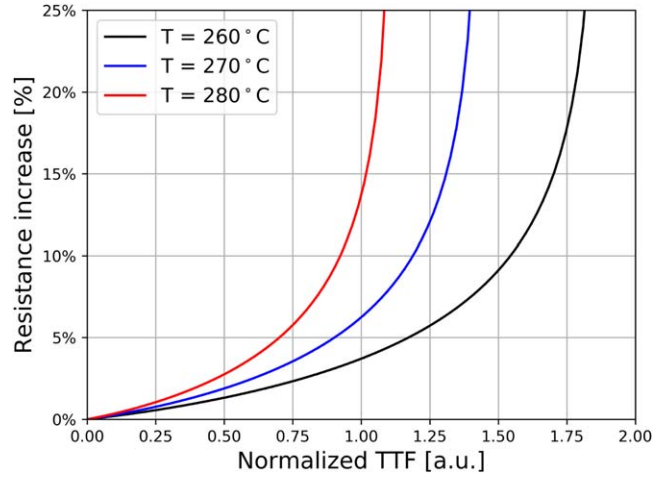


Figure 12. Resistance change for three different temperatures.

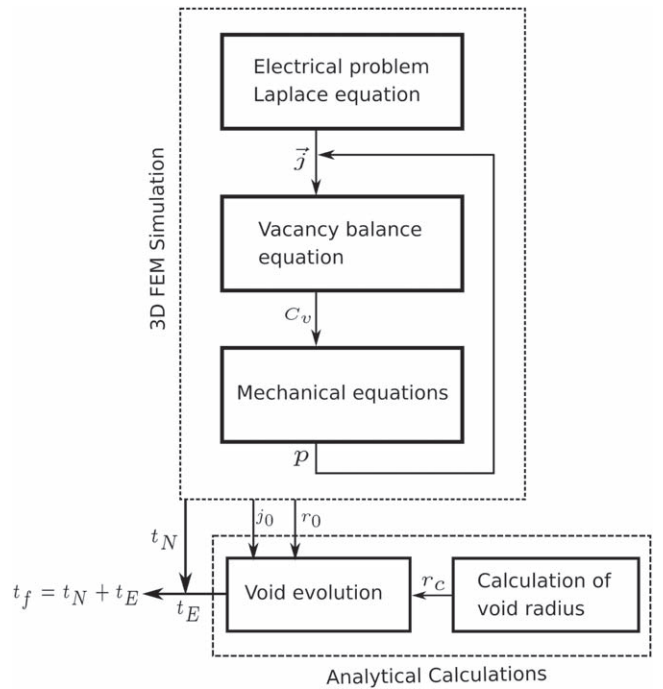
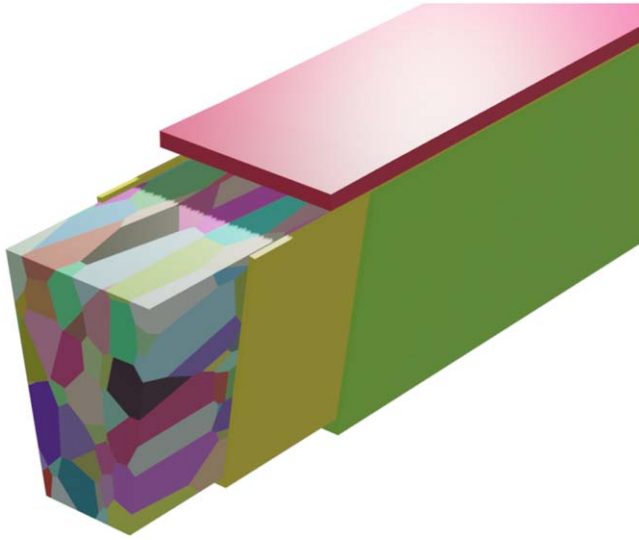


Figure 13. Overall two-part simulation scheme. The void nucleation time is determined in the “3D FEM Simulation” part and the void evolution time in the “Analytical Calculations” part.

distribution of the current density  $\vec{j}$  inside the metallization which is needed for solving the vacancy balance Eqs. 2 and 3. The solution of the vacancy balance equations determines the vacancy concentration,  $C_v$ , throughout the metal bulk. The redistribution of vacancies, driven by the EM and the accompanying driving forces, gives rise to mechanical stress, which is obtained by simultaneously solving Eqs. 5 and 6. The vacancy balance equation and the mechanical equations are solved in a time loop, until the critical stress is reached at some triple point at the capping layer. This event also marks the end of the 3D FEM part of the simulation flow. The results from the 3D FEM solution which are carried over to further processing are: the void nucleation time  $t_N$ , the current density  $j_0$ , and the radius of the initial void  $r_0$ . The current density  $j_0$  and the void radius  $r_0$  are needed for the calculation of the void evolution time. The critical void radius  $r_c$  is obtained by solving Eq. 28.





**Figure 14.** Polycrystalline Cu is wrapped from all sides except on the top with liner metals (green-TaN and yellow-Co). The top surface is covered by the SiCN etch-stop layer (red).

### Simulation Studies and Discussion

In this section we demonstrate the capability of the effective domain method through its application in study cases of reliability relevant for the down-scaling of modern nano-interconnects. The goal is, rather than to study some specific experimental results, to reproduce several major effects and features observed in a number of previous studies. The primary focus is on two effects: change of the failure time distribution due to the temperature variation and due to the reduced interconnect width. A particular emphasis is put on the role of microstructure.

The layer structure of a single interconnect line used for simulations is presented in Fig. 14. As a cap layer SiCN is used while liner consists of two layers, Co and TaN.<sup>6,14</sup>

In order to perform a detailed study in COMSOL Multiphysics<sup>38</sup> for each simulated interconnect line an artificial microstructure is generated by means of the effective domain method. As presented in Fig. 15 an artificial microstructure consists of alternate polycrystalline and large-crystal domains. Figure 16 shows a part of the geometry used as input for the COMSOL Multiphysics<sup>38</sup> simulation.

A single simulation run consists of simultaneously solving (2), (3), (5), and (6) on the geometrical domain of the interconnect line and estimating the void growth time by (27). The mechanical parameters and the diffusion coefficients used are taken from the previous publication.<sup>14</sup>

**Reproducing the microstructure by the effective domain method.**—Using the method presented above, for a straight interconnect defined by its widths  $w_T$ ,  $w_B$ , thickness  $h$ , and its total length  $L$ , a microstructure is generated as an array of alternate polycrystalline and single-crystal domains with lengths  $L_p$  and  $L_s$ , respectively (see Figs. 4 and 16). The values for  $L_p$  and  $L_s$  are generated according to the lognormal distribution with the mean length of polycrystalline domains  $m_p$ , the mean length of the single grain domains  $m_s$ , and the corresponding standard deviations,  $\sigma_p$  and  $\sigma_s$ .

**Impact of temperature on nano-interconnect failure.**—As presented above, in our concept the failure development is separated into two phases which are modeled by two distinctive approaches allowing for the estimation of the duration of each phase. The effective domain method is applied only for the first phase, which ends when a certain stress-threshold is reached at the interface between the metal and cap layer.<sup>14</sup> The site, where the stress-threshold is reached, is chosen as the site of the void nucleation. An

example of the peak stress dynamics at the capping layer interface for different microstructures is presented in Fig. 17.

For modeling of the second phase, which is the phase of the void growth, an analytical estimate for the growth time  $t_E$  is utilized. The interconnect fails, when a pre-defined increase of the interconnect resistance is reached. In this work, a resistance increase of 20% is used<sup>6,39</sup> as failure condition. The interconnect cross-section is defined by the following dimensions:  $h = 44$  nm,  $w_T = 24$  nm,  $w_B = 22$  nm, (see Figs. 14 and 15). The capping layer (SiCN) and liner (Co/TaN) are implemented utilizing the COMSOL-shell model<sup>38</sup> and the whole structure is embedded in a box of low- $k$  (ULK 2.5) dielectric.

As described above, an increased temperature affects the failure dynamics in several different ways. The most obvious one is due to the thermo-mechanics. Since the interconnect is heated from the stress-free temperature to the testing temperature, the mismatch of the thermal expansion coefficients causes thermo-mechanical stress. Furthermore, all diffusivities are thermally activated according to the Arrhenius law, leading to a more intense atomic transport at higher temperatures. Since a varying microstructure corresponds to a varying ratio of polycrystalline and large crystal domains, each with its own characteristic diffusivity, the failure times for a higher temperature are distributed similarly to the failure times for lower temperatures. However, the mean failure time decreases as the temperature increases. As we can see in Fig. 18, the simulation results clearly confirm this behavior which is also consistent with previous studies.<sup>6,14</sup>

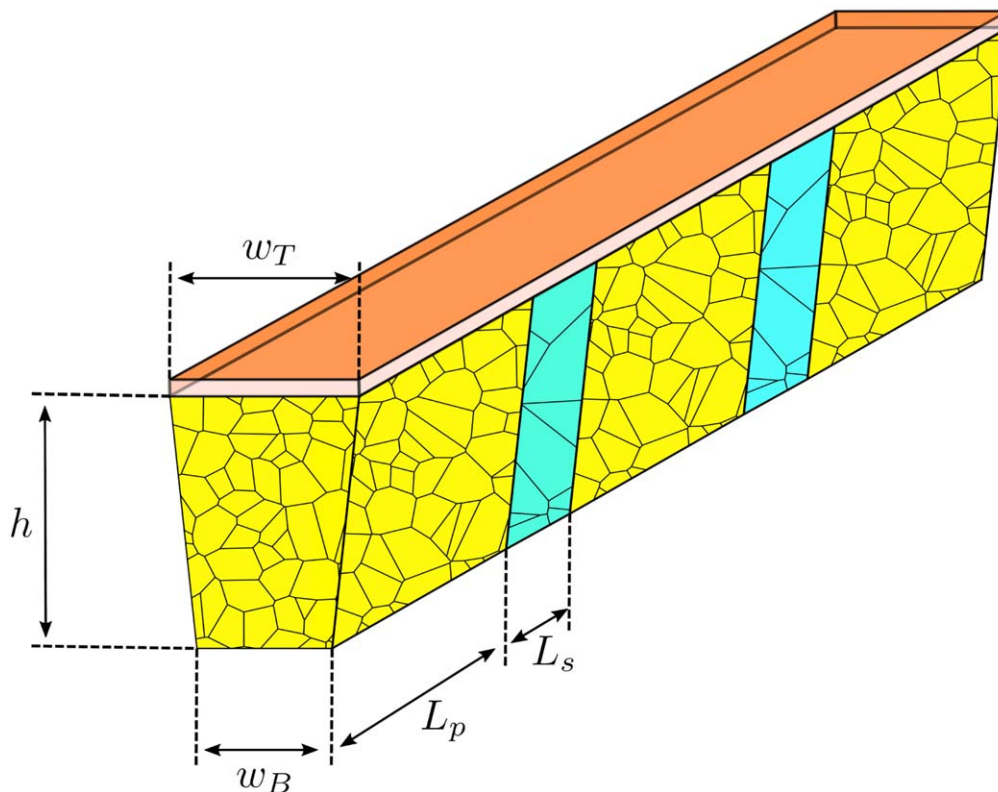
**Impact of nano-interconnect linewidth on failure.**—The effective domain method is also applied to investigate the impact of the nano-interconnect linewidth on the failure development and the nano-interconnect lifetime. As in the previous section, the simulations are performed for a set of different microstructures, generated and implemented into three different layouts (see Fig. 16). Each layout is scaled to accommodate interconnects with the average linewidths  $w = 23$  nm, 18 nm, and 11 nm ( $w = (w_T + w_B)/2$ ), respectively. The scaling behavior of the the mean length of the polycrystalline domains  $m_p$  and the mean length of the large grain domains  $m_s$  are set according to (20) with a constant standard deviation  $\sigma_{s,p} = 0.3$ .

With the chosen mean values and the standard deviation,  $L_p$  and  $L_s$  are generated according to the lognormal distribution. Subsequently,  $L_p$  and  $L_s$  are used as the lengths of the polycrystalline and large grain domains geometrically defined by the tilted cutting planes (Fig. 16). A tilt angle of 30° for all cutting planes and for all three considered interconnect linewidths is used. The tilt angle is a configurable parameter in the simulation and it may be optionally used also as a distributed value.

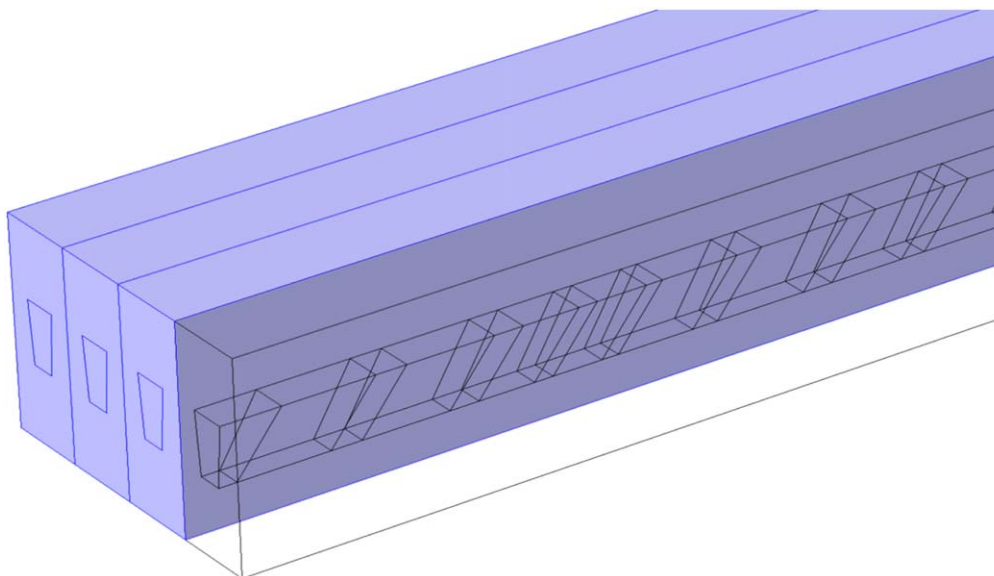
The material choice for the barrier, the cap layers and the dielectric are the same as in the study of the impact of temperature variations in the previous section.

When the interconnect linewidth is reduced, there are several circumstances which results in the reduction of its lifetime. The reduced linewidth leads to increased current densities, increased fraction of atoms migrating along the cap layer, and less time needed for a void to grow to its critical size. The change of the microstructural pattern for the reduced interconnect linewidth plays here a particular role.

As described above, the ratio of large crystal domains for a thinner interconnect generally reduces and, correspondingly, the ratio of polycrystalline domains increases. Consequently, the GBs becomes the dominant fast diffusivity path for atomic transport and thus for the interconnect degradation. As we can see in Fig. 19, there is a significant shift toward shorter interconnect lifetimes, when the linewidth is reduced. A similar behavior is observed in experiments, e.g., Choi and Christiansen et al.,<sup>3</sup> where for a number of layouts, a clear correlation between the interconnects' linewidths and their failure times was determined.



**Figure 15.** Schematic picture of an interconnect for the analysis with the effective domain method. The interconnect is divided into polycrystalline and large grain-domains, defined by their respective lengths,  $L_s$  and  $L_p$ .



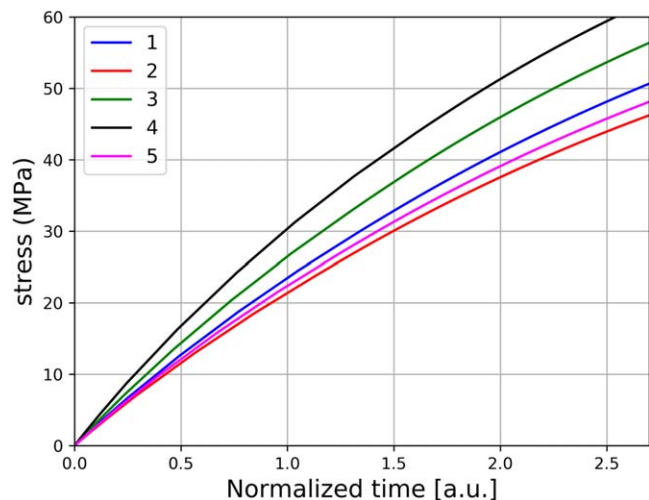
**Figure 16.** An example of an interconnect layout used in the simulations. The first structure to the right is made transparent so that the microstructure produced by the effective domain method is seen. The microstructure consists of alternate polycrystalline and single crystalline domains. The geometrical dimensions are given in Fig. 15.

### Application to New Interconnect Technologies

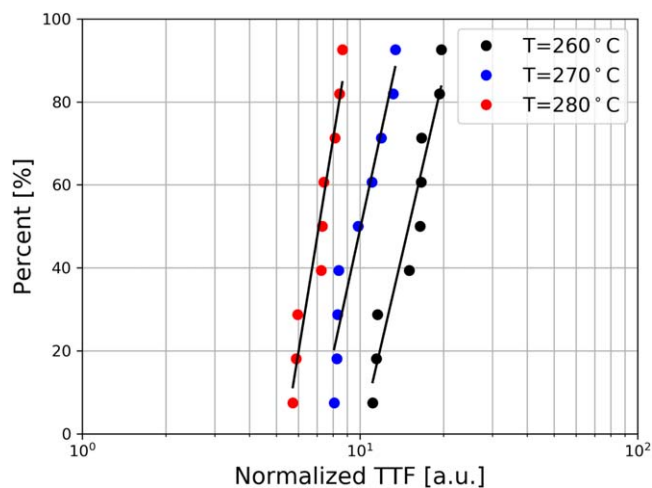
The effective domain method is readily applicable to a wide spectrum of modifications of Cu technology, such as introduction of new materials for cap layers and liners, changing interconnect dimensions, and process conditions. Furthermore, the effective domain method can also be utilized for interconnect technologies based on Cu-replacement metals such as Ru and Co. The framework provided by the effective domain method is independent of a

material choice, however, handling new materials demands a new set of configurational parameters which have to be extracted from experimental studies:<sup>40,41</sup>

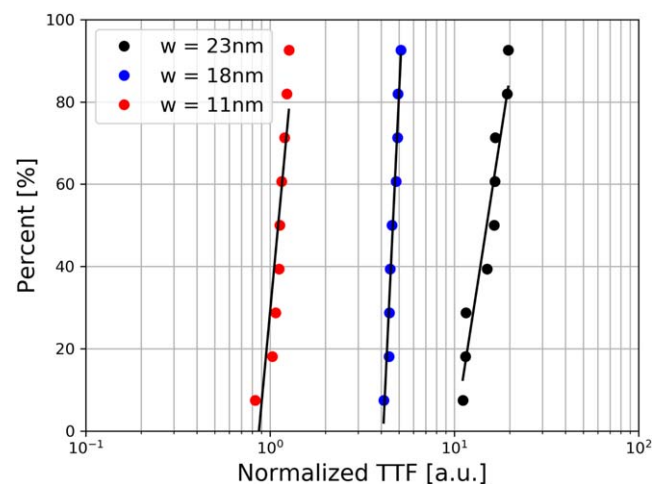
- Diffusion coefficients: Pre-exponentials and activation energies.
- Microstructural features: Statistical properties of grain size distribution.



**Figure 17.** Variation of stress-time dynamics for 5 different metal microstructures implemented by the effective domain method.



**Figure 18.** Failure behavior for  $T = 260\text{ }^{\circ}\text{C}$ ,  $270\text{ }^{\circ}\text{C}$ , and  $280\text{ }^{\circ}\text{C}$ . The black lines represent a linear fit to the data.



**Figure 19.** Impact of interconnect linewidth on the failure dynamics for three different interconnect linewidths. The black lines represent a linear fit to the data.

- Dependence of grain size distribution on interconnect line-width.

With these parameters, simulation and reliability analysis based on the effective domain method can target the specific degradation mechanisms for the given interconnect technology. A direct insight into how particular types of crystalline structure, resulting from a series of technology process steps, influence interconnect failure opens different possibilities for improvements of interconnect reliability.

## Conclusions

We have introduced a novel method, the effective domain method, to model the interconnect microstructure including major microstructural features relevant for modeling the physics of degradation. The effective domain method is used to generate large grain and polycrystalline regions inside a given interconnect geometry which approximates the real microstructure. By means of simulations based on a comprehensive three-dimensional EM model combined with the effective domain method, the impact of statistical microstructural features on the statistics of interconnect lifetime has been investigated. An important capability of the effective domain method is that it opens a path for studying the effect of reduced interconnect widths and increased temperatures on the interconnect reliability. In addition to the novel effective domain method, we have presented a numerically efficient method for estimating the void growth time. Both methods are useful for an assessment of the reliability of the various interconnect layouts or for developing and improving new ones. The simulations reproduce all key features and characteristics of published experimental results.

## ORCID

H. Ceric  <https://orcid.org/0000-0003-0918-7732>

## References

1. C.-K. Hu et al., "Mechanisms of electromigration damage in Cu interconnects." *Proc. International Electron Devices Meeting* 5.2.1 (2018).
2. K. Croes et al., "Interconnect metals beyond copper: Reliability challenges and opportunities." *Proc. International Electron Devices Meeting* 5.3.1 (2018).
3. S. Choi et al., "Effect of metal line width on electromigration of BEOL Cu interconnects." *Proc. International Reliability Physics Symposium* F.4.1 (2018).
4. E. Zschech, M. A. Meyer, S. G. Mhaisalkar, A. V. Vairagar, A. Krishnamoorthy, H. J. Engelmann, and V. Sukharev, "Effect of interface modification on EM-induced degradation mechanisms in copper interconnects." *Proc. International Conference on Materials for Advanced Technologies*, **504**, 279 (2005).
5. K. Croes, S. Demuynck, Y. K. Siew, M. Pantouvakis, Ch. J. Wilson, N. Heylen, G. P. Beyer, and Z. Tókei, "Full reliability study of advanced metallization options for 30 nm 1/2 pitch interconnects." *Microelectron. Eng.*, **106**, 210 (2013).
6. O. Varela Pedreira, K. Croes, H. Zahedmanesh, K. Vandersmissen, M. van der Veen, V. V. Gonzalez, D. Dictus, L. Zhao, A. Kolies, and Z. Tókei, "Electromigration and thermal storage study of barrierless Co vias." *Proc. International Interconnect Technology Conference*, 48 (2018).
7. J. R. Lloyd and K. P. Rodbell, "Reliability." *Handbook of Semiconductor Interconnection Technology*, ed. G. C. Schwartz and K. V. Srikrishnan (CRC Press, Boca Raton) p. 471 (2006).
8. A. O. Oates, "Strategies to ensure electromigration reliability of Cu/low-k interconnects at 10 nm." *ECS J. Sol. Stat. Sci. Techn.*, **4**, N3168 (2015).
9. L. Cao, P. S. Ho, and P. Justison, "Electromigration reliability of Mn-doped Cu interconnects for the 28 nm technology." *Proc. International Reliability Physics Symposium* EM.5.1 (2013).
10. M. H. Lin and A. S. Oates, "Electromigration in dual-damascene CuMn alloy IC interconnects." *IEEE Trans. Device Mater. Reliab.*, **13**, 330 (2013).
11. A. Joi, R. Akolkar, and U. Landau, "Pulse electrodeposition of copper-manganese alloy for application in interconnect metallization." *J. Electrochem. Soc.*, **160**, D3145 (2013).
12. H. Ceric, R. L. de Orio, J. Cervenka, S. Selberherr, A. J. Cervenka, and S. Selberherr, "A comprehensive TCAD approach for assessing electromigration reliability of modern interconnects." *IEEE Trans. Device Mater. Reliab.*, **9**, 9 (2009).
13. H. Ceric and S. Selberherr, "Electromigration in submicron interconnect features of integrated circuits." *Materials Science and Engineering R*, **71**, 53 (2011).
14. H. Ceric, H. Zahedmanesh, and K. Croes, "Analysis of electromigration failure of nano-interconnects through a combination of modeling and experimental methods." *Microelectron. Reliab.*, **100–101**, 113362 (2019).

15. M. E. Sarychev and Yu. V. Zhitnikov, "General model for mechanical stress evolution during electromigration." *J. Appl. Phys.*, **86**, 3075 (1999).
16. R. Rosenberg and M. Ohring, "Void formation and growth during electromigration in thin films." *J. Appl. Phys.*, **42**, 5671 (1971).
17. R. S. Sorbello, "Microscopic driving forces for electromigration." *Symposium K – Advanced Metallization for Future ULSI*, ed. L. J. Chen, J. W. Mayer, J. M. Poate, and K. N. Tu (Cambridge University Press, Cambridge) *MRS Online Proceedings Library*, 427, p. 73 (1996).
18. J. P. Dekker, A. Lodder, and J. van Ek, "Theory for the electromigration wind force in dilute alloys." *Phys. Rev. B*, **56**, 12167 (1997).
19. I. Ciofi et al., "Modeling of via resistance for advanced technology nodes." *IEEE Trans. Electron Devices*, **64**, 2306 (2017).
20. H. Ceric and H. Zahedmanesh, "Advanced modeling and simulation of Cu nano-interconnects reliability." *Proc. International Interconnect Technology Conference 1* (2019).
21. Ch. S. Hau-Riege, S. P. Hau-Riege, and A. P. Marathe, "The effect of interlevel dielectric on the critical tensile stress to void nucleation for the reliability of cu interconnects." *J. Appl. Phys.*, **96**, 5792 (2004).
22. N. Singh, A. F. Bower, D. Gan, S. Yoon, P. S. Ho, J. Leu, and S. Shankar, "Numerical simulations and experimental measurements of stress relaxation by interface diffusion in a patterned copper interconnect structure." *J. Appl. Phys.*, **97**, 135391 (2004).
23. Z.-S. Choi, R. Mönig, and C. V. Thompson, "Dependence of the electromigration flux on the crystallographic orientations of different grains in polycrystalline copper interconnects." *Appl. Phys. Lett.*, **90**, 1 (2007).
24. L. Arnaud, T. Berger, and G. Reimbold, "Evidence of grain-boundary versus interface diffusion in electromigration experiments in copper damascene interconnects." *J. Appl. Phys.*, **93**, 192 (2003).
25. K. E. Aifantis and S. A. Hackney, "Morphological stability analysis of polycrystalline interconnects under the influence of electromigration." *Rev. Adv. Mater. Sci.*, **19**, 98 (2009).
26. L. Filipovic, "A method for simulating the influence of grain boundaries and material interfaces on electromigration." *Microelectron. Reliab.*, **97**, 38 (2019).
27. S.-T. Hu, L. Cao, L. Spinella, and P. S. Ho, "Microstructure evolution and effect on resistivity for cu nanointerconnects and beyond." *Proc. International Electron Devices Meeting 5.4.1* (2018).
28. C.-K. Hu et al., "Mechanisms of electromigration damage in Cu interconnects." *Proc. International Electron Devices Meeting 5.2.1* (2018).
29. L. Spinella, T. Jiang, N. Tamura, J.-H. Im, and P. S. Ho, "Effect of scaling copper through-silicon vias on stress and reliability for 3D interconnects." *Proc. International Interconnect Technology Conference 80* (2016).
30. L. Spinella, T. Jiang, N. Tamura, J.-H. Im, and P. S. Ho, "Synchrotron X-ray microdiffraction investigation of scaling effects on reliability for through-silicon vias for 3-d integration." *IEEE Trans. Device Mater. Reliab.*, **19**, 568 (2019).
31. M. A. Meyer, I. Zienert, and E. Zschech, "Electron backscatter diffraction: application to cu interconnects in top-view and cross section." *Materials for Information Technology*, ed. E. Zschech, C. Whelan, and Th. Mikolajick (Springer, New York City) 485 (2005).
32. L. E. Spinella, "The scaling and microstructure effects on the thermal stress and reliability of through-silicon vias in 3d integrated circuits." *Dissertation*, The University of Texas at Austin (2017).
33. C. S. Smith, "Grain shapes and other metallurgical applications of topology." *Metallogr. Microstruct. Anal.*, **4**, 543 (1952).
34. J. J. Clement, "Electromigration modeling for integrated circuit interconnect reliability analysis." *IEEE Trans. Device Mater. Reliab.*, **1**, 33 (2001).
35. L. F. Fenton, "The sum of log-normal probability distributions in scatter transmission systems." *IRE Trans. Comm. Sys.*, **8**, 57 (1960).
36. V. Sukharev, A. Kteyan, E. Zschech, and W. D. Nix, "Microstructure effect on em-induced degradations in dual inlaid copper interconnects." *IEEE Trans. Dev. Mat. Rel.*, **9**, 87 (2009).
37. D. T. Walton, H. J. Frost, and C. V. Thompson, "Computer simulation of grain growth in thin film interconnect lines." *Mat. Res. Soc. Symp. Proc.*, **225**, 219 (1991).
38. COMSOL Multiphysics, Version 5.4. (2018).
39. H. Zahedmanesh, O. Varela Pedreira, C. Wilson, Z. Tőkei, and K. Croes, "Copper electromigration; prediction of scaling limits." *Proc. International Interconnect Technology Conference 1* (2019).
40. S. Beyne, O. Varela Pedreira, I. De Wolf, Z. Tőkei, and K. Croes, "Low-frequency noise measurements to characterize Cu-electromigration down to 44 nm metal pitch." *Proc. International Reliability Physics Symposium 1* (2019).
41. S. Beyne, O. Varela Pedreira, H. Oprins, I. De Wolf, Z. Tőkei, and K. Croes, "Electromigration activation energies in alternative metal interconnects." *IEEE Trans. Electron Devices*, **66**, 5278 (2019).