

## TWO-DIMENSIONAL MATERIALS

## Inorganic molecular crystals for 2D electronics

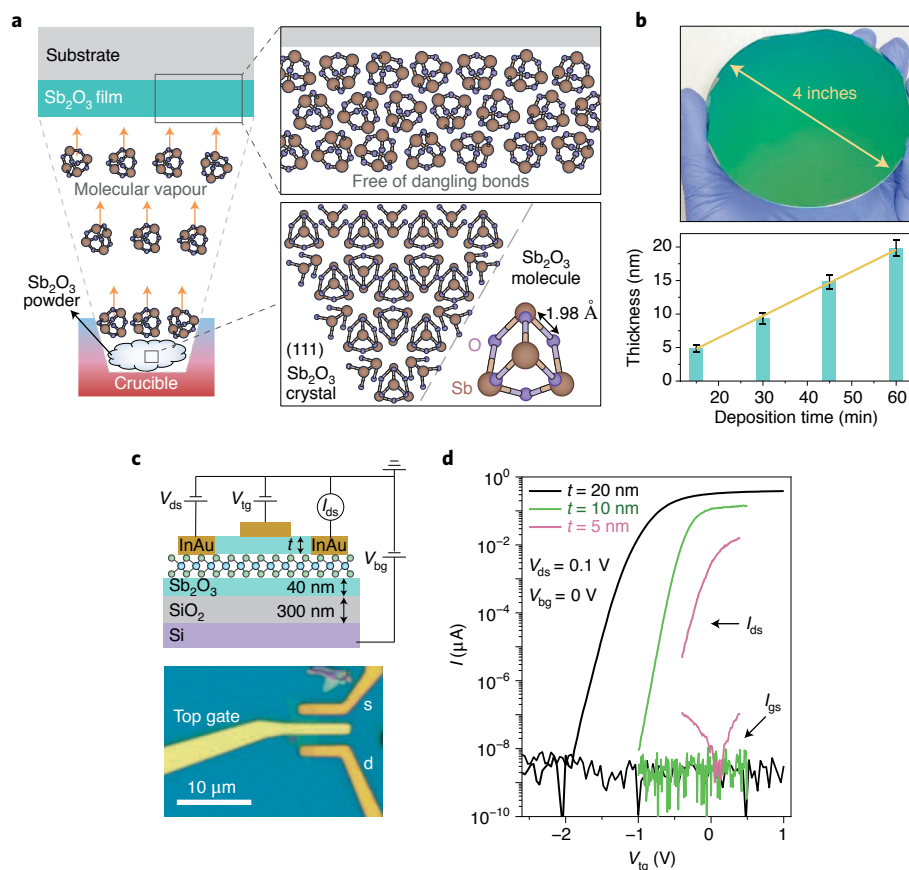
Inorganic molecular crystal films of antimony trioxide can be grown on 4-inch wafers via a thermal evaporation process and used as a top-gate oxide in two-dimensional molybdenum disulfide transistors.

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The digital logic circuit industry relies on silicon as a semiconducting material and complementary metal-oxide-semiconductor (CMOS) cells as elementary building blocks. Such silicon technology is, however, approaching its scaling limits<sup>1</sup>. This is owing to a drop in mobility at reduced channel thicknesses and to increasing short-channel effects at channel dimensions with physical gate lengths below 20 nm (corresponding to the 5-nm technology node and beyond)<sup>2</sup>. One potential solution is to use channels made of two-dimensional (2D) semiconductors<sup>3</sup> such as molybdenum disulfide (MoS<sub>2</sub>). With their atomic thinness, these materials can, in theory, overcome the scaling limits of silicon.

Considerable progress has been made in the fabrication of 2D devices in recent years, but challenges remain including the absence of competitive insulators. These insulators have to maintain low leakage currents when scaled down to below 1 nm equivalent oxide thickness (EOT; the thickness of SiO<sub>2</sub> that would result in the same capacitance as a certain thickness of an alternative insulator). They also have to form a well-defined interface with the channel, contain a low density of defects and have high dielectric stability. Amorphous oxides including silicon dioxide (SiO<sub>2</sub>), hafnium oxide (HfO<sub>2</sub>) and aluminium oxide (Al<sub>2</sub>O<sub>3</sub>) are widely used in silicon technology but have ill-defined interfaces and contain many defects. Crystalline hexagonal boron nitride (hBN) has previously been considered a promising alternative, but it exhibits high leakage currents at sub-1 nm EOT, which is prohibitive for low-power digital applications<sup>4</sup>. Writing in *Nature Electronics*, Kailang Liu, Tianyou Zhai and colleagues now show that an inorganic molecular crystal layer of antimony trioxide (Sb<sub>2</sub>O<sub>3</sub>) can be grown on 4-inch wafers using standard thermal evaporation deposition, and used as the top-gate oxide in field-effect transistors (FETs) with MoS<sub>2</sub> channels<sup>5</sup>.

This demonstration follows a series of exciting results on the development of insulators for 2D devices. First, sub-1 nm EOT crystalline calcium fluoride (CaF<sub>2</sub>)



**Fig. 1 | The development of MoS<sub>2</sub> FETs with Sb<sub>2</sub>O<sub>3</sub> insulators.** **a**, Schematic of standard thermal evaporation deposition of Sb<sub>2</sub>O<sub>3</sub> films from inorganic molecular crystal powder. **b**, Sb<sub>2</sub>O<sub>3</sub> film deposited on a 4-inch wafer (top), allowing for precise thickness control (bottom). **c**, Schematic layout (top) and optical image (bottom) of top-gated MoS<sub>2</sub> FETs with Sb<sub>2</sub>O<sub>3</sub> as a top-gate insulator and as a buffer layer at the back. **d**, The typical top-gate transfer characteristics of these devices with various thicknesses of Sb<sub>2</sub>O<sub>3</sub> and the corresponding gate leakage currents.  $V_{ds}$  drain voltage;  $V_{tg}$  top-gate voltage;  $V_{bg}$  back-gate voltage;  $I_{ds}$  drain current;  $I_{gs}$  gate leakage current;  $t$ , thickness of top-gate insulator; s, source; d, drain. Figure reproduced with permission from ref. <sup>5</sup>, Springer Nature Ltd.

was used as a gate insulator to create competitive MoS<sub>2</sub> FETs, although top-gated devices, which are required for circuit integration, were not reported<sup>6</sup>. Later, molecular crystal monolayers were used to passivate the interface between ultrathin HfO<sub>2</sub> and MoS<sub>2</sub> in top-gated devices<sup>7</sup>, but it remained unclear if the thickness of buffer

layers formed by discrete molecules could be large enough to block charge trapping by border traps<sup>8</sup> in the amorphous HfO<sub>2</sub> while maintaining the required EOT. Finally, top-gated FETs were fabricated via layer-by-layer oxidation of Bi<sub>2</sub>O<sub>3</sub>Se to its native oxide Bi<sub>2</sub>SeO<sub>5</sub> (ref. <sup>9</sup>); the approach created atomically sharp native

interfaces and thus led to excellent device performance, but the scaling potential of these devices requires further analysis considering the narrow bandgap (3.9 eV) of  $\text{Bi}_2\text{SeO}_5$ .

The approach developed by Zhai and colleagues can create  $\text{MoS}_2$  FETs using inorganic molecular crystal dielectrics that are grown via a scalable method and allow for top-gate integration. The researchers — who are based at Huazhong University of Science and Technology, Nanjing University of Science and Technology, Southern University of Science and Technology, Anhui University and Zhengzhou University — used a standard thermal evaporation process to deposit homogeneous  $\text{Sb}_2\text{O}_3$  films at room temperature, which enables large-scale integration on 4-inch wafers with a precise thickness control at a given growth rate (Fig. 1a,b). The films are van der Waals insulators with a narrow bandgap of 3.95 eV, but a decent dielectric constant of 11.5.

By using the films as buffer layers in back-gate insulator stacks,  $\text{MoS}_2$  FETs can be created that offer improved mobility and smaller hysteresis compared with devices using  $\text{SiO}_2$  as the back-gate oxide. The researchers fabricated top-gated  $\text{MoS}_2$  FETs with 5- to 20-nm-thick  $\text{Sb}_2\text{O}_3$  (EOT from about 1.6 nm to 6.6 nm) as a top-gate insulator (Fig. 1c). With a 10-nm-thick  $\text{Sb}_2\text{O}_3$  insulator (corresponding to an EOT

of 3.3 nm), the devices exhibited a near-ideal subthreshold swing of  $68 \text{ mV dec}^{-1}$  and a high on/off current ratio approaching  $10^8$  (Fig. 1d). They also performed a detailed study of hysteresis in their devices and found that it is small for sweep rates of several kiloseconds, which confirms the low defect density in crystalline  $\text{Sb}_2\text{O}_3$ .

Crystalline  $\text{Sb}_2\text{O}_3$  insulators can offer top-gate integration via direct deposition onto 2D channels at a low thermal budget, as well as large-area growth — these are key attributes for the development of industrial applications. However, similar to the native oxide  $\text{Bi}_2\text{SeO}_5$  (ref. <sup>9</sup>),  $\text{Sb}_2\text{O}_3$  has a narrow bandgap of about 4 eV. This could make it challenging to achieve a high on/off current ratio for sub-1 nm EOT, as suggested by the results for FETs with the thinnest  $\text{Sb}_2\text{O}_3$  films of 5 nm (EOT of 1.6 nm) in which sizeable gate leakage currents were observed (Fig. 1d). Also, the breakdown field obtained by Zhai and colleagues for 10-nm-thick  $\text{Sb}_2\text{O}_3$  is only  $2.7 \text{ MV cm}^{-1}$ , which is far lower than typical operating fields for nanoscale FETs (more than  $10 \text{ MV cm}^{-1}$ ) and might be related to the loose intramolecular van der Waals bonding within the  $\text{Sb}_2\text{O}_3$  layer. Further work is required to better understand the scaling potential of  $\text{Sb}_2\text{O}_3$ , paying particular attention to gate leakage currents and the dielectric strength at sub-1 nm EOT. Nevertheless, the successful

use of  $\text{Sb}_2\text{O}_3$  films as gate insulators in  $\text{MoS}_2$  FETs could prove to be beneficial in the development of sensors, optoelectronics and other applications of 2D materials that do not require aggressive thickness scaling and operation at high electric fields, but would benefit from the simplicity of the growth method and the high-quality van der Waals interface formed by this inorganic crystalline insulator. □

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Published online: 21 December 2021  
<https://doi.org/10.1038/s41928-021-00691-w>

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#### Competing interests

The authors declare no competing interests.