Efficient Modeling of Charge Trapping at Cryogenic Temperatures—Part II: Experimental

Jakob Michl*, Alexander Grill*, Member, IEEE, Dominic Waldhoer**, Wolfgang Goes, Ben Kaczer*, Dimitri Linten, Senior Member, IEEE, Bertrand Parvais*, Bogdan Govoreanu, Senior Member, IEEE, Iuliana Radu*, Tibor Grasser*, Fellow, IEEE, and Michael Waltl*, Member, IEEE

Abstract—We present time-zero characterization and an investigation on bias temperature instability (BTI) degradation between 4 and 300 K on large area high-κ CMOS devices. Our measurements show that negative BTI (NBTI) on pMOSFETs freezes out when approaching cryogenic temperatures, whereas there is still significant positive BTI (PBTI) degradation in nMOSFETs even at 4 K. To explain this behavior, we use an efficient implementation of the quantum mechanical nonradiative multiphonon charge trapping model presented in Part I and extract two separate trap bands in the SiO₂ and HfO₂ layer. We show that NBTI is dominated by defects in the SiO₂ layer, whereas PBTI arises mainly from defects in the HfO₂ layer, which are weakly recoverable and do not freeze out at low temperatures due to dominant nuclear tunneling at the defect site.

Index Terms—4 K, 28-nm bulk CMOS, advanced CMOS, bias temperature instability (BTI), cryoelectronics, cryogenic, physical modeling.

I. INTRODUCTION

Bias temperature instability (BTI) [1], [2] is one of the main reliability issues in modern MOSFET technologies. Pre-existing or created defects in the insulator or the interface layer are responsible for the BTI degradation. Several defect candidates, such as oxygen vacancies [3], [4], hydrogen bridges [5]–[7], or hydroxyl E’ centers [8], have been identified, which can trap and release charges during operation. In addition, the creation of silicon dangling bonds at the Si/SiO２ interface has been demonstrated as a critical contribution to the degradation [9]. The trapped charges cause a shift in the threshold voltage, which can lead to a failure at the circuit level. Thus, obtaining a physical understanding of the charge trapping mechanisms is essential to predict the impact of BTI on different technologies.

Typically, BTI measurements are performed under accelerated conditions by using elevated stress voltages and temperatures. Since we focus on cryogenic environments, an increase in device temperature is not feasible, and instead, elevated stress voltages are used in this work. There are various applications in astronomy [10] or quantum computing [11], [12] that operate at cryogenic conditions and require high stability. One of the main limiting factors for realizing quantum computers with the capability to solve “real-world” problems is the quantum–classical interface (QCI) [13]. A large number of readout and control components are needed between the qubits and a classical computer for successfully running quantum algorithms and performing error correction protocols.

The manuscript received July 15, 2021; revised September 24, 2021; accepted September 28, 2021. Date of current version December 1, 2021. This work was supported in part by imec’s Industrial Affiliation Program on Quantum Computing and Cryoelectronics, in part by the Austrian Research Promotion Agency FFG (Take off Program) under Project 861022 and Project 867414, in part by the European Union’s Horizon 2020 Research and Innovation Program within the framework of the project Modeling Unconventional Nanoscaled DeviceFABrication (MUNDFAB) under Grant 871813, in part by the Austrian Federal Ministry for Digital and Economic Affairs, in part by the National Foundation for Research, Technology and Development, and in part by the Christian Doppler Research Association. The review of this article was arranged by Editor E. A. Gutiérrez-D. (Corresponding author: Jakob Michl.)

Jakob Michl, Dominic Waldhoer, and Tibor Grasser are with the Institute for Microelectronics, TU Wien, 1040 Vienna, Austria (e-mail: michl@iue.tuwien.ac.at).
Alexander Grill, Ben Kaczer, Dimitri Linten, Bogdan Govoreanu, and Iuliana Radu are with imec, 3001 Leuven, Belgium.
Wolfgang Goes is with Silvaco Europe Ltd., Cambridge PE27 5JL, U.K.
Bertrand Parvais is with imec, 3001 Leuven, Belgium, and also with the ETRO Department, Vrije Universiteit Brussels, 1050 Brussels, Belgium.
Michael Waltl is with the Christian Doppler Laboratory for Single Defect Spectroscopy, Institute for Microelectronics, TU Wien, 1040 Vienna, Austria.
Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3117740.
Digital Object Identifier 10.1109/TED.2021.3117740.

the interface layer are responsible for the BTI degradation. Several defect candidates, such as oxygen vacancies [3], [4], hydrogen bridges [5]–[7], or hydroxyl E’ centers [8], have been identified, which can trap and release charges during operation. In addition, the creation of silicon dangling bonds at the Si/SiO₂ interface has been demonstrated as a critical contribution to the degradation [9]. The trapped charges cause a shift in the threshold voltage, which can lead to a failure at the circuit level. Thus, obtaining a physical understanding of the charge trapping mechanisms is essential to predict the impact of BTI on different technologies.
To minimize coherence loss due to large temperature gradients, the QCI should be integrated inside the high-vacuum stage of the cryostat [12]. Thus, it is necessary to evaluate the reliability over longer periods of time of the used CMOS technologies at cryogenic temperatures.

There are several publications focusing on the time-zero characteristics [14]–[17]; however, for a safe application, also the reliability of the CMOS devices needs to be guaranteed. Recent publications show that even in cryogenic environments reliability issues, such as random telegraph noise (RTN) [18], [19], hot carrier degradation (HCD) [20], and BTI [21], occur. For predicting the impact of these degradation mechanisms during the lifetime of the devices, a physical understanding of the charge transfer mechanisms is necessary. As we showed in Part I [22], using nonradiative multi-phonon (NMP) theory [23], charge trapping does not freeze out toward cryogenic temperatures but rather becomes dominated by nuclear tunneling. We have already demonstrated preliminary results regarding positive BTI (PBTI) degradation on nMOS devices [21]. In the following, we will present both negative BTI (NBTI) and PBTI extended measure-stress-measure (eMSM)-measurement data (see Fig. 1) between room temperature and 4 K and show how these measurements can be explained and efficiently modeled with a quantum mechanical charge trapping model.

II. EXPERIMENTAL SETUP AND SIMULATION

For our BTI measurements, we used large-area n-type and p-type 28-nm bulk CMOS high-k devices with dimensions $W \times L = 10 \mu m \times 10 \mu m$ and a metal gate. A HfO$_2$ layer is processed on top of a rapid thermal oxidation SiO$_2$ interfacial layer, resulting in an equivalent oxide thickness of about 1.41 nm.

A. Measurements

For the characterization of the electrostatics and the BTI degradation, measurements between 4 and 300 K were conducted on a manual Lakeshore CRX-4K cryogenic probe station using a custom-built defect probing instrument [24], which has an optimized signal-to-noise ratio and provides a logarithmic sampling scheme to record measurement data for a long period without any accuracy lost.

1) Characterization: First, the temperature dependence of some important device characteristics were measured, as can be seen in Figs. 2 and 3 for nMOS and pMOS devices, respectively. In (a), the transfer characteristics in the linear regime ($|V_{DS}| = 10 mV$) are shown for temperatures varied between 4 and 300 K with steps of 25 K. It can be clearly seen that toward low temperatures, the transfer characteristic becomes steeper and the ON-current increases. This is due to reduced electron–phonon scattering at lower temperatures, leading to higher charge mobilities [14]. Therefore, the transconductance increases at lower temperatures, as can be seen in (c). Figs. 2(b) and 3(b) show the subthreshold swing, which does not follow the Boltzmann theoretical limit, but starts saturating below approximately 100 K. This feature has been seen across various technologies and has been explained by band-tail tunneling at interface defects [17]. In Figs. 2 and 3(d), the increasing threshold voltage is shown with two different definitions: either defined at a constant current $|I_{cc}| = 1 \mu A$.
or at the point of maximum transconductance. Depending on the definition, the exact values of the threshold voltage differ, however, both absolute values increase at $T \to 4$ K due to the temperature-dependent bulk Fermi level [16], [25].

2) eMSM Measurements: For the characterization of BTI degradation, we apply the eMSM scheme [26], as shown in Fig. 1. After measuring the initial $I_S(V_G)$ curve, the measured device is first stressed by applying a gate stress bias $V_{G,s}$ for a stress time $t_s$. After that, a recovery voltage $V_{G,r}$ in the linear regime is applied for a certain recovery period $t_r$. During the recovery phase, the source current $I_S$ is recorded, which is more stable against oxide degradation compared to $I_D$ [26]. Using the initial $I_S(V_G)$, the source current can be mapped to a threshold voltage shift $\Delta V_{th}$. These alternating stress and recovery cycles are then repeated for increasing stress times and recovery times. The following stress and recovery times have been used: $(t,S,t_D) \in \{[10 \mu s, 10 s], (1 ms, 100 s), (100 ms, 100 s), (10 s, 1 ks), (1 ks, 10 ks)\}$. During stress, a gate voltage of $|V_{G,s}| = 2$ V and $|V_{D,s}| = 25$ mV was applied.

During the stress phases, pre-existing defects in the oxide and at the interface can become charged, which leads to a shift in the $I_S(V_G)$ curve and thus changes the threshold voltage. During the recovery phase, on the other hand, the defects can emit the captured charges, which can be seen as an increase in the measured source current $I_S$. The typical transients of $I_S$ and $\Delta V_{th}$ are indicated in the bottom of Fig. 1. While the source currents in the recovery phase can be measured directly, during stress, $\Delta V_{th}$ can only be estimated from on-the-fly measurements [27] or determined from simulations.

B. Simulation

For the simulation of the measured eMSM sequences, we use our 1-D BTI simulator Comphy [28]. After calibration of the electrostatics of the device, the simulator computes the surface potential for a given gate voltage $V_G$. Employing a two-state nonradiative multiphonon model [23], the capture and emission rates of pre-existing oxide defects can be computed and subsequently can be used to explain the observed transient $\Delta V_{th}$.

As discussed in detail in Part I [22], the classical NMP charge transition rate freezes out toward cryogenic temperatures. Thus, the exponential approximation, which holds in the high-temperature limit, needs to be replaced by the full quantum mechanical transition rate. Since the computation of this full quantum mechanical transition rate is computationally expensive, we use our efficient WKB approximation suitable for TCAD device simulation developed in Part I [22].

The potential energy surfaces of the charged and uncharged defect can be assumed to be parabolic within the harmonic approximation, as shown in Fig. 4. For the computation of the classical capture and emission barriers $\epsilon_{ij}$ and $\epsilon_{ji}$, it is necessary to find the intersection point of the two parabolas, which are typically described by three Huang–Rhys parameters [29]: the energetic offset $\Delta E$, the relaxation energy $E_R$, and the ratio of the curvatures $R$. Since the classical transition rate only depends on the barrier height, the distance between the minima of the potential energy surfaces does not need to be considered. However, in the full quantum mechanical treatment as well as the employed WKB-approximation, the configuration coordinate (CC) difference $\Delta Q$ is crucial. Here, $\Delta Q$ determines the overlap integral $|I_{in,1β}|^2$, which becomes relevant in the nuclear tunneling regime.

Typically, it is assumed that the experimental data can be reproduced by placing trap bands in the oxide, e.g., by assuming normally distributed trap levels and relaxation energies as well as spatially uniform defect distribution across the oxide. Therefore, a trap band can be characterized by the following parameters: $(E_T, \sigma_{E_T}, (E_R), \sigma_{E_R}, x_T, \Delta Q, \text{ and } N_T)$. These parameters need to be calibrated to the experimental dataset by using an optimization algorithm for all defect bands. This process is typically very time consuming and the resulting parameters can be very sensitive to the choice of the initial guess. Therefore, we employ our recently developed effective single defect decomposition (ESiD) method to extract the defect parameters [30]. Using this method, defects are sampled on a predefined grid over $E_T, E_R, x_T$ and $\Delta Q$ and the response of the defects is compared to the measured eMSM sequence. For every $(E_T, E_R)$-grid point, the mean response over all $x_T$ and $\Delta Q$ is computed and used to reduce the 4-D grid to a 2-D grid. Thus, the eMSM sequence can be described as a superposition of defects with different trap levels and relaxation energies, where the obtained coefficients are proportional to the respective trap densities. To avoid artificially high defect densities and to get smooth defect distributions, the ESiD scheme uses a Tikhonov term regularization [31].

The used grid parameters are shown in Table I.

III. RESULTS AND DISCUSSION

The measured $\Delta V_{th}$ shifts for the sequences described in Section II-A2 can be seen in Fig. 5 (circles) for temperatures between $T = 4$ and $300$ K. When comparing the PBTI traces of the nMOS device (upper panel) and the NBPTI traces of the pMOS device (lower panel), it is remarkable that PBTI does not freeze out, whereas NBPTI freezes out completely.
TABLE I
INITIAL GRID PARAMETERS OF THE ESiD OPTIMIZATION FOR A SHALLOW AND A DEEP TRAP BAND IN BOTH THE SiO2 LAYER AND THE HfO2 LAYER

<table>
<thead>
<tr>
<th>Layer</th>
<th>$E_T$ range</th>
<th>$\Delta E_T$</th>
<th>$E_R$ range</th>
<th>$\Delta E_R$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO2</td>
<td>-2 to 2 eV</td>
<td>0.1 eV</td>
<td>0.1 to 5.0 eV</td>
<td>0.2 eV</td>
</tr>
<tr>
<td>HfO2</td>
<td>-2 to 2 eV</td>
<td>0.1 eV</td>
<td>0.1 to 5.0 eV</td>
<td>0.2 eV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Layer</th>
<th>$\tau_T$ range</th>
<th>$\Delta \tau_T$</th>
<th>$\Delta Q$ range</th>
<th>$\Delta Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO2</td>
<td>0.1 nm</td>
<td>0.1 nm</td>
<td>2.0 to 5.0 $\sqrt{\text{A}}$</td>
<td>1.0 $\sqrt{\text{A}}$</td>
</tr>
<tr>
<td>HfO2</td>
<td>1.0 to 3.1 nm</td>
<td>0.1 nm</td>
<td>2.0 to 5.0 $\sqrt{\text{A}}$</td>
<td>1.0 $\sqrt{\text{A}}$</td>
</tr>
</tbody>
</table>

Fig. 5. $\Delta V_{th}$ transients at temperatures between $T = 4$ and 300 K for nMOS and pMOS devices using a logarithmic time scale starting at 1 ms. The nMOS device shows a large $\Delta V_{th}$ shift even at $T = 4$ K, whereas $\Delta V_{th}$ of the pMOS freezes out completely at cryogenic temperatures. This behavior can be understood using quantum mechanical transition rates and trap bands generated with our ESiD algorithm. (a) nMOS (PBTI). (b) pMOS (NBTI).

Fig. 6. Freeze-out behavior of BTI in the nMOS and pMOS devices shows an asymmetric behavior. The threshold voltage shift of the pMOS devices is negligible for temperatures below $T = 150$ K, whereas the nMOS device shows a large $\Delta V_{th}$ shift even at $T = 4$ K. (a) pMOS (NBTI). (b) nMOS (PBTI).

Fig. 7. Extracted distributions of the relaxation energies $E_R$ (top) and the trap levels $E_T$ (bottom) are shown. The histograms are normalized to $N_{tot} = 1.11 \times 10^{17} \text{ cm}^{-3}$, the largest extracted defect density of the shallow HfO2 electron trap band. All extracted trap bands show peaks at low relaxation energies.

Fig. 8. Extracted $(E_T, E_R)$ maps show that hole traps (red) are distributed over a wide range up to 1 eV below the Si valence band edge. Electron traps (blue) are mostly located near the Si conduction band edge and show relaxation energy peaks at low $E_T$, around $E_R = 2.5$ eV (HfO2) and $E_R = 4.5$ eV (SiO2). Device Fig. 6(b) is almost twice as high for the same stress conditions. In contrast to the pMOS device, the nMOS device shows a threshold voltage shift of $\Delta V_{th} = 25$ mV even at $T = 4$ K.

The above findings can only be explained consistently within a QM model, as the classical approach would always lead to a freeze-out. To demonstrate this, an efficient WKB approximation of the full QM NMP model was implemented in our device simulator Comphy. The resulting theoretical $\Delta V_{th}$ curves are in excellent agreement with the experimental data, as shown in Fig. 5 (lines). Using the ESiD algorithm, we obtain trap bands that are not bound to any specific distribution. The trap levels $E_T$ for hole and electron traps together with their corresponding relaxation energies $E_R$ are shown in Fig. 7. For both hole and electron traps, it is assumed that there are two independent trap bands: one trap band in the high-$\kappa$ layer HfO2 and one trap band close to the SiO2–Si interface. We remark that the relaxation energies extracted using the ESiD algorithm are smaller compared to previous works [28]. This is a consequence of fixing the curvature when approaching low temperatures. This is highlighted in Fig. 6 where $\Delta V_{th}$ after different increasing stress times $t_s$ for different temperatures is shown. For the pMOS device in Fig. 6(a), $\Delta V_{th}$ is approximately zero for temperatures below $T = 150$ K, independent of the stress time $t_s$. At $T = 300$ K, a threshold voltage shift of approximately $\Delta V_{th} = 35$ mV is measured. Compared to that, $\Delta V_{th}$ measured on the nMOS device Fig. 6(b) is almost twice as high for the same stress conditions. In contrast to the pMOS device, the nMOS device shows a threshold voltage shift of $\Delta V_{th} = 25$ mV even at $T = 4$ K.
Fig. 9. Total threshold voltage shift of the nMOS device is composed of $\Delta V_{th}$ from defects in the SiO$_2$ layer and defects in the HfO$_2$ layer. Defects in the HfO$_2$ layer dominate the slowly recoverable part of the threshold voltage shift, while the recovery is dominated by defects in the SiO$_2$ layer. (a) $T = 300$ K. (b) $T = 4$ K.

Fig. 10. Threshold voltage shift per defect of an nMOS device. At room temperature (left), the threshold voltage shift is caused by electron traps in both the SiO$_2$ layer and the HfO$_2$ layer. At cryogenic temperatures, the main contribution of $\Delta V_{th}$ is caused by defects in the HfO$_2$ layer, which have large recovery times, whereas only a small recoverable contribution is caused by defects in the SiO$_2$ layer.

Fig. 11. Threshold voltage shift per defect of a pMOS device. At $T = 300$ K (left), the main contribution of the threshold voltage shift $\Delta V_{th}$ is caused by defects in the SiO$_2$ layer. These defects freeze out toward $T = 4$ K as can be seen in the right panel.

Fig. 12. Exemplary active defect in an nMOS with the configuration coordinate (CC) diagram at the right shows both stress and recovery condition low classical barriers. As a consequence at cryogenic temperatures, the overlap of the ground state (indicated with solid lines in the CC diagram) with the corresponding wave function in the final state is large and transitions at 4 K are within the measurement window.

Fig. 13. Compared to active defects in the nMOS as shown in Fig. 12, the classical barriers in pMOS are higher due to the given $(E_T, E_R)$ distributions. As a consequence, the overlaps of the ground state with the corresponding wave function are smaller compared to the exemplary defect in nMOS, and thus, the corresponding time constants are outside the measurement window at low temperatures.

The distribution of the relaxation energies and the corresponding trap levels are plotted in a $(E_T, E_R)$ heat map shown in Fig. 8. Acceptor-like defects that are responsible for PBTI are dominated by traps in the HfO$_2$ layer above the Si bandgap. Donor-like defects that dominate the NBTI degradation are close to the valence band edge.
Using the extracted trap bands, it is possible to compare the impact of each trap band on the total threshold voltage shift. This can be seen for the nMOS device in Fig. 9 for $T = 300$ K (top) and $T = 4$ K (bottom). At $T = 300$ K, the main contribution of the threshold voltage shift within our measurement window arises from the traps in the HfO$_2$ layer; in contrast, defects in the SiO$_2$ layer show a stronger recovery. In addition, the SiO$_2$ layer contains very fast defects, which recover immediately ($t_c < 100$ $\mu$s) after removal of the stress voltage. At $T = 4$ K, both defects in the HfO$_2$ layer and defects in the SiO$_2$ contribute almost equally to the total threshold voltage shift and both defect bands show very weak recovery. The described mechanisms are illustrated for the nMOS device in Fig. 10. The color indicates the threshold voltage shift, after a stress of $V_{G} = 2$ V for $t_s = 1$ ks (i.e., blue defects deliver a large contribution to the total $\Delta V_{th}$ and gray defects give a small contribution). In addition, defects that recover immediately after removal of the stress are represented by stars. At $T = 300$ K (left), defects in the HfO$_2$ layer give a larger contribution to the total $\Delta V_{th}$ than defects in the SiO$_2$ layer. In contrast to the HfO$_2$ layer, the SiO$_2$ layer contains many defects that recover immediately. These defects are not active at $T = 4$ K, and at this temperature, defects in the SiO$_2$ layer and the HfO$_2$ layer contribute equally to the total shift.

The same analysis of the impact of each trap band was done for the pMOS device. As shown in Fig. 11, after applying a stress $V_{G} = -2$ V for $t_s = 1$ ks at $T = 300$ K (left), the main contribution to the threshold voltage shift arises from defects in the SiO$_2$ layer. These defects have transition rates, which freezes out toward $T = 4$ K, so that pMOS devices show no NBTI at cryogenic temperatures.

The impact of trap level ($E_T$) and relaxation energy ($E_R$) distributions on the recovery transients is shown exemplarily in Figs. 12 and 13 for two active defects in nMOS and pMOS devices, respectively. Compared to the donor-like trap in the pMOS, the acceptor-like trap in the nMOS has a lower classical barrier (for both stress and recovery). Thus, in the classical limit, capture and emission times will be smaller, and hence, the threshold voltage shift in nMOS devices is larger, which is in agreement with the measured transients in Fig. 5. At cryogenic temperatures, capture and emission times are dominated by the ground state. For the ($E_T$, $E_R$) parameter combinations shown for nMOS in Fig. 12, the overlap of the ground state is considerably larger than in the pMOS scenario in Fig. 13 because the distance of the two exponential decays of the wave functions is larger (compared to part I). Thus, the acceptor-like nMOS defect is still active at 4 K, whereas the donor-like pMOS defect has very high capture and emission times.

The time constants corresponding to the active defects in Figs. 12 and 13 are specifically highlighted in the ensemble of all other defects in Fig. 14. The majority of time constants of the nMOS is lower than for the pMOS, which results in active defects in nMOS devices even at 4 K, while the time constants of defects in the pMOS device have moved outside of the measurement window.

**IV. Conclusion**

Large-area n-type and p-type, 28-nm bulk CMOS devices were characterized between $T = 4$ and 300 K. Afterward, PBTI on the nMOS device and NBTI on the pMOS device were characterized using the eMSM scheme. The measured threshold voltage shifts show that NBTI completely freezes out while approaching cryogenic temperatures, whereas there is still significant PBTI measured at $T = 4$ K. In order to explain this asymmetry, we implemented a WKB approximation of the full quantum mechanical charge transition rate in our device simulator Comphy, which allows the computation of transition rates at very low temperatures, where the frequently used classical approximation is no longer applicable, as we demonstrated in Part I [22]. We automatically extracted a shallow and a deep trap band in both the SiO$_2$ and the HfO$_2$ layers of the device using our novel ESiD scheme [30]. By analyzing the impact of each trap band on the total threshold voltage shift, we showed that NBTI is dominated by defects in the deep SiO$_2$ layer. These defects completely freeze out at cryogenic temperatures. On the other hand, PBTI is composed of responses in the HfO$_2$ layer, which are weakly recoverable and responses of fast defects in the SiO$_2$. 
layer, which dominates the recovery. The asymmetric freeze-out behavior of nMOS and pMOS devices results from the different distribution of the trap levels $E_T$ and the relaxation energies $E_R$.

REFERENCES


