Localizing Hot-Carrier Degradation in Silicon Trench MOSFETs

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***Abstract*— Hot-carrier degradation (HCD) is investigated in silicon trench MOSFETs with field plate compensation. With the aid of charge pumping (CP), it is possible to obtain the total trap densities created by the hot-carrier stress. We will demonstrate that, in combination with TCAD simulations, profiling of the spatial distribution of the damage at the interface is possible in the accessible regions by extending the well-known reverse-bias CP method for planar devices to trench devices. Four process variations are investigated to show the impact of the cell geometry on the degradation location with the results being confirmed by capacitance measurements. It is found that the impact ionization rate seen in drift-diffusion TCAD simulations provides a straightforward means to estimate the defect locations.**

***Index Terms*— Charge pumping (CP), dual-poly MOSFET, hot carrier degradation (HCD), MOSFET, reliability, silicon, trench MOSFET, U-shaped notch MOS field-effect transistor (UMOSFET).**

I. Introduction

HOT-CARRIER degradation (HCD) has been a highly relevant reliability problem since the 1980s [1] and is a major degradation mechanism of the Si–SiO_2 interface of MOS structures. While HCD has been thoroughly studied for lateral MOSFETs during those 40 years [1]–[3], much less is known for trench structures, especially for more complex cells, such as field plate (FP)-compensated devices, where the FP allows for performance improvements compared to conventional trench MOSFETs [4]. The major advantage of using trench devices in contrast to lateral MOSFETs is the considerable increase in packing density. Adding an FP connected to the source electrode increases the drain–source breakdown voltage by inducing a negative electric field into the drain region, thereby smoothing the fields of the body-drain p-n junction. As a consequence, the field peaks necessary for inducing avalanche breakdown are shifted to higher drain–source voltages. This allows for higher doping and, thus, lower ON-resistance of the structure compared to an uncompensated trench FET. Naturally, these complex field distributions raise questions about the nature of HCD in these cell geometries. While there are a few studies of HCD on these special devices [5], so far, the location of defects created by hot-carrier stress (HCS) in such structures is not well known. Our goal is to improve the understanding of HCD for these FP-compensated structures to understand the limits of the device in case of misuse outside its safe operating area. We achieved this by developing a measurement approach based on the charge pumping (CP) method [6], which, in principle, allows for the quantitative spatial profiling of defects to pinpoint the hot-carrier damage. Comparing experimental results to TCAD simulations, we also check if the results of a drift-diffusion calculation (electric field distribution and impact ionization rates) are suitable for the prediction of the location of Si–SiO_2 interface degradation without having to resort to more complicated physics-based TCAD HCD models [7].

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II. Structures and Measurement Procedure

We use FP-compensated trench Si-MOSFETs of a 25-V class (see Fig. 1) with an SiO_2-filled trench in all experiments. The gate and FP electrodes consist of highly doped polycrystalline Si buried in oxide with a thickness on the order of around 40 nm, while source and drain are connected with metal contacts. Using the FP electrode, which can be arbitrarily biased in our special test structures, we are able to manipulate the field constellations in the cell. Thus, we are able to manipulate the fields during HCS and, therefore, overstress the device to create large degradation on which our measurement method can be tested.

We use four geometry variations for our dedicated test structures: the reference P1, a device with a lower gate base point (P2) (see Fig. 1), and a structure with a deeper trench (P3). Finally, P4 corresponds to a combination of P2 and P3 (lower gate base point and a deeper trench). Each device consists of 263 parallel trenches.

The worst case conditions for HCD in long-channel lateral MOSFETs are usually around a gate voltage of $V_G \approx V_D/2$ [8]. Due to the fundamentally different geometry, this relation is not applicable to trench devices. We stress our devices at $V_D = 20$ V and $V_G = 2$ V as our devices are designed as power MOSFETs where high electric fields between drain and source required for HCD conditions can only be reached at such low gate voltages. In order to vary the location of the degradation on the interface, we apply an FP bias of $V_{FP} = 10$ V or $V_{FP} = 0$ V (the latter being the

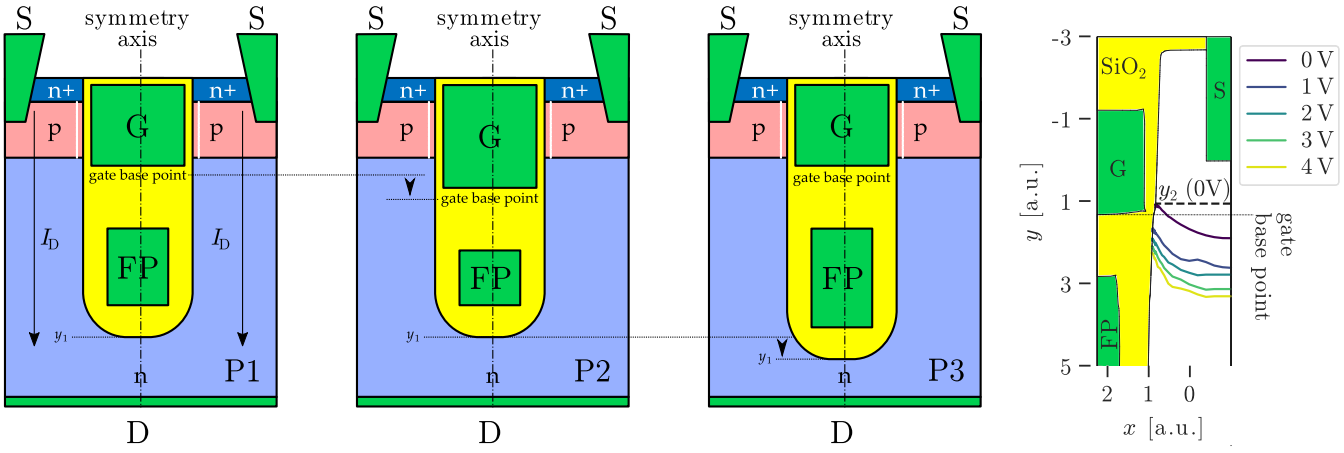

Fig. 1. Visualization of the FP-compensated trench MOSFET, where "*G*" is the gate electrode, "FP" the FP electrode, "*S*" the source, and "*D*" the drain. The channel is represented as a white line in the left three figures. P1–P3 represent three major process variations investigated. A simulation of a more realistic structure is shown in the right figure, where the border of the SCR in the drain region is drawn for various drain biases at $V_G = 0$ V and $V_{FP} = 20$ V. The position of y_1 is at $y = 9$.

potential during regular operation), while the source contact acts as ground potential. Although a positive bias on the FP is not representative for the ON-state of these devices, where the FP is usually hardwired to the source, we use the FP potential to emulate a compensated trench MOSFET where the electric field constellations cause a localized degradation near the gate base point by design. It is noted that the aforementioned stress condition already stresses the devices disproportionately much compared to normal operation. Without these harsh conditions, we would not have been able to create significant amounts of traps resulting in convincing HCD data within a reasonable measurement window. We rule out bias temperature instability components because, according to TCAD simulations, the electric fields in the vicinity of the Si–SiO_2 interfaces do not exceed 1 MV/cm.

HCS-induced defects can be accurately characterized with the CP method [6], [9] where the electrode of an MOS structure is pulsed between full inversion and full accumulation. For fast slopes, charges trapped in defects during the accumulation phase cannot emit during accumulation and recombine with carriers near the interface in the inversion phase and vice versa. This causes a measurable CP current I_{CP} proportional to the trap density between n-doped and p-doped regions of the semiconductor. Instead of using the gate, we apply the CP pulse to the FP electrode, as described in [10]. The quantitative localization of the defects is achieved by extending the lateral profiling technique of CP [11] by TCAD simulations where the location of the space charge region (SCR) border at the Si–oxide interface is mapped to the drain voltage [$y_2(V_D)$; see Fig. 1 (right)] for each of our structures. The position of the SCR border at various drain voltages is visualized in Fig. 2 (left) for the device P1. When CP is done via the FP (see Fig. 3), increasing drain voltages causes a shift of the SCR in the drain region toward the bottom of the trench during the accumulation phase of the pulse ($V_{FP} = 20$ V). Within the SCR, i.e., above its border along with the Si–SiO_2 interface, the important CP condition of full accumulation cannot be fulfilled. Hence, the areas along

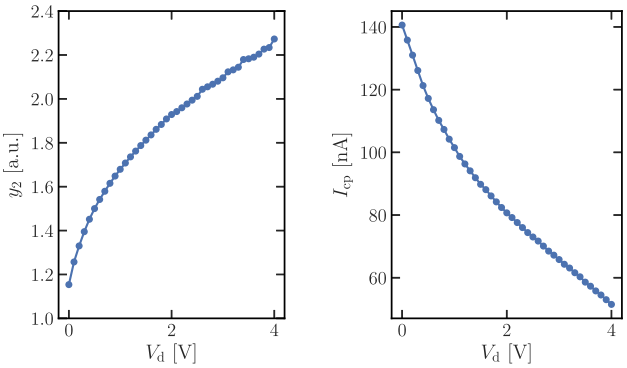

Fig. 2. Intermediate steps for the calculation of the localized trap density. Left: transformation of reverse-bias voltage to the SCR position at the Si–SiO_2 interface. Right: CP current dependence on the reverse-bias voltage.

the interface covered by an SCR cannot contribute to I_{CP}, thereby resulting in a reduction. Using the position of the SCR border $y_2(V_D)$, quantitative localized profiling is possible by adaption of the CP relation [9]

$$N_t = \frac{I_{CP}}{f q A} \tag{1}$$

which describes the relationship of the CP current I_{CP} and the trap density N_t. In our case, $A = W(y_1 - y_2)$ is the active CP area, where W is the sum of the width of all trenches, y_2 the position of the border of the SCR directly at the interface, and y_1 the position of the bottom of the trench [see Figs. 1 and 2 (left)]. f is the CP frequency and q the elementary electron charge.

In order to quantify the local trap densities, it is necessary to investigate the number of traps $N_t A = I_{CP}/fq$

$$\frac{I_{CP}}{fq} = \int_{z_1}^{z_2} \int_{y_1}^{y_2(V_D)} n_t(y) \mathrm{d}y \mathrm{d}z. \tag{2}$$

The z-axis in (2) represents the third depth dimension in Fig. 1, which is not shown in the respective perspective.

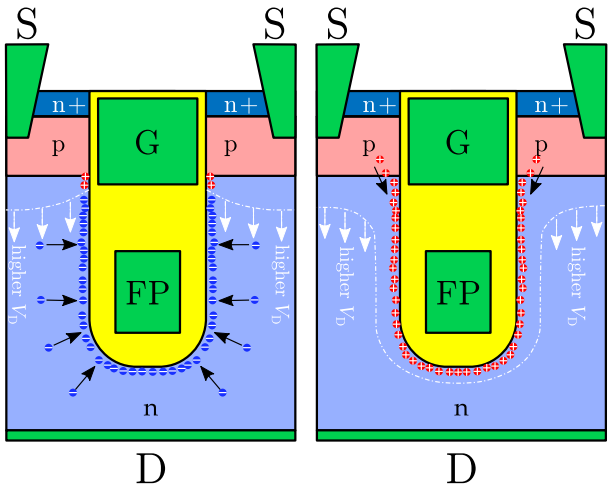

Fig. 3. Schematic illustration of the CP effect in trench devices. The dashed-dotted line represents the border of the SCR in the drain region. Left: positive FP voltage, i.e., electron accumulation at the trench interface. Electrons are attracted from the drain region. Right: negative FP voltage, i.e., hole inversion at the trench interface. Holes are provided from the p-doped body region.

It corresponds to the width extension of the trenches and is another symmetry axis. Therefore, the differential localized trap density $n_t(y_2)$ only depends on the y-axis, which is assumed to align with the interface. Since the CP current stems from the sum of all trenches, the integral over the z-dimension can be replaced by W

$$W \int_{y_1}^{y_2(V_D)} n_t(y)\mathrm{d}y = \frac{I_{\mathrm{CP}}}{fq}. \tag{3}$$

Differentiating (3) with respect to y_2 yields

$$n_t(y_2) = \frac{\mathrm{d}I_{\mathrm{CP}}(y_2)}{\mathrm{d}y_2}\frac{1}{fqW} \tag{4}$$

which can be evaluated using the mapping of the drain reverse-bias to the respective positions y_2 on the trench interface. Since all y_2 data points originate from discrete V_D steps, numerical algorithms, such as the Savitzky–Golay filter, can be used for obtaining a smooth derivative $\mathrm{d}I_{\mathrm{CP}}(y_2)/\mathrm{d}y_2$. A typical characteristic of the CP current and drain bias, which is the raw data needed for this transformation, is shown in Fig. 2 (right).

Equation (1) can be used for the definition of the mean trap density

$$\overline{N}_t(y_2(V_D)) := \frac{I_{\mathrm{CP}}(V_D)}{fqW(y_1 - y_2)}. \tag{5}$$

This quantity describes an average trap density along the trench between $y_2(V_D)$ and the trench bottom y_1. While the trap distribution along the trench is generally not uniform, the parameter can be used to quantify the average increase in degradation after stress.

The samples from all process variations were stressed for 1 h, and readouts of $n_t(y_2)$ and $\overline{N}_t$ were taken for various drain voltages. In addition, C–V measurements were performed using the gate and the FP contacts. In these C–V measurements, the target electrode voltage was swept, while all other contacts were grounded.

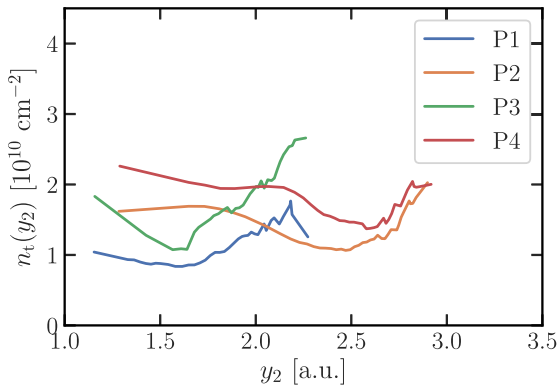

Fig. 4. Trap densities of the virgin device. The y-coordinate uses the same units as in Fig. 1. Localized trap density of virgin devices for the four process variations around the gate base point as per (4).

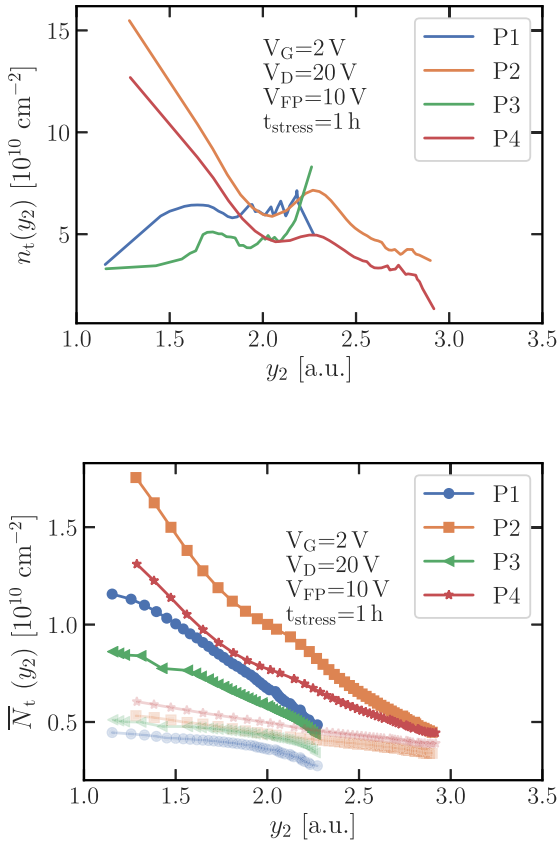

Fig. 5. Trap densities after an HCS with an FP bias of $V_{\mathrm{FP}} = 10$ V. The y-coordinate uses the same units as in Fig. 1. Top: localized trap density after HCS for the four process variations around the gate base point. Bottom: mean trap density in the trench below the respective coordinate y after stress [see (5)]. The virgin mean trap density curves are plotted with a lower transparency.

III. Results

In the unstressed devices, all process variations show a slightly increased trap density around the gate base point (see Fig. 4) compared to the mean densities, which mainly includes contributions of traps near the trench bottom (see Fig. 5 (bottom), low transparency). This is most likely caused by the sharp corner in the trench wall at the gate base point where the gate oxide transitions into the FP oxide. This geometric imperfection is prone to additional initial defects.

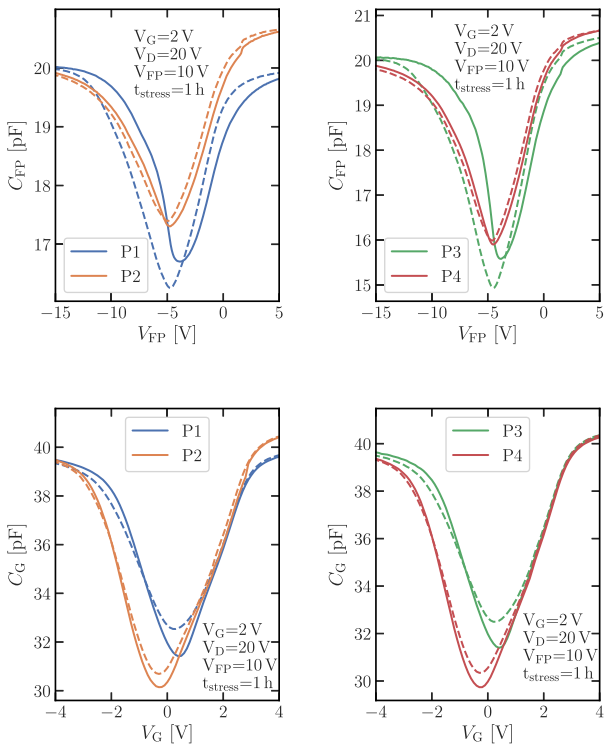

Fig. 6. Capacitance before and after an HCS with an FP bias of V_{FP} = 10 V. Dashed lines represent the virgin device and full lines the stressed device. Top: FP capacitance. Bottom: gate capacitance.

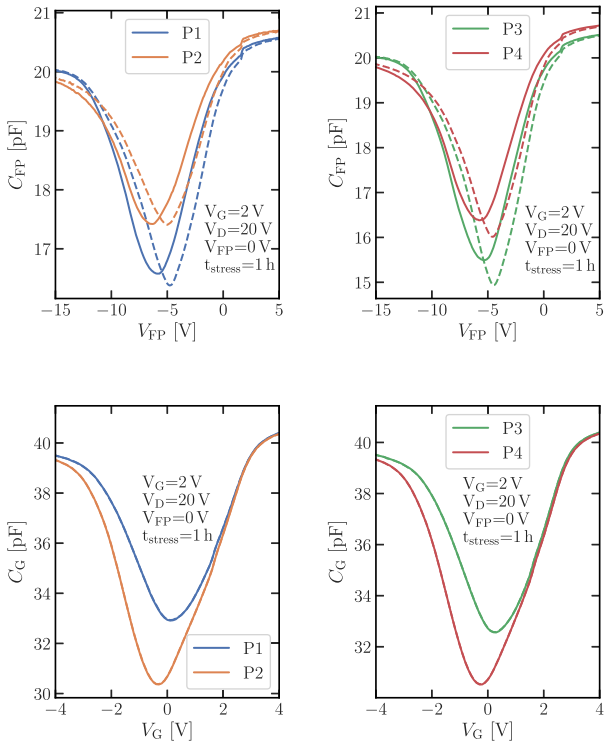

Fig. 7. Capacitance before and after an HCS with an FP bias of V_{FP} = 0 V. Dashed lines represent the virgin device and full lines the stressed device. Top: FP capacitance. Bottom: gate capacitance; dashed and full lines overlap.

After the stress with an FP voltage of 10 V, a significant increase in the defects is observed near the gate base point [see Fig. 5 (top)]. This raise of the trap density rapidly abates

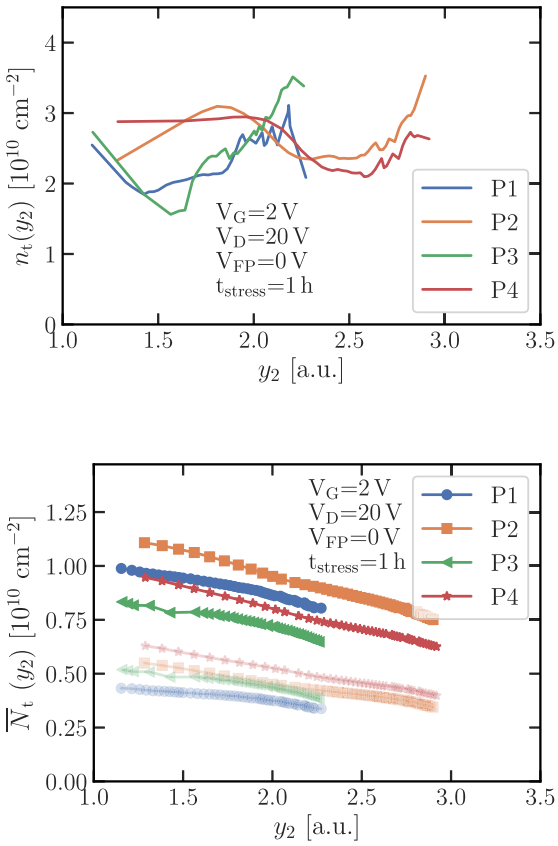

Fig. 8. Trap densities after an HCS with an FP bias of V_{FP} = 0 V. The y-coordinate uses the same units as in Fig. 1. Top: localized trap density after stress for the four process variations around the gate base point. Bottom: mean trap density in the trench below the respective coordinate y after stress [see (5)]. The virgin mean trap density curves are plotted with a lower transparency.

toward the trench bottom until the devices reach almost virgin levels [see Fig. 5 (bottom)]. It is noted that although the localized degradation seems constant for P1 and P3, the value is approximately five to ten times higher than the mean trap densities. This strong localization of all device variations of the interface damage is mainly caused by the high positive bias on the FP.

Capacitance measurements on gate and FP qualitatively confirm the trap location information gained from CP measurements. The change of FP and gate capacitance after stress are shown in Fig. 6, respectively. Since the FP electrode was chosen for the CP investigation, which successfully profiled the degradation, it was expected that the FP capacitance would also be influenced by the stress. The major increase in trap density near the gate base point found in CP is reflected in the change of the gate capacitance. If no defects had been present near the gate base point, the gate capacitance would not have changed as the field of the gate cannot influence the surface potential at low positions of the trench. The presence of negative capacitance changes is an indication that the whole C–V curves are shifted after stress due to the charge of the defects itself.

We also investigated all devices after stress with no FP voltage instead of 10 V which showed an insignificant change of the gate capacitance [see Fig. 7 (bottom)] after stress.

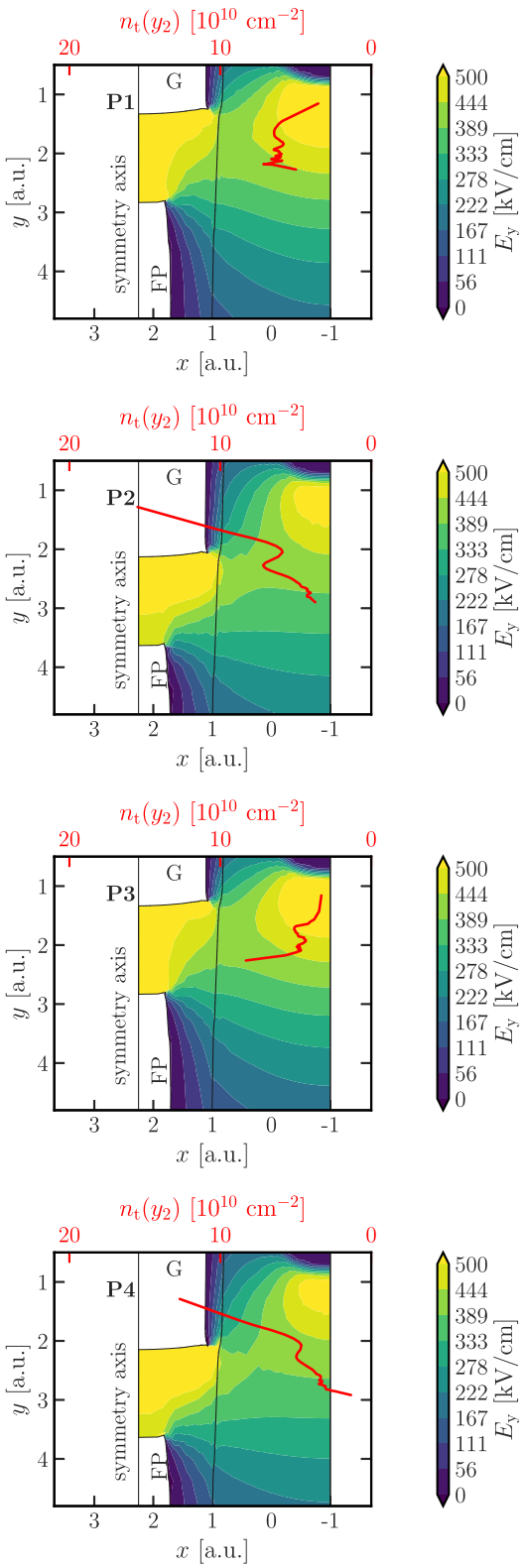

Fig. 9. Simulation of the y-component of the electric field for the process variations P1–P4 (top to bottom) under HCS conditions (V_{FP} = 10 V). The top *x*-axis represents the localized trap density after stress, as shown in Fig. 5 (top). The y-coordinate uses the same units as in Fig. 1.

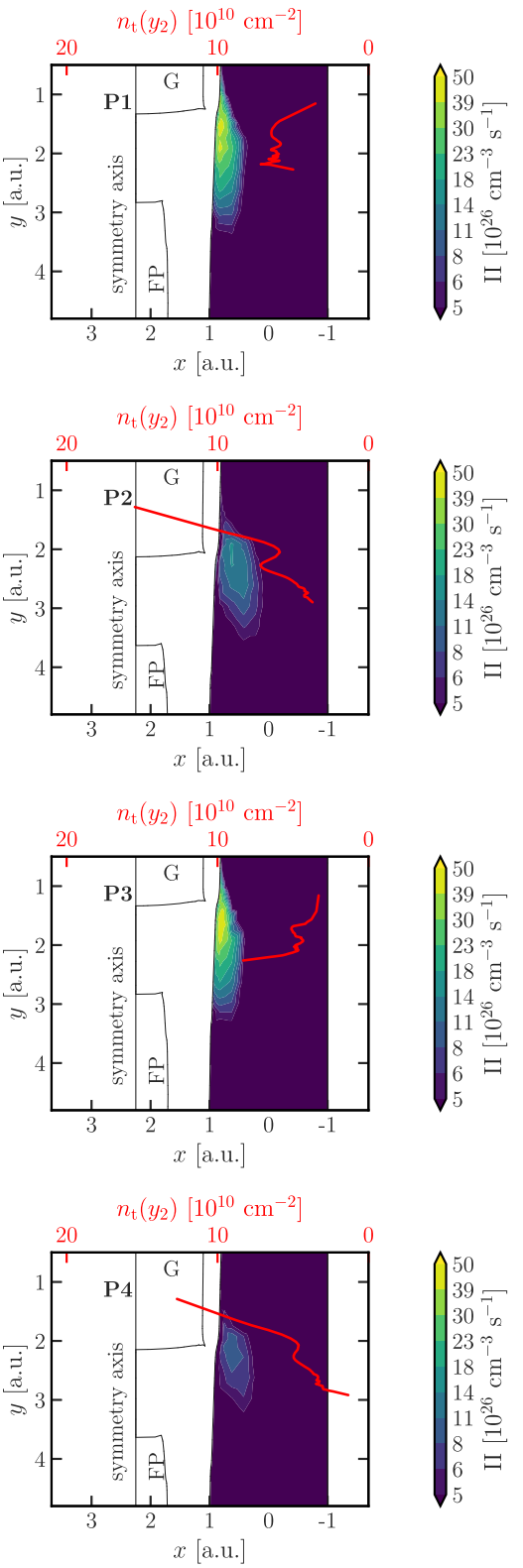

Fig. 10. Simulation of the impact ionization rate for the process variations P1–P4 (top to bottom) under HCS conditions (V_{FP} = 10 V). The top *x*-axis represents the localized trap density after stress, as shown in Fig. 5 (top). The y-coordinate uses the same units as in Fig. 1.

This was consistent with an increase in the mean trap density without a disproportional change of the localized trap density (see Fig. 8) and a significant change of the FP capacitance (see Fig. 7 top). As expected, the FP voltage plays a major role in the location of HCD since the electric fields are indirectly responsible for the HCD effect. Therefore, in addition to

traditional criteria in the design of the FP compensation principle, such as the breakdown voltage, HCD must be considered.

It is noted that the change of the gate and FP capacitance is only a qualitative indicator. Quantitative correlations of capacitance changes and trap densities are not possible since the localized degradation has a nonlinear impact on the capacitance. Furthermore, geometric variations strongly influence the capacitance characteristics. Thus, as is the case in our experiments, some geometries may not be as sensitive to capacitance changes after HCS-induced damage as others. For example, the gate capacitance of device P3 changes significantly after an HCS at 10-V FP voltage but hardly after stress at 0-V FP voltage even though the mean trap density increases are comparable at the first glance. As previously mentioned, a closer look at the local trap densities near the gate base point reveals that, for the stress at 10-V FP voltage, the localized trap density near the gate base point is higher than at 0 V.

Comparing the results of the localized CP trap profiling [see Fig. 5 (top)] after HCS at $V_{\mathrm{FP}} = 10$ V to TCAD simulations allows for analyzing the predictability of HCD in these complex structures. Fig. 9 shows results of the simulation of the y-component of the electric field E_y, which is approximately parallel to the Si–SiO_2 interface. The electric field has long been used as an indicator for the location of HCD [12] in lateral MOSFETs although it was shown to only approximate the true position [13]. In our devices, E_y seems to fit well for the geometric variants P1 and P3 where the gate does not reach as far into the drain region as in P2 and P4 but only vaguely resembles the true stress location in P2 and P4. A better candidate for the prediction of the HCD location is the impact ionization rate, obtained from TCAD. TCAD simulations at an FP voltage of 0 V show negligible magnitudes around the gate base point consistent with the observation of uniform degradation. On the other hand, at an FP voltage of 10 V during HCS conditions, the impact ionization predicts the defect location in all of our process variations and seems to pinpoint the location better than E_y (see Fig. 10), and the magnitudes of the degradation cannot be predicted at all. Generally, this observation is consistent with previous results, showing that simple drift diffusion models are not able to model the complex physics [14] involved in HCD and can only be used as general guidance for more detailed investigations. Without better physical models, our experimental approach is an easy alternative to profiling interface damage.

IV. Conclusion

We investigated HCD in FP-compensated trench MOSFETs. In order to pinpoint the location of the degradation, we introduced an extension for the well-known CP spatial profiling method that uses the p-n junction SCR to vary the active CP area. This variation is achieved by applying a drain–source voltage during the CP experiment. We use TCAD simulations to quantitatively map the locations of the SCR to drain biases and present a simple mathematical framework to transform CP currents at various drain voltages into localized and mean trap densities. After stress, all devices where an FP bias of 10 V was applied show significant changes of the trap density near the gate base point, while the mean trap density near the trench bottom is only insignificantly influenced. For an FP potential of 0 V, the mean trap density increases constantly at all positions, suggesting a uniform degradation of the device. These results are qualitatively confirmed by capacitance measurements at the FP and gate electrode. In a TCAD approach, two output quantities, the y-component of the electric field E_y and the impact ionization rate, were screened for their predictability of the spatial distribution of HCS-induced defects. While the electric field does not provide a good fit, the impact ionization rate may allow for better localization of the HCD damage, albeit being incorrect in the magnitude of the degradation due to nonlocal effects.

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