On the Distribution of Single Defect Threshold Voltage Shifts in SiON Transistors

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***Abstract*—To improve MOS transistors operating characteristics, such as the switching speed and power consumption, the dimensions of integrated devices are continuously decreased, amongst other advances. One of the main drawbacks of geometry scaling is the increased variability of the threshold voltage between nominally identical devices. The origin for this lies in defects located inside the oxide and at the interfacial layer between the oxide and the semiconductor. At the same time, the number of defects becomes a countable quantity in devices approaching the tens of nanometer scale. Furthermore, their impact on the device performance significantly increases, in a way that charge transitions from single defects can be observed directly from electrical measurements. To describe the degradation of the devices caused by single defects, one has to investigate the distribution of their impact on the V_{th} shift. For SiON technologies, uni-modal exponential distributions of step heights of single defects have been reported in the literature. However, our results reveal that the step heights are more likely bi-modal exponential distributed. These findings are essential for the accurate evaluation of the tail of the distribution, i.e., the defects showing an enormous impact on ΔV_{th}. Such defects can give rise to an immediate failure of devices and circuits. In this study, the statistical distributions of the effect of single defects are created and analyzed. We compare the results to values calculated using the commonly applied charge sheet approximation (CSA) and show that the CSA significantly underestimates the real impact of the defects for the studied technology. Finally, we use the obtained distributions and analyze their effect on the variability of measure-stress-measure simulations using our compact physical modeling framework.**

***Index Terms*—SiON nanoscale devices, single oxide defects, positive and negative bias temperature instability (PBTI, NBTI), complementary cumulative distribution function (CCDF).**

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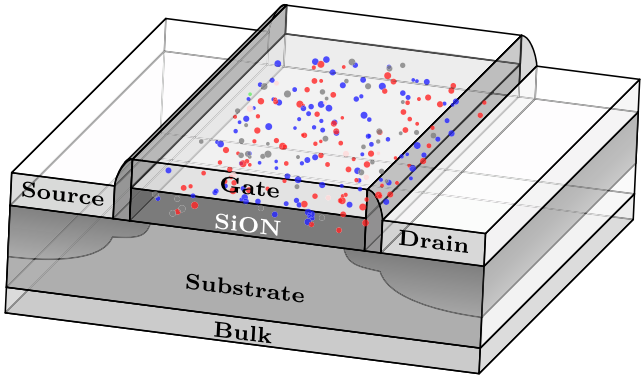

Fig. 1. Schematic of a MOS transistor with indicated defects. Defects located within the device (oxide traps and interface states) affect the reliable operation of transistors. Electron traps (blue) and hole traps (red) can be examined when nanoscale devices are employed. Taken from [7].

I. Introduction

SINGLE defects located inside the oxide and at the oxide/semiconductor interface of a MOS transistor, see Figure 1, can affect the absolute value of its threshold voltage V_{th}. Furthermore, as the charge state of such defects can change under operation, a drift of the threshold voltages can be observed, denoted as ΔV_{th} [1], [2]. This reliability issue is typically referred to as Bias temperature instability (BTI), which is classified regarding the sign of the applied gate bias. The positive BTI (PBTI) is commonly investigated employing nMOS devices, while negative BTI (NBTI) refers to negative applied gate biases and is typically studied for pMOS devices [3]–[6]. To analyze BTI, the drain-source current through a transistor is measured after the devices have been stressed at high gate biases while the drain, source and bulk terminals are grounded. The respective experiments are mostly conducted at elevated temperatures. In this case, the defects exhibit shorter charge capture and emission times and can thus become charged considerably faster compared to experiments conducted at room temperature. The so measured drift of the current ΔI_{D} is commonly expressed in terms of ΔV_{th} using the initial $I_{\text{D}}(V_{\text{G}})$ characteristics of the device.

The experiments are typically conducted at large-area devices [8], [9], where a continuous drift of the ΔV_{th} can be measured. However, to extract the impact of single defects on the device behavior, it is necessary to use scaled devices with dimensions of a few tens of nanometers. In such devices, the charge transitions of defects can be observed as discrete steps in the ΔV_{th} data, which can

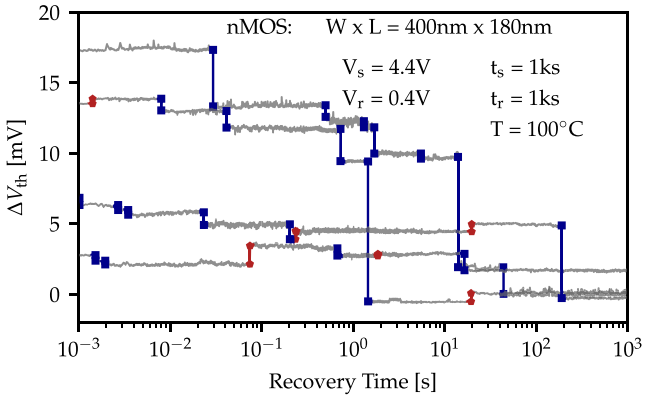

Fig. 2. Selected recovery traces showing the drift of the threshold voltage after PBTI stress, measured using scaled SiON nMOS transistors. The recovery proceeds in discrete steps in these devices. Electron (blue) and hole (red) emission events can be observed as negative and positive discrete steps in the ΔV_{th} behavior.

be extracted semi-automatically [10]. A general observation regarding charge transitions in recovery traces is that pMOS devices exhibit considerably more defects than their nMOS counterparts [11]. Thus, more devices have to be measured to have sufficient transition events to get accurate statistics for the nMOS technologies.

In this work, we investigate both nMOS and pMOS devices. For each device kind, we evaluate the distribution of step heights employing transistors with different geometries. The observation is that the average step heights extracted from the distribution depend on the device dimensions. The shape of some of the distribution follows bi-modal exponential behavior, which is contradictory to what is reported in the literature so far. The bi-modal exponential distributions have been observed for devices with high-κ gate stacks where each branch of the distribution has been assigned to traps residing in the SiO_2 or the high-κ layer [12]. However, we now also report similar distributions for single-layer insulators. Afterwards we use the extracted distributions and combine them with our calibrated simulations conducted for similar large-area devices from [13] to evaluate the impact of distributed traps on the variability of simulated measure-stress-measure (MSM) sequences.

II. Experimental

Our working horse for the electrical characterization of single defects is MSM sequences, where stress and recovery phases are sequentially applied to a transistor. During the stress phase, a high bias is applied to the gate of the device, and defects can become charged. Note that, during stress phases, the drain bias is kept at zero bias to avoid any degradation effects on the devices related to hot-carriers [14]. During recovery, a bias close to the device threshold voltage is applied. In this phase, certain defects can emit their charge, causing a discrete step in the device current, see Figure 2. The recovery traces are shown in terms of a ΔV_{th} which is calculated by making use of an $I_{\text{D}}(V_{\text{G}})$ characteristic that is recorded prior to the stress phase. It has to be noted that in order to avoid any stress conditions during the measurements of the initial $I_{\text{D}}(V_{\text{G}})$, a very narrow gate bias range is selected. The data

TABLE I
Experimental Parameters, i.e., Stress/Recovery Time and Device Temperature, and Device-Specific Parameters Used in Our Study

Common Parameters:			
t_s	1ks		
t_r	1ks		
T	100°C		
Device-Specific Parameters (nMOS/PBTI):			
W(nm)	L(nm)	V_s(V)	V_r(V)
400	180	4.4	0.4
440	360	4.4	0.4
1000	700	7.56	0.35
Device-Specific Parameters (nMOS/NBTI):			
W(nm)	L(nm)	V_s(V)	V_r(V)
400	180	-4.4	0.4
440	360	-4.4	0.4
1000	700	-7.56	0.35
Device-Specific Parameters (pMOS/NBTI):			
W(nm)	L(nm)	V_s(V)	V_r(V)
220	180	-4.4	-0.4
400	180	-4.4	-0.4
800	180	-4.4	-0.4
440	360	-4.4	-0.4
1000	500	-7.62	-0.45

from the recovery traces are analyzed with the Canny algorithm which enables us to extract the discrete steps of ΔV_{th} from the recovery traces [10].

As has been mentioned before, during the recovery phase the threshold shift decreases as the defects emit their charges. The decrease of the ΔV_{th} can be seen in Figure 2. The electron emissions, which cause the recovery of the devices, are depicted with the blue lines. In our nMOS devices, we also observe a significant number of hole emission events. These transitions are indicated by an increase in the ΔV_{th} during the recovery phase. This is because hole traps affect the inversion layer of the semiconductor channel in an opposite way to the electron traps.

The experimental parameters that have been used for our studies can be seen in Table I. The stress and recovery times (t_s,t_r) for all devices have been kept the same. However, the stress bias has been adjusted according to the oxide thickness of the device kinds in order to achieve similar electric fields. Finally, the recovery biases (V_r) have also been adjusted to account for the different V_{th} of each device kind.

III. Distribution of Step Heights

It has to be noted that the trap distributions change between devices of the same kind. This means that precise evaluation of the number of active steps per device and the impact of the traps on the ΔV_{th} has to be evaluated using statistical methods. The number of defects per device is generally considered to follow a Poisson distribution which has been proposed by Kaczer *et al.* [15]. We extracted the number of defects per device for one of the tested device kinds, see Figure 3, which confirms the assumption made.

The average ΔV_{th} caused by a single defect can be estimated by a distribution function. For this, we create the complementary cumulative distribution functions (CCDFs), to present our

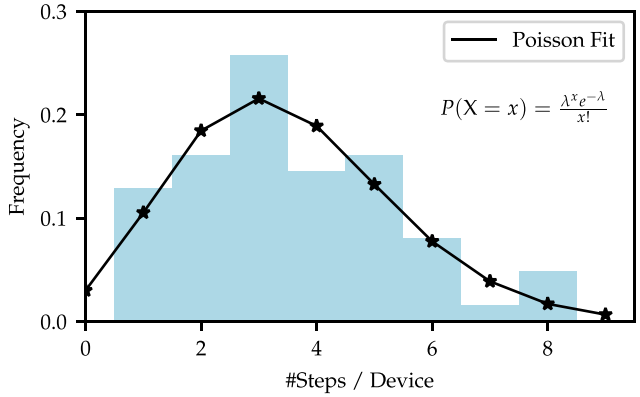

Fig. 3. Histogram of the number of steps per device detected from the relaxation curves of one of the tested geometries (W × L = 400 nm × 180 nm). The steps can be seen to follow a Poisson distribution.

results using the convention used in previous works [15]–[18]. The CCDFs are generated from the extracted step heights from recovery traces of the MSM measurements. In the previous investigations, the distributions extracted from experimental data have been documented to have exponential characteristics. The respective probability distribution function (PDF) for a single-mode has been described in [15] by the following formula

$$f(\Delta V_{\text{th}}) = \frac{1}{\eta} \exp\left(-\frac{\Delta V_{\text{th}}}{\eta}\right), \tag{1}$$

where η is the mean threshold voltage shift caused by a single charge transition event of a single defect. From the PDF the corresponding CDF can be calculated as

$$F(\Delta V_{\text{th}}) = \int f(\Delta V_{\text{th}}) \mathrm{d}\Delta V_{\text{th}} = 1 - \exp\left(-\frac{\Delta V_{\text{th}}}{\eta}\right). \tag{2}$$

By normalizing the CCDF to the number of devices, the following relation can be obtained

$$\frac{1 - \text{CDF}}{\#\text{devices}} = \sum_i N_{\text{T}_i} \exp\left(-\frac{\Delta V_{\text{th}}}{\eta_i}\right), \tag{3}$$

where $N_{\text{T}i}$ is the number of defects per device for each existing exponential branch i, ΔV_{th} is the threshold voltage shift and η_i is the average threshold shift induced by a single carrier. The expression above accounts for a possible multi-modal behavior of the experimental CCDFs [14], [19].

IV. Measurement Results

To get a detailed understanding of charge trapping for a certain technology, we evaluate both nMOS and pMOS transistors with different gate areas and oxide thicknesses. We analyze the step height distributions of electron and hole traps and demonstrate that uni-modal exponential distributions cannot describe the experimental data. Furthermore, we observe the electron and hole trap contributions for each device kind, indicating that trapping at both trap types is of equal importance for precise descriptions of the devices.

TABLE II
Extracted Parameters of CCDF Fitting on Experimental Data for the PBTI Study Case. Superscripts e,h Refer to Electron and Hole Trapping Accordingly. Bi-Modal Fit Is Only Used for Electron Traps Since Hole Traps do Not Exhibit Two Branches

Uni-modal					
W(nm)	L(nm)	$\eta^{\text{e}}(mV)$	N^{e}	$\eta^{\text{h}}(mV)$	N^{h}
400	180	1.8	4	0.35	2.4
440	360	0.83	7	0.37	0.5
1000	700	0.56	10.4	0.6	0.31
Bi-modal					
W(nm)	L(nm)	$\eta_1(mV)$	N_1	$\eta_2(mV)$	N_2
400	180	0.52	6.64	2.86	1.4
440	360	0.42	11.79	1.86	0.89
1000	700	0.36	10.54	0.76	3.52

A. Positive BTI of NMOS Transistors

First, we study nMOS devices with a positive applied stress bias. When a positive bias is applied at the gate of a MOS structure the valence and conduction energy bands bend towards lower energies. A schematic of the band diagram under PBTI stress can be seen in Figure 4 (left). A necessary condition for a defect to contribute to ΔV_{th} is that the defect must be energetically located in the so-called active energy region (AER) for charge trapping. For the PBTI case, electron traps above the Fermi level of the channel carrier reservoir and hole traps below the Fermi level at the poly-gate can become charged and then discharged under the initial conditions, provided that the stress conditions are applied for a time larger than the charge capture and the recovery time is larger than emission time of the respective defect. Thus, the bias used for the MSM measurement determines the energetic area spanned by the AER for both the charge exchange between the channel and electron traps (marked as a blue triangle) and between the poly-gate and hole traps (red triangle).

The respective CCDFs for the PBTI case of three sets of devices with different geometries are depicted in Figure 4 (right). The largest device (W × L = 1000 nm × 700 nm), which is marked as (T) in the figure legend, has a thicker oxide than the other two devices. Therefore a higher gate bias has been used to guarantee the same oxide field. The blue shades are used for electron trapping, i.e., interaction between silicon channel and defects, while the red ones are used for the hole traps, i.e., interactions between the poly gate and the defects. The CCDFs after PBTI stress reveal a bi-modal exponential behavior for electron traps and unimodal exponential characteristics for hole traps. Normalized CCDF (Eq. 3) can be used to fit the experimental data and extract device parameters η and N_{T}. Dashed and solid lines are used to depict uni- and bi-modal fits, respectively. Collected parameters for the PBTI case can be found in Table II.

As can be seen from the collection of parameters and the CCDF plots, the impact on ΔV_{th} under PBTI stress conditions is dominated by electron traps, still a small number of hole traps is found to be active: From 990 recorded traps, 910 defects (92%) have been characterized as electron-related. Charge trapping of electron traps has been recently assigned to defect/channel interactions, while hole trapping arises from

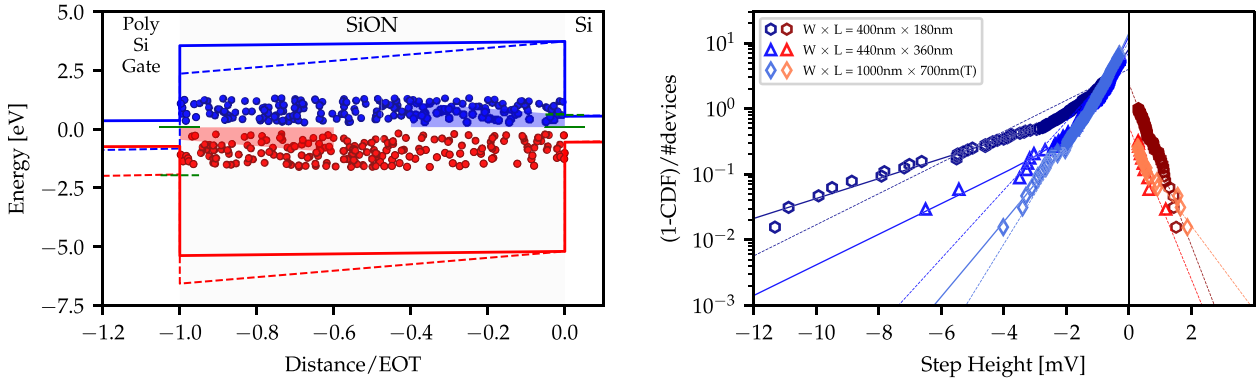

Fig. 4. (Left) Band diagram of nMOS devices shown for the positive bias stress case. Electron (blue) and hole traps (red) are shown, with the respective active energy regions (AERs) for charge trapping. The AER for charge transitions between the defects and the channel is marked with blue and for charge transitions between the defects and the gate with red. These areas define the energetic regions inside of which the defects can change their charge state during the experiments and thus, contribute to the drift of the measurement signal. Note that the height of the AERs changes with the applied gate bias. (Right) Distribution of step heights measured from SiON nMOS transistors after PBTI stress for three device sets with different geometries. The majority of the observed traps are electron traps (left), but a certain number of hole traps (right) can be observed too. The behavior of electron traps follows a bi-modal exponential distribution, while for the holes a uni-modal exponential behavior can be observed.

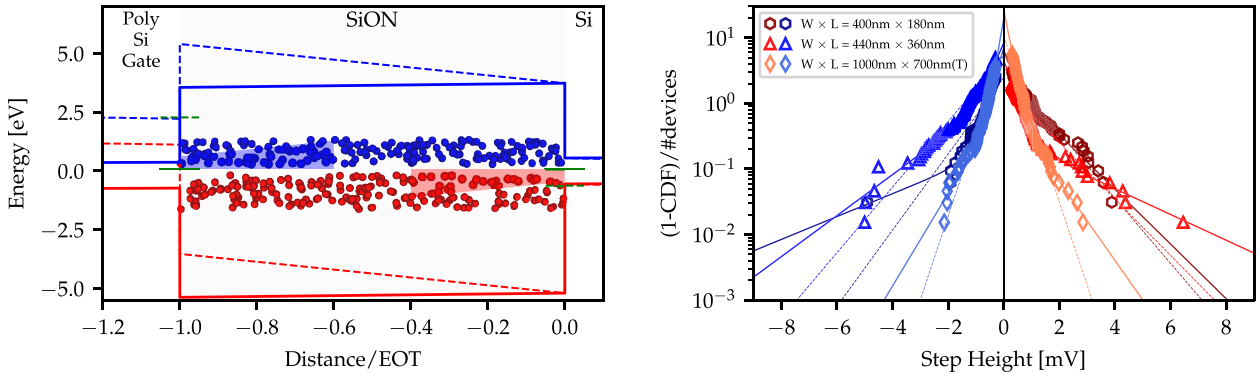

Fig. 5. (Left) The band diagram of nMOS devices for the negative stress gate bias case is shown here. In contrast to the PBTI case, more hole traps can contribute to total ΔV_{th} now as the AER at the channel covers the lower half of the band-gap. The AERs for charge transitions between the defects and the channel and for charge transitions between the defects and the gate are marked in blue and red color, respectively. (Right) Distribution of step heights of defects extracted after NBTI stress.Bi-modal exponential behavior can be observed for both types of traps.

defect/gate interactions [17]. A significant benefit of studying single-defects is that the contributions of the electron traps and hole traps can be separated, while in large-area devices, only the average response of a multitude of defects can be measured. The absolute contribution of a carrier type, for example electrons, to the total threshold voltage shift ΔV_{th}, can be calculated by [17]

$$r_e = \frac{\sum_{i=1}^{N_e} |d_e|}{\sum_{i=1}^{N_e} |d_e| + \sum_{i=1}^{N_h} |d_h|}, \tag{4}$$

where N_e and N_h are the numbers of electron and hole defects respectively, and $|d_e|$ and $|d_h|$ are the corresponding step heights of the single hole/electron emission events. It can be observed that hole trapping decreases the total ΔVth by about 5.9% for the bias and temperature conditions used for the PBTI case.

B. Negative BTI of NMOS Transistors

The device types studied in the previous section are also examined under negative bias stress conditions. The negative applied gate voltage creates an opposite bending compared to the PBTI case. Thus, the conduction and valence energy bands bend towards higher energies. The respective band diagram of the NBTI case can be seen at the left part of Figure 5. The AERs for hole trapping are depicted with red color and for electron trapping with blue. Under NBTI stress, hole traps below the Fermi level can become charged with carriers from the channel and carriers from the poly-gate can charge the electron traps. More holes traps and fewer electron traps are expected to contribute to the threshold voltage shift compared to the PBTI case.

The increased hole trapping can be clearly confirmed by the extracted CCDFs for both electron and hole traps of the right part of the figure. The CCDF for each kind of traps exhibits two branches, and considering a uni-modal model would lead to an underestimation of the tail of the distributions. A significant difference to the PBTI case is that in this case bi-modal exponential distributions can be seen for both kinds of traps. The extracted parameters from the bi-modal fitting are collected at Table III. Extracted parameters from a bi-modal model do not seem to be related to the device area as observed in works where uni-modal models are applied [15].

TABLE III
EXTRACTED PARAMETERS OF CCDF FITTING ON EXPERIMENTAL DATA FOR THE NMOS/NBTI STUDY CASE. SUPERSCRIPTS E,H REFER TO ELECTRON AND HOLE TRAPPING RESPECTIVELY

W(nm)	L(nm)	$\eta^e{}_1(mV)$	$N^e{}_1$	$\eta^e{}_2(mV)$	$N^e{}_2$	$\eta^h{}_1(mV)$	$N^h{}_1$	$\eta^h{}_2(mV)$	$N^h{}_1$
400	180	0.33	6.73	2.49	0.21	0.25	4.22	1.04	2.26
440	360	0.37	6.9	1.39	1.45	0.37	4.15	2.22	0.3
1000	700	0.16	18.54	0.62	1.08	0.18	26.33	0.72	1.02

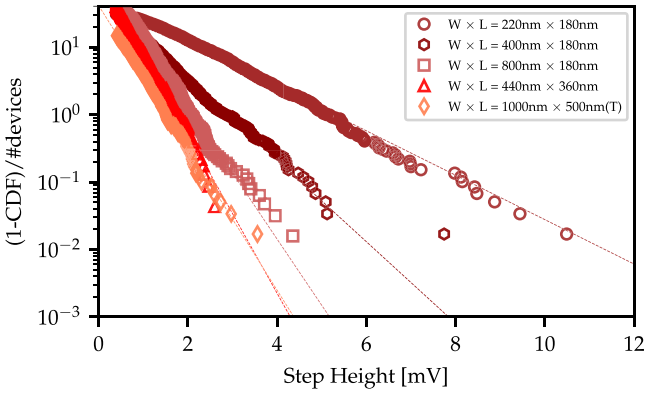

Fig. 6. Distribution of step heights of hole traps extracted after NBTI stress on pMOS devices. The dashed lines depict the uni-modal exponential function that has been used to explain the results.

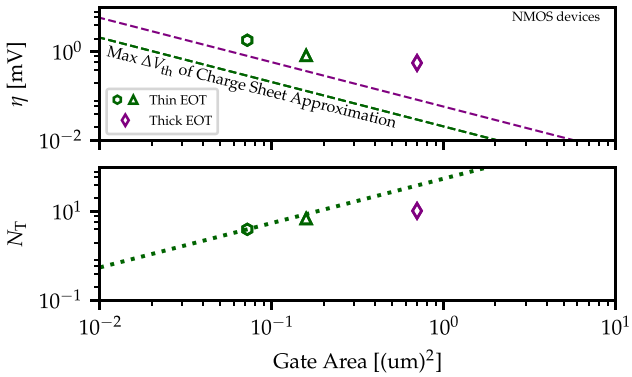

Fig. 7. Extracted impact of a single defect on the ΔV_{th} (η) and the number of traps per device (N_T) considering uni-modal exponential distribution. Clearly visible is the underestimation of the charge sheet approximation of the impact of the defects, on the device behavior. The maximum impact of CSA is considered by considering the traps directly at the interface.

TABLE IV
EXTRACTED PARAMETERS OF CCDFS FOR EXPERIMENTAL DATA OF PMOS DEVICES UNDER NBTI STRESS CONDITIONS

Uni-modal			
W(nm)	L(nm)	$\eta^h(mV)$	N^h
220	180	1.32	54.63
400	180	0.72	56.39
800	180	0.44	120.66
440	360	0.37	121.8
1000	500	0.4	42.77

C. Negative BTI of PMOS Transistors

In the previous section we showed that both electron and hole traps contribute the ΔV_{th} shift and that the step height needs to be described bi-modal. Using the same device geometries as in the nMOS case, we tested pMOS devices under NBTI conditions to compare the results. Analogously to the nMOS device, the largest device has a thicker oxide than the other geometries, and thus a higher stress gate bias was used to guarantee an equivalent oxide field.

The CCDFs of the pMOS device can be seen in Figure 6. In contrast to the nMOS device, only hole traps are observed, electron traps do not contribute to the threshold voltage shift at all. This can be explained by the larger effective number of defects prevalent in pMOS devices [11]. The step heights can be described uni-modal on all geometries, the extracted parameters can be found in Table IV.

D. Extracted Parameters

1) Comparison Between NBTI and PBTI: The step heights of electron traps extracted from nMOS devices follow a bi-modal exponential distribution. For SiON technologies, only uni-modal exponential distributions have been reported in the literature [11], [12]. Bi-modal distributions of single-defects have been observed for technologies with high-κ gate stacks [12]. In high-κ devices, each branch of the distribution has been assigned to charge-transfer interactions of defects residing in one of the insulating layers with the channel. Recently, this kind of distribution has been reported for nMOS devices with SiON insulators, too [14]. The overall bi-modal CCDF has been separated into two almost uni-modal ones, where one branch has been assigned to electron trap/channel interactions and the second one to hole trap/poly-gate interactions [17]. According to our latest results, bi-modal CCDFs are obtained for each kind of trap. For PBTI, the behavior of nMOS devices is clearly dominated by electron traps (approximately 92% of all traps are electron traps), whereas for NBTI, hole trapping becomes significantly important. The ratio between electron and hole traps is approximately 52% to 48%. Therefore both electron and hole traps need to be considered. On pMOS devices, the ΔV_{th} results entirely from hole traps. Note that a large number of traps with small average step height are more likely to be far from the channel [17], and thus their measurement requires optimized low-noise tools [14]. Otherwise, charge trapping at hole traps might completely vanish in the measurement noise.

2) Comparison to Charge Sheet Approximation: The extracted parameters for nMOS/PBTI devices, i.e., average step height and the number of traps per device, considering uni-modal and bi-modal CCDFs are shown in Figure 7 and Figure 8, respectively, together with the max limit of charge sheet approximation (CSA). The parameters extracted from the measurements made employing pMOS devices can be seen in Figure 9. It seems that the η values are proportional to the

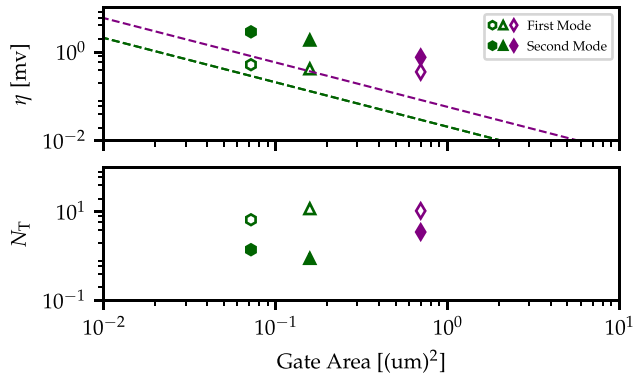

Fig. 8. The extracted values for the two modes of the bi-modal exponential distribution are shown. As can be seen from Fig. 4, the distribution follows more a bi-modal exponential behavior than a uni-modal one. Again, the charge sheet approximation significantly underestimates the impact of the defects, which lead to a too pessimistic estimation for defect density from ΔV_{th}.

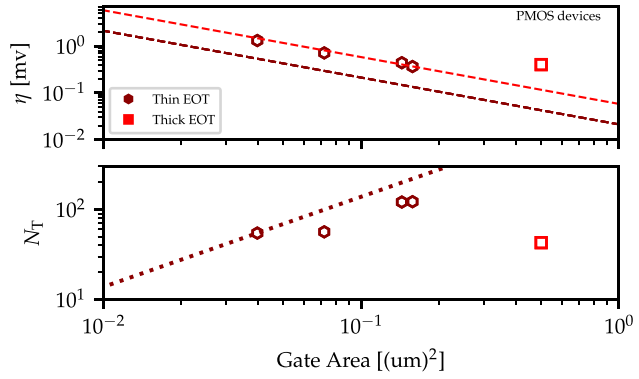

Fig. 9. The extracted values for the uni-modal exponential distribution of the hole traps of pMOS devices. The η values seem to be proportional to the gate area. Max limit of charge sheet approximation is around 3 times smaller from values extracted from the CCDFs.

gate area under the assumption of a uni-modal distribution of the step heights.

To estimate the impact of a single defect on the ΔV_{th} the CSA is often used in device simulators. This model assumes that the oxide charge is uniformly distributed over a fictitious sheet in the insulator and can be described by [20]

$$\Delta V_{\text{th}} = -\frac{q}{\epsilon_0 \epsilon_{\text{r}} WL} t_{ox}\left(1 - \frac{x_{\text{T}}}{t_{\text{ox}}}\right), \tag{5}$$

where q is the elementary charge, ϵ_0 and ϵ_{r} the dielectric constants, t_{ox} the oxide thickness, and x_{T} the position of the trap with respect to Si/SiON interface. By applying the CSA, the trap density can be estimated from a given ΔV_{th}. In our work, we compare the extracted values of threshold voltage shift from CCDFs by considering the maximum impact given by the CSA which occurs at $x_{\text{T}} = 0$, i.e., directly at the interface. It is clearly visible from the dashed lines in Figure 7 and Figure 8, that for both distributions the CSA significantly underestimates the extracted average impact of the defects η. As a consequence too pessimistic results for defect densities will be extracted from ΔV_{th}. The results shown here are of particular importance to enhance charge trapping models and the accuracy of the simulations.

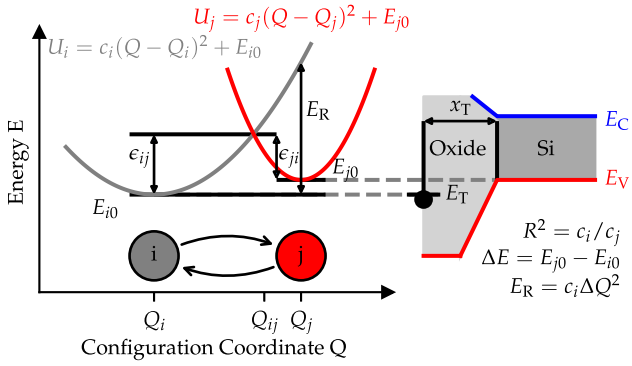

Fig. 10. The BTI simulator Comphy uses an effective 2-state NMP model to describe a charge transition of a pre-existing oxide defect. Such a transition from state i to state j is possible by overcoming the barrier ϵ_{ij}. The harmonic potential energy surfaces are characterized by the trap level E_{T}, the relaxation energy E_{R} and the ratio of the curvatures R. The spatial coordinate x_{T} is used for computing the tunneling factor.

V. Simulation Results

The BTI simulator Comphy [21] is used for a verification of the distributions, which were extracted in Section IV. Comphy uses an one-dimensional gate-stack for which the surface potential is computed at a given gate voltage using several input quantities such as doping concentrations or the work-function difference for the ideal device. During the execution of a BTI simulation defects are sampled in the oxide. Capture and emission rates of these pre-existing defects can be computed using a two-state nonradiative-multiphonon theory [22]. For the computation of the rates, the barrier heights ϵ_{ij} (see Figure 10) between the defect and the bandedges needs to be computed.

For this, the trap level E_{T}, the relaxation energy E_{R} and the ratio of the curvatures of the potential energy surfaces R is needed. Additionally, it is necessary to know the spatial position x_{T} of the defect for computing the Wentzel-Kramers-Brillouin (WKB) factor. By sampling E_{T}, E_{R}, x_{T} for a fixed R-value, it is possible to compute the transition rates:

$$k_{ij} = n v_{\text{th}} \vartheta_{\text{WKB}} \sigma \exp\left(-\frac{\epsilon_{ij}}{k_{\text{B}} T}\right) \tag{6}$$

with n being the carrier concentration, the thermal velocity v_{th}, the WKB factor ϑ_{WKB} and the capture cross-section σ [22]. We use the defect bands extracted in [13] for the simulations, which have been extracted for large-area devices using a non-negative least square approach for finding optimal defect distributions semi-automatically. We randomly draw defects and sample a η-values for every contributing defect from these defect bands using the CCDFs extracted in Section IV.

Using this setup, we can simulate the measured MSM-traces from large area devices presented in [13], as shown in the top part of Figure 11. The measurements were performed at $T = 100\,°\text{C}$ with three different stress conditions. As can be seen, the step heights extracted from our CCDFs allow a precise simulation of the measurement data. The lower figures show recovery traces for the measurement with the highest

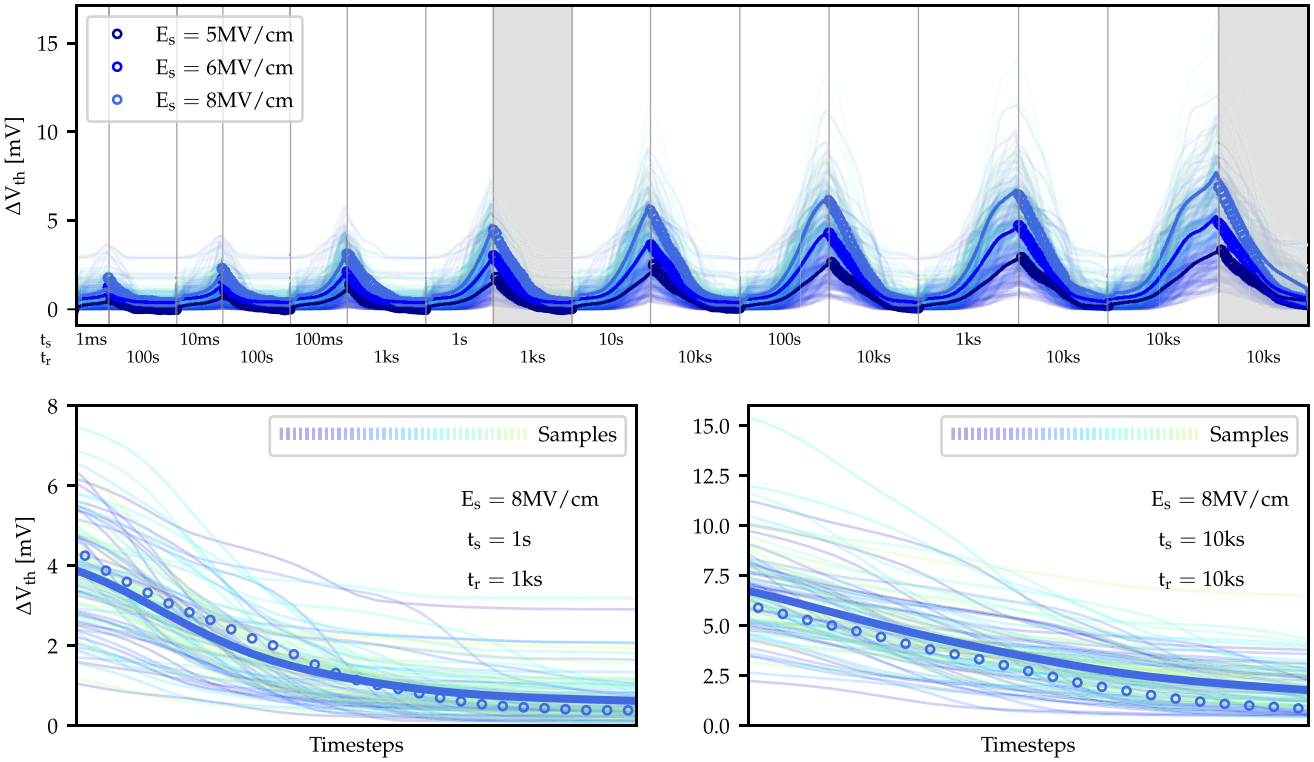

Fig. 11. In the top figure MSM measurements (dots) on large-area devices are shown, as presented in [13], at $T = 100\,°C$ under three different stress conditions. The lines are simulated with the BTI simulator Comphy averaged for 100 sets of sampled step heights η using the CCDFs extracted in Section IV. The regions marked grey are shown more detailed in the two bottom figures. Every light line presents a BTI simulation with a sampled set of step heights, the solid line is the average of all performed simulations.

oxide field for two selected regions (marked grey) with re-sampled step heights. The solid line shows the average of all recovery traces with different sampled step heights.

VI. Conclusion

The distribution of the step heights of single defects plays an important role in nanoscale devices. To examine this, we used MSM measurements and applied both NBTI and PBTI stress. We used devices small enough to detect single steps when charge transitions occur. From the detected steps, we extracted the distributions of the step heights and showed that in the case of PBTI/nMOS bi-modal distributions are needed for a correct description. The extracted distributions deliver higher average step heights than the usual in the simulation used charge sheet approximation, which leads to underestimating the contribution of single defects. We then used our model CCDFs in our device simulator Comphy and showed that we can explain our measurements made on large-area devices with our extracted step height distributions.

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