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Impact of negative bias temperature instability on single event transients in scaled logic circuits

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[Correction added on 20 January 2021, after first online publication: corrected email address of Michael Waltl.]

Abstract

Altering the performance of single transistors and integrated circuits at nominal operating conditions over time, as well as soft errors, are serious reliability issues for integrated CMOS circuits, especially when used in space applications. In principle, the effect of soft errors becomes even more critical if the circuit performance degrades over time. To address this detrimental behavior, the impact of performance degradation due to NBTI on the soft error susceptibility of integrated circuits is analyzed thoroughly. For this, we analyze the critical charge sensitivity of the two-input NAND gate and NOR gate for different operating temperatures at stress times up to 3 years. The results show that the critical charge decreases with the temperature and strongly depends on the input states. Next, we validate the results employing the c17 ISCAS'85 benchmark suite, employing the PTM model with the HSPICE to estimate the soft error at the sensitive nodes. The critical charge is observed to be sensitive to the selected supply voltage and device temperature and thus provides a good measure for the soft error susceptibility with respect to NBTI at various operation conditions.

KEYWORDS

circuit simulation, ISCAS'85 benchmark circuit, NBTI, reliability, soft error

1 | INTRODUCTION

With the scaling of CMOS technology toward only tens of nanometer small transistors, variability between seemingly identical transistors, and reliability challenges of single transistors have become more and more important for the performance and lifetime of integrated circuits.[1] In this context, negative bias temperature instabilities (NBTI) and positive BTI (PBTI) play an important role for NMOS and PMOS transistors and have been the subject of many experimental and theoretical studies.[2,3] Many of the experiments reveal that NBTI in PMOS transistors is much more dominant compared to PBTI in NMOS transistors. Thus, the NBTI/PMOS case is typically studied and considered to be primarily responsible for the lifetime of CMOS circuits.[4,5]

In more detail, NBTI refers to the case when a negative stress bias (negative V_{gs}) is applied which can trigger the creation of so-called interface states and oxide defects, which lead to a drift of the threshold voltage, reduction of the sub-threshold slope, and a reduction of the on-current.[4] When the gate stress has released the shift of the threshold voltage accumulated during the stress phase partially recovers. The threshold voltage shift which remains after a large recovery period of the device has elapsed is considered the permanent degradation which can also slightly increase from

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one stress cycle to the next stress cycle. This permanent shift of the threshold voltage is particularly disadvantageous for CMOS circuits, as it can introduce some uncertainty in the device and circuit behavior and can lead to a decrease of the device/circuit lifetime.[6,7] Note that NBTI is the dominant device degradation mechanism at low drain biases. At high drain bias, the so called hot-carrier degradation becomes more dominant and seriously affects the device behavior.[8,9]

Along with susceptibility to NBTI, nanoscale devices are more sensitive to radiation-induced errors, which also aggravates the noise immunity of the circuits.[10,11] Also, the recent technology generation operates at low supply voltages which can, on one hand, reduce the circuit node capacitances, but on the other hand increase the probability of soft errors.[12,13] Overall the scaled feature sizes, the lowered operating voltage, and the higher operating frequencies in combination with reduced noise margins give rise to an increased soft error rate occurring in integrated circuits.[14,15]

In addition, the susceptibility to soft errors can become even worse when single event transients (SETs) are considered in such advanced nodes. Such SETs can be caused by strikes from highly energetic particles, like cosmic neutrons on a sensitive region of the semiconductor device, which can affect the circuit performance.[16,17] For example, when particles strike the silicon substrate, they can create secondary electron–hole pairs that can be collected by surrounding pn-junctions and so influence the device behavior.[18,19] The alpha particles are emitted mostly due to the radioactive decay of uranium and thorium impurities in the chip packaging. As the alpha particle passes through the semiconductor device, electrons a dislodged from the crystal lattice sites along the track of the alpha particle.[20,21] The critical charge is the minimum charge required to flip the logic. Next to SETs, the strikes may lead to single event upsets (SEUs) where both can hamper the proper functioning of the circuit, and lead to soft errors.[22-25] The direct ionization by protons may cause SEU in devices with low critical charge (Q_{crit}).[26]

The aforementioned SEU is the most common type for a single event effect (SEE) occurring in storage elements (latches and memory cells), which can lead to a flip of the logic state of a circuits' output. In combinational circuits, SEUs can be induced as an additional current which is injected at selected nodes and then propagates through the logic elements and can give rise to soft errors.[27]

In this work, we evaluate the effect of NBTI in combination with the soft error radiation hardening enhancement of integrated CMOS circuits. To this end, firstly the soft error analysis of a two-input NAND gate is performed at different operating temperatures and a total stress time of up to 3 years. Furthermore, we compute and compare the critical charge of the circuit nodes to evaluate the worst-case input combination which is maximum susceptible to soft errors. Subsequently, the sensitivity of the radiation hardening of the two-input NAND gate is evaluated using the soft error rate ratio (SERR). The worst-case input combination is then identified and used for further analysis. To this extend, we further implement the c17 benchmark circuit from the ISCAS'85 suite[28] and focus on the node which propagates a possible SET directly to the output of the circuit. Further, we analyze the critical charge variation of the c17 circuit with the stress time for the case when the maximum number of PMOS transistors stressed.

2 | RADIATION HARDENING ANALYSIS METHODOLOGY

To study the performance of circuits considering device aging due to NBTI, we apply the PTM model calibrated to a 32 nm CMOS technology node.[29] For stress analysis and aging evaluation, we used the HSPICE MOSRA model[30] and perform all simulations at a supply voltage $V_{\text{dd}} = 0.9$ V. The operating temperature is set to T = 125°C, which leads to an acceleration of the aging effects. We have considered the DC stress for analyzing the aging effects in the circuits.

To inject SEU into the simulations, the induced current is modeled by a double exponential current source[31] specified by

$$I_{\text{inj}}(t) = \frac{Q_{\text{inj}}}{\tau_f - \tau_r} \times \left(e^{-t/\tau_f} - e^{-t/\tau_r}\right) \tag{1}$$

or alternatively by

$$I_{\text{inj}}(t) = I_{\text{peak}} \times \left(e^{-t/\tau_f} - e^{-t/\tau_r}\right) \tag{2}$$

where Q_{inj} is the total amount of charge deposited at the sensitive node in fC, and I_{peak} is the peak value of the current source in μA. The parameters τ_f and τ_r are material dependent parameters and are set to $\tau_r = 1$ ps and $\tau_f = 50$ ps according to Ref. 32.

To further calculate Q_{crit} (in fC), we determine the minimum magnitude and duration of the injected current pulse that is required to flip the state of a logic output. In that way, Q_{crit} is determined by integrating over the current pulse and can be given as

$$Q_{\mathrm{crit}} = \int_0^{T_{\mathrm{crit}}} I_{\mathrm{inj}}(t)dt \tag{3}$$

where $I_{inj}(t)$ is the injected current pulse injected at the node considered for the SEU analysis.

2.1 | Soft error rate (SER)

In principle, a soft error can occur in any digital circuit when enough charge is externally induced that this can lead to a change of the logic value of the respective circuit node. In this work, the SER of a circuit is analyzed considering combinational circuits like the two-input NAND gate and can be evaluated from its Q_{crit}. The SER depends exponentially on Q_{crit} and it is found that a larger value of Q_{crit} directly translates into lower SER.[33] Thus, the SER can be expressed as.[34]

$$SER \propto N_{\mathrm{flux}} A e^{-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{S}}}} \tag{4}$$

where N_{flux} is the neutron flux intensity in particles/(cm^2 × s), A is the cross-section area of the sensitive node in cm^2, and Q_S is the charge collection efficiency of the device in fC.[35] From the above equation, it is obvious that a small increase in Q_{crit} will significantly reduce the SER.

For the validation of soft error enhancement of the two-input NAND gate for different input combinations, the soft error rate ratio (SERR) is introduced. The SERR is calculated by assuming only Q_{crit} being affected by NBTI stress

$$\mathrm{SERR} = \left.\frac{\mathrm{SER}_{\mathrm{Unstressed}}}{\mathrm{SER}_{\mathrm{Stressed}}}\right|_{@T} = \left.\frac{\mathrm{SER}_{\mathrm{0Year}}}{\mathrm{SER}_{\mathrm{3Years}}}\right|_{@T}. \tag{5}$$

In terms of the critical charge, the SERR is given by

$$\mathrm{SERR} \approx \mathrm{antilog}_e\left[Q_{\mathrm{crit}}^{\mathrm{3Years}} - Q_{\mathrm{crit}}^{\mathrm{0Year}}\right]\Big|_{@T} \tag{6}$$

where SER_{0Year} and SER_{3Years} are the soft error rates, and ${Q_{crit}}^{0Year}$ and ${Q_{crit}}^{3Years}$ are the critical charges without stress and after 3 years of NBTI stress, respectively.

2.2 | Masking factors

A direct way to improve the immunity of a logic circuit to radiation is adjusting the sizes of all the gates in order to sustain striking particle energy.[36] However, this approach brings overhead costs like increased required chip area with it. One alternative solution can be masking of the SETs from the logic input to the circuits. The logical masking of any circuit depends on the input pattern, which is applied to the given circuit. Figure 1 shows the two possible combinations for the sensitization and logical masking for the two-input NAND gate. If one of the inputs is at logic high, a possible SET occurring at the other input at the same time will be directly transferred to the output. Whereas if one of the two inputs is at a logic low state, the SET occurring at the other input terminal is logically masked and it will not be transferred to the output and thus the SET will not affect subsequent stages. The probability of logical masking for any circuit is given by[36]

FIGURE 1 Logical masking of the SET shown for the two-input NAND gate

$$P_{\text{Logical masking}} = 1 - P_{\text{Sensitization}}. \tag{7}$$

3 | SINGLE EVENT TRANSIENT EFFECT ON CIRCUIT PERFORMANCE

Figures 2 and 3 show the simulated circuit for the two-input NAND gate and NOR gate, respectively. In our simulations, the effect of the SET strike is considered to occur at the drain terminals of each of the transistors. In Figure 2, the parallel PMOS transistors are sensitive to the SET when both M1 and M2 are under stress and we inject SET current into the circuit node *Y*. In this situation, the active area for strike includes the drain area of both of the PMOS transistors. If we inject SET current with the opposite direction then it will perform a strike on M3. Similarly, if a SET current is injected at node *N*, it will perform strike on M4.[37]

In Figure 3, the PMOS transistor M2 is sensitive to the SET when it is under stress, and we inject SET current into the circuit node *Y*. Similarly, the PMOS transistor M1 is sensitive to the SET when it is under stress, and we inject SET current into the circuit node *P*. In this situation, the active area for strike includes the drain area of PMOS transistors M2 and M1. If we inject SET current at node *Y* in the opposite direction, it will then perform a strike on the parallel NMOS transistors M3 and M4.[38,39]

Here, we have considered a SET strike on only PMOS transistors for both NAND and NOR gates because the effect of NBTI is more severe for PMOS transistors.

3.1 | Critical charge analysis

Figure 4 shows the critical charge of a two-input NAND gate as a function of the temperature and stress time for the four possible input combinations. Results demonstrate that the input combinations AB = 01 and AB = 10 exhibits the lowest and highest critical charge compared to the two other input combinations, respectively. Similarly, Figure 5

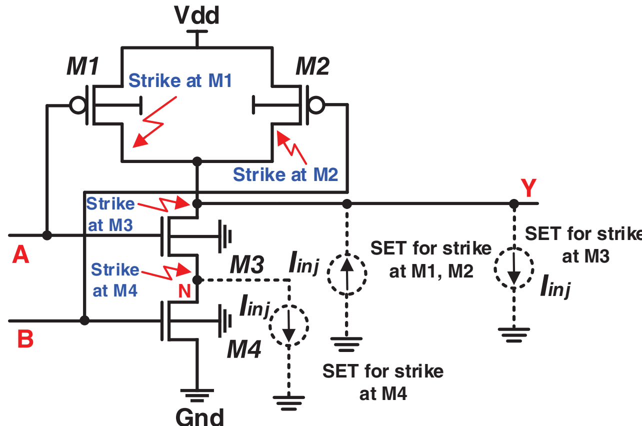

FIGURE 2 SETs current source injecting into the sensitive node of all four transistors of the two-input NAND gate

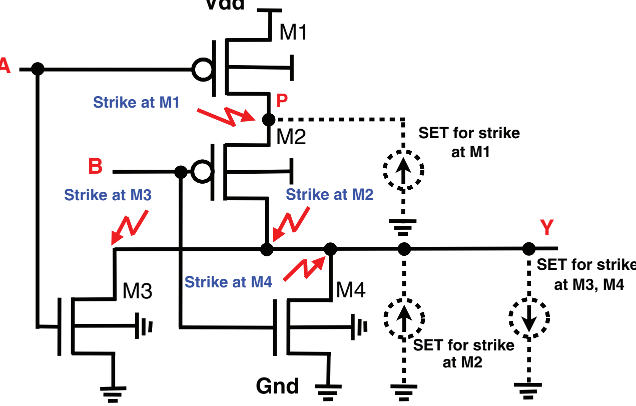

FIGURE 3 SETs current source injecting into the sensitive node of all four transistors of the two-input NOR gate

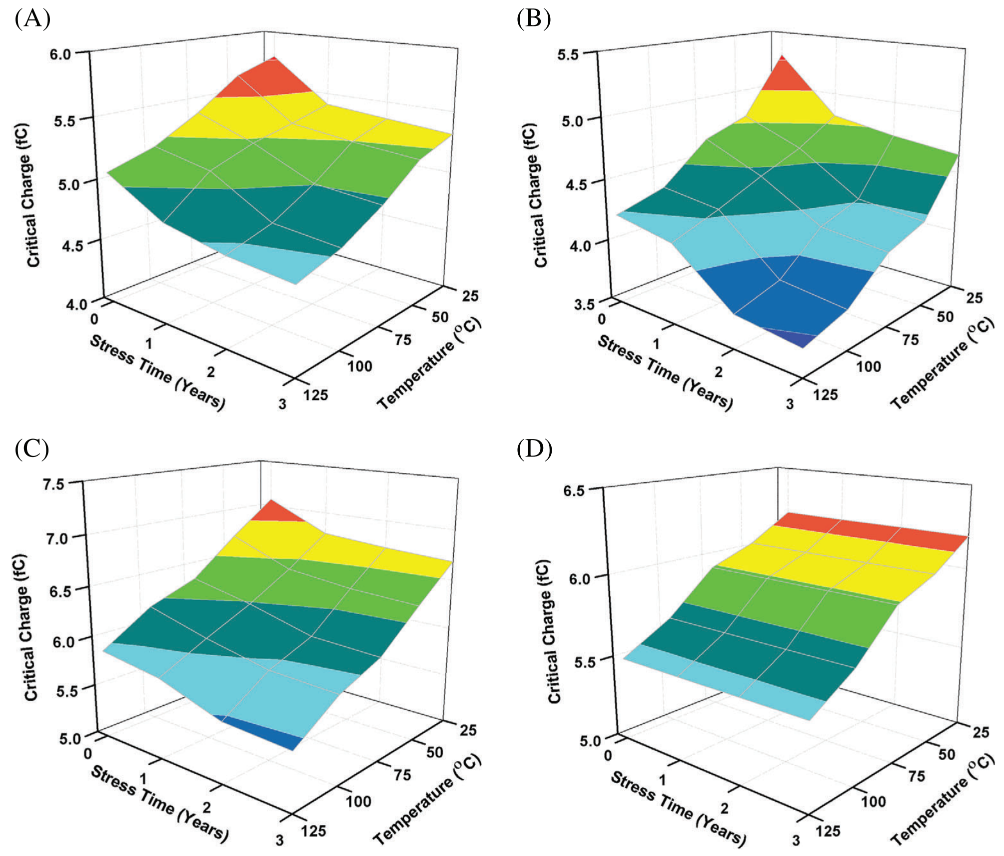

FIGURE 4 Critical charge of the two-input NAND gate as a function of temperature at different stress times with different input patterns

shows the critical charge of a two-input NOR gate as a function of the temperature and stress time for the four possible input combinations. Results demonstrate that the input combinations AB = 00 and AB = 11 exhibits the lowest and highest critical charge compared to the two other input combinations, respectively. It is further observed that the critical charge for both the NAND gate and NOR gate decreases with increasing stress time and temperature.

From the above results, we conclude that the two-input NAND gate and two-input NOR gate has minimum critical charges at AB = 01 and AB = 00, respectively, indicating that the effect of the soft error is highest for these input combinations. Our objective is to analyze the effect of the soft error on the ISCAS'85 c17 benchmark circuit, which consists of NAND gates. Therefore, input combination AB = 01 for NAND gate is considered for further analysis in Figure 6, which shows the critical charge variation for different supply voltages, considering different load capacitances. As can be seen, the critical charge of the sensitive node increases with the supply voltage due to the higher current flowing from the supply to the node and thus providing more charge at the sensitive node. A higher supply voltage changes the junction capacitance. When the supply voltage increases, the junction capacitance decreases due to the widening of the depletion region. An increase of the load capacitance also increases the effective circuit capacitance and thus a higher charge is required to unintendedly flip the logic.

3.2 | Soft error analysis

For the resistivity of the two-input NAND gate and NOR gate against soft errors, the SERR is evaluated. Table 1 shows the SERR after 3 years of stress at different operating temperatures. It is observed that the SERR increases with temperature for three possible input combinations of both two-input NAND gate and NOR gate. However, in the case of AB = 11, the SERR is constant for all the operating temperatures because none of the PMOS transistors is under NBTI stress. As can be seen, the two-input NAND gate and NOR gate is most sensitive to soft errors at the input combination of AB = 01 and AB = 00, respectively. To extend our analysis, we use the c17 circuit from the ISCAS'85 benchmark suite and is explained in the subsequent section.

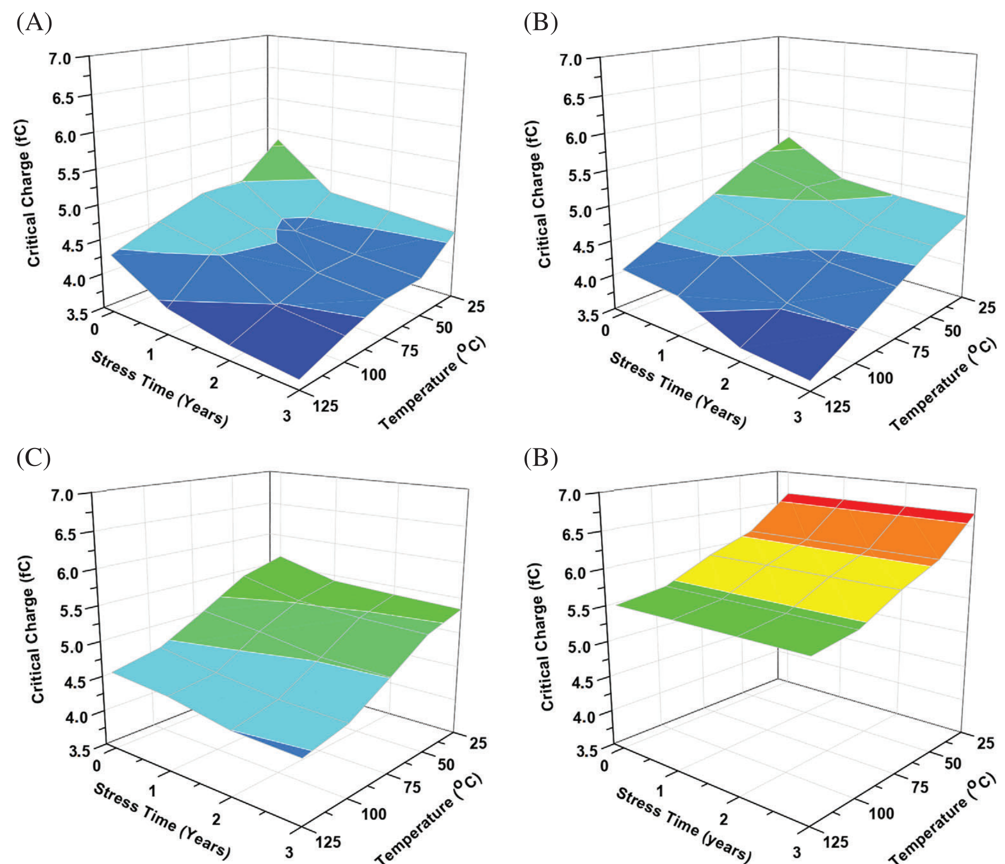

FIGURE 5 Critical charge of the two-input NOR gate as a function of temperature at different stress times with different input patterns

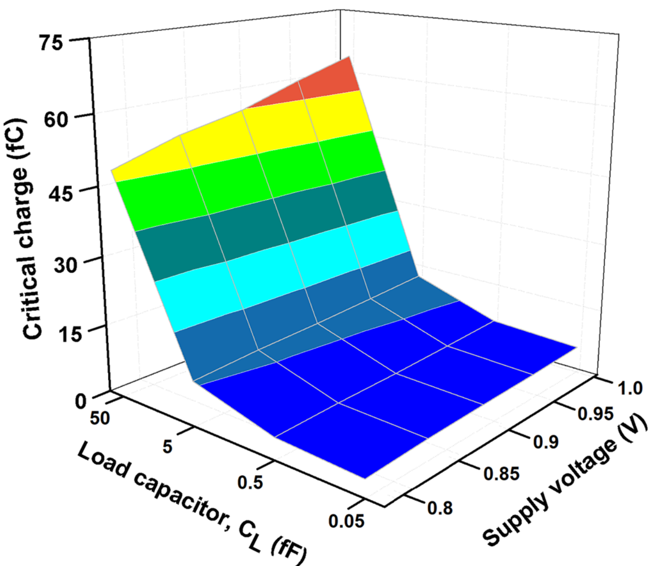

FIGURE 6 Two-input NAND gate critical charge characteristics shown at different supply voltages for various load capacitors (C_L)

4 | ISCAS'85 C17 BENCHMARK CIRCUIT

Figure 7 shows the circuit for c17 from the ISCAS'85 benchmark suite which consists of six interconnected NAND gates. We need to identify the critical path in the c17 circuit where the most number of PMOS transistors are stressed during normal operation.[40] In this paper, we primarily focus on the NBTI for PMOS transistors. The PMOS transistors are stressed when a logical low state is applied at the respective input of the NAND gates. The probabilities of getting

TABLE 1 Soft error rate ratio (SERR) at various operating temperatures for all possible input combinations of the two-input (A,B) NAND gate and NOR gate

	NAND gate				NOR gate			
Temperature (°C)	0,0	0,1	1,0	1,1	0,0	0,1	1,0	1,1
25	0.629	0.524	0.677	1.0	0.424	0.518	0.732	1.0
50	0.634	0.557	0.689	1.0	0.461	0.533	0.739	1.0
75	0.648	0.566	0.703	1.0	0.462	0.556	0.755	1.0
100	0.658	0.588	0.710	1.0	0.478	0.579	0.770	1.0
125	0.665	0.596	0.723	1.0	0.498	0.603	0.776	1.0

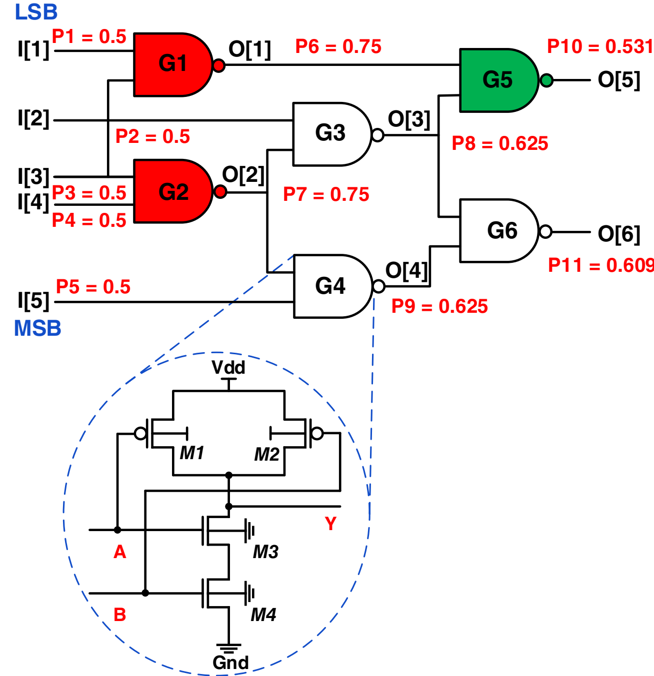

FIGURE 7 Schematic of the c17 circuit from the ISCAS'85 benchmark suite. P_1 through P_{11} are the input and output signal probabilities for six NAND gates of the c17 circuit. The PMOS transistors are under NBTI stress conditions when a logic low state is applied at the respective inputs

logic high at each node of the circuit, P_1 through P_{11} are shown in Figure 7. All possible input pattern combinations are applied to the inputs I[1]-I[5] of the circuit to compute the probabilities. Here P_i is the ratio of the number of logic high states on line i to the total number of input patterns. The total number of possible combinations for this circuit are $2^5 = 32$. The input signal probability for each of the inputs I[1]-I[5] is considered to be 0.5, as the probability of primary input is 0 or 1 is assumed to be equal.

The effect of NBTI on PMOS transistors and its performance degradation depends on the input signal probability. Furthermore, the impact of NBTI on the entire c17 circuit depends on the input and output signal probability of each NAND gate. The output signal probability of each NAND gate is again the input probability of a subsequent NAND gate. The output signal probability for a logic high state of the input of each NAND gate can be expressed as[41]

$$P(Y=1) = 1 - P_A P_B \tag{8}$$

where P_A and P_B are the input signal probabilities for having a logic high state at the inputs (considering A and B are two inputs) of the respective NAND gate. As can be seen from Figure 7, the gates G1 and G2 have the highest probability to be NBTI stressed, as one or both inputs are at the logic low state more frequently than the inputs of other NAND gates. NAND gate G5 has the minimum probability of being stressed during operation. The NAND gates with the maximum stress during operation are highlighted in red whereas the NAND gates with minimum NBTI stress are highlighted in green.

Table 2 summarizes the minimum stress patterns and the worst-case stress patterns of 12 PMOS transistors from 6 NAND gates of the c17 circuit. In the c17 circuit, we have 32 possible input combinations and 12 PMOS transistors from 6 NAND gates. For each input combination, the number of stressed PMOS transistors are different. As there is a

total of 12 PMOS transistors, we manually checked the stressed transistors for all possible combinations. We observed that the input patterns 00010 and 10010 has the maximum number of stressed PMOS transistors. These input patterns are further used to analyze the degradation of the c17 circuit.[42]

4.1 | Sensitization and Logical Masking

Table 3 shows the logical masking and sensitization probabilities of all NAND gates in the c17 benchmark circuit. It can be observed that the logical masking decreases with the number of stages move toward the output of the circuit.

For further analysis, the two worst-case input combinations (00010 and 10010) having the maximum number of PMOS transistors under stress are considered. The logical masking and sensitization of NAND gates on the c17 circuit for the most critical input patterns are shown in Figure 8. For the input pattern 00010, the gates G1, G2, and G4 are logically masked. As the output node (S) of G2 transfers the logic to the next stage, it is the primarily sensitive node in the c17 circuit. This node is considered to be a sensitive node because the stress of PMOS transistors and sensitization probability of the next stage gates depends on the logic at node S. A SET at this sensitive node will be directly transferred to the outputs through G3, G5, and G6, as shown in Figure 8A. The effect of the soft error to NAND gate G6 is more as compared to G5 because the critical charge for the NAND gate input combination 01 is the smallest among all other possible combinations. Thus the transfer of SET to the O[6] will be higher as compared to the output O[5].

Similarly for the input pattern 10010, the gates G1 and G2 are logically masked. A SET induced at node S in the circuit will transfer to the outputs through G3, G4, G5, and G6 as shown in Figure 8B. The effect of SET to NAND gate G6 is more as compared to G6 because the critical charge for input combination 00 is less as compared to the 10.

4.2 | Effect of supply voltage variation and device temperature variation on c17 circuit

We calculate the active power dissipation of the c17 benchmark circuit considering all possible input combinations without stressing the circuit, as shown in Figure 9. From results, it is observed that the input combinations 10010 and 11110 have the minimum and maximum power dissipations, respectively.

Further, to analyze the effect of supply voltage variation and temperature variation on the dynamic power dissipation by the c17 circuit, we calculated the circuit power dissipation for the device temperature ranging from 25°C to 125°C and different supply voltages from 0.45 to 1.05 V as shown in Figure 10. Results demonstrate that the circuit

TABLE 2 Stressed PMOS transistors (M_1 and M_2) in all NAND gates of c17 circuit for the four extreme input patterns

	Maximum stress		Minimum stress	
NAND Gates	00010	10010	11110	11111
G1	M_1, M_2	M_1, M_2	M_1	–
G2	M_1, M_2	M_1, M_2	–	–
G3	–	–	M_2	M_2
G4	M_2	–	M_1	M_1
G5	M_2	M_2	–	M_1
G6	M_1	M_1, M_2	–	–

TABLE 3 Sensitization and logical masking probabilities of all NAND gates of the c17 circuit

NAND Gates	$P_{Sensitization}$	$P_{Logical\text{-}masking}$
G1	0.25	0.75
G2	0.25	0.75
G3	0.375	0.625
G4	0.375	0.625
G5	0.4375	0.5625
G6	0.4375	0.5625

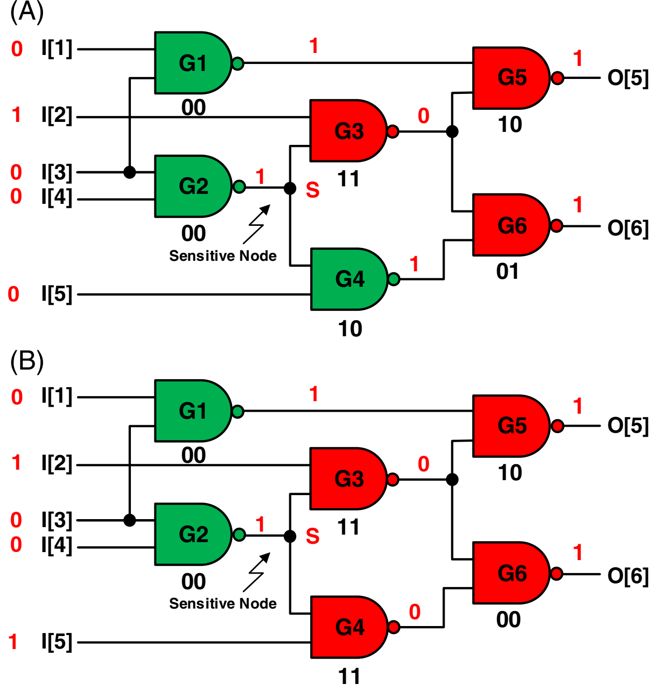

FIGURE 8 Logical masking of the SET of the c17 circuit for two input combinations having maximum stressed PMOS transistors. A, For the input pattern 00010; and B, for the input pattern 10010. The logically masked NAND gates are represented in green whereas the NAND gates are not logically masked as represented in red

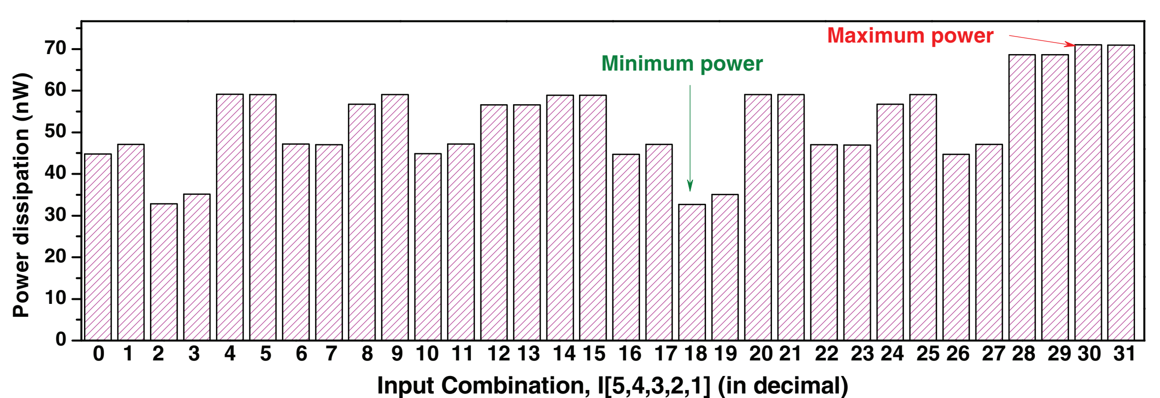

FIGURE 9 Static power dissipation of the c17 circuit for all the possible input combinations. Here, I[5] and I[1] are the most and least significant bits, respectively. There are 32 (0 to 31) total number of input combinations from five input c17 circuit

power dissipation increases with the supply voltages as well as the operating temperature of the circuit. To analyze the effect of supply and temperature variations, we calculated power dissipation sensitivity for the c17 circuit. The power dissipation sensitivity with supply voltage and temperature can be calculated as

$$\text{Sensitivity}_{\text{power}}\Big|_{@T} = \left.\frac{\text{Power}|_{V_{\text{dd}}^{\text{H}}} - \text{Power}|_{V_{\text{dd}}^{\text{L}}}}{V_{\text{dd}}^{\text{H}} - V_{\text{dd}}^{\text{L}}}\right|_{@T} \tag{9}$$

and

$$\text{Sensitivity}_{\text{power}}\Big|_{@V_{\text{dd}}} = \left.\frac{\text{Power}|_{\text{T}^{\text{H}}} - \text{Power}|_{\text{T}^{\text{L}}}}{\text{T}^{\text{H}} - \text{T}^{\text{L}}}\right|_{@V_{\text{dd}}} \tag{10}$$

where ${V_{\text{dd}}}^{\text{H}}$ and ${V_{\text{dd}}}^{\text{L}}$ are the higher and lower supply voltages and T^{H} and T^{L} are higher and lower temperatures, respectively. The power dissipation sensitivity with supply variations is 156.92 and 407.47 μW/mV at 25°C and 125°C

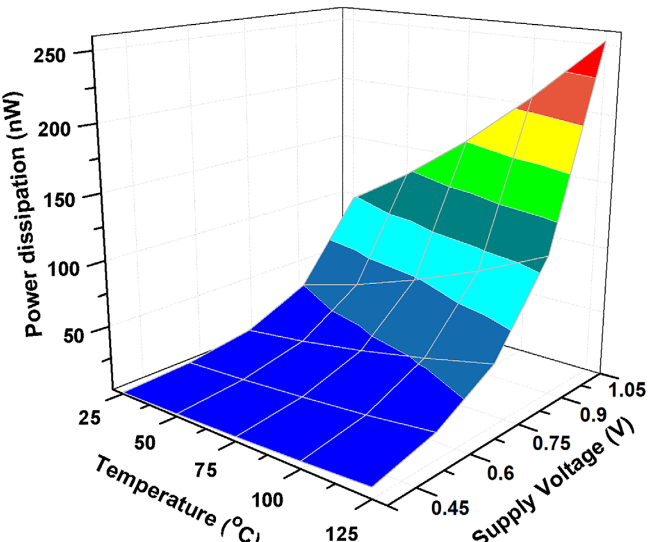

FIGURE 10 c17 circuit dynamic power dissipation with supply voltage and temperature variations

operating temperatures respectively, whereas, the power dissipation sensitivity with temperature variations are 71.49 μW/°C and 1.57 nW/°C at 0.45 and 1.05 V supply voltages, respectively. From the above discussions, we observe that the change in power dissipation sensitivity is greater for supply voltage variations as compared to the temperature variations. This indicates that the power dissipation sensitivity increases at a higher temperature and supply voltage.

4.3 | Effect of SET on c17 circuit

Figure 11 shows the critical charge at the sensitive node (S) of the c17 circuit for the input combination 00010 leading to maximum net stress for PMOS transistors. The stress time is considered to be 3 years in total. The result shows that the critical charge decreases with the stress time. Further, the critical charge at the sensitive node (S) for input combination 00010 is lower than 10010, and thus, the effect of SET is higher for 00010. The critical charge for the c17 circuit is decreased by 9.87% for the input combination 00010 after the stress time of 3 years, whereas, the critical charge is decreased by 6.72% in case the pattern 10010 is applied. This indicates that the soft error hardening of the circuit seriously depends on the NBTI stress of the PMOS transistor, on the selected input pattern of the circuit, and the logical masking and sensitization probability of the gates involved in the circuit.

Also, the effect of supply voltage and temperature variations on the critical charge at the sensitive node (S) of c17 circuit is analyzed, as shown in Figure 12. Results demonstrate that the critical charge increases with the supply voltage, whereas the critical charge decreases with increasing temperature. The critical charge sensitivity with supply voltage and temperature can be calculated as

$$\text{Sensitivity}_{Q_{\text{crit}}}\Big|_{@\text{T}} = \frac{Q_{\text{crit}}|_{V_{\text{dd}}^{\text{H}}} - Q_{\text{crit}}|_{V_{\text{dd}}^{\text{L}}}}{V_{\text{dd}}^{\text{H}} - V_{\text{dd}}^{\text{L}}}\Bigg|_{@T} \tag{11}$$

and

$$\text{Sensitivity}_{Q_{\text{crit}}}\Big|_{@V_{\text{dd}}} = \frac{Q_{\text{crit}}|_{\text{T}^{\text{H}}} - Q_{\text{crit}}|_{\text{T}^{\text{L}}}}{\text{T}^{\text{H}} - \text{T}^{\text{L}}}\Bigg|_{@V_{\text{dd}}} \tag{12}$$

The critical charge sensitivity with supply variations are 10.43 and 7.983 fC/V at 25°C and 125°C operating temperatures respectively, whereas, the critical charge sensitivity with temperature variations is 6.7 aJ/10°C and 153.4 aJ/10°C at 0.45 and 1.05 V supply voltages, respectively. From the above discussions, we can observe that the critical change

FIGURE 11 Critical charge at the sensitive node (S) of the c17 circuit for two worst-case input combinations with the different stress time

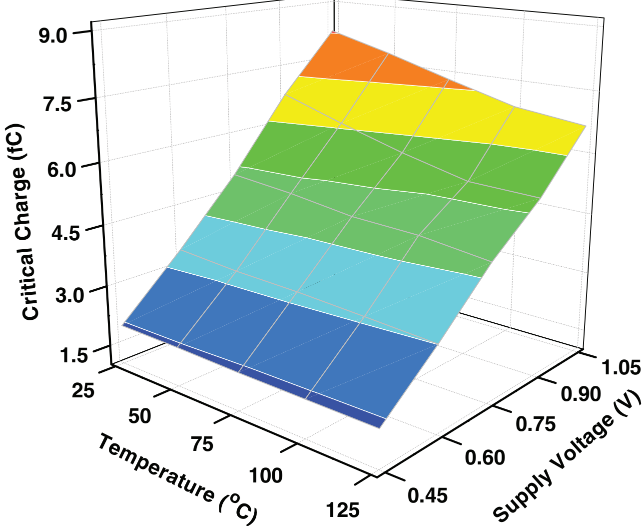

FIGURE 12 Critical charge variation at the sensitive node (S) of the c17 circuit with supply voltage and temperature variations for the input combination '00010'

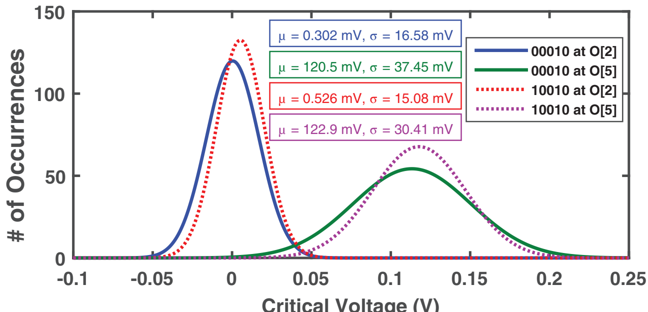

FIGURE 13 Monte Carlo distribution of the critical voltages at the sensitive node 'S' or O[2] and output O[5] of the c17 circuit for the input patterns having the maximum number of PMOS are under stress

sensitivity with supply voltage is higher as compared to the critical charge sensitivity with temperature. The critical charge at the sensitive node increases with supply voltage because the current driving capability of the circuit increases at higher supply voltage.

4.4 | Effect of process variations on c17 circuit

For the effect of process variations on the critical voltage at the sensitive node (S) and output node O[5], we have performed 5000 Monte Carlo simulations for the input combinations '00010' and '10010' as shown in Figure 13. We have considered only the O[5] output node because the signal probability is less as compared to the output node O[6], as shown in Figure 7. Results demonstrate that the effect of process variation is more at the sensitive node (S) and output

node O[5] for the input combination '00010' as compared to the '10010'. A higher deviation indicates that the sensitive node is more sensitive to the process variation as well as a single event transient.

5 | CONCLUSION

Performance degradation of transistors due to NBTI and single event transients occurring in ICs might give rise to unstable electronic applications. We analyze the effect of NBTI on the soft error susceptibility on two input NAND and NOR gates as well as on the ISCAS'85 c17 benchmark circuit. We show that NBTI significantly reduces the critical charge at the sensitive nodes of the circuits. We further introduce a soft error rate ratio (SERR) to validate the effect of NBTI at various operating temperatures and observe that the NAND gate and NOR gate is most sensitive to the soft error at the input combination AB = 01 and AB = 00, respectively. Further, we also determine the critical charge of the sensitive node for all possible worst-case input combinations of the c17 benchmark circuit. We also evaluate the critical charge sensitivity at the sensitive node of the c17 circuit with temperature and supply variations and observe that the critical charge sensitivity with supply variation is more as compared to temperature variations. The effect of process variations is considered using 5000 Monte Carlo simulations at the sensitive node of the c17 circuit. The result indicates that the c17 circuit is most sensitive to the soft error if the maximum number of PMOS transistors is under stress.

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