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High-performance radiation hardened NMOS only Schmitt Trigger based latch designs

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Abstract
CMOS circuits based on scaled transistors are typically more susceptible to soft errors caused by energetic particles in the radiation environment than circuits employing their large-area counterparts. In this paper, a soft error tolerant latch built on a Schmitt trigger, which is entirely realized with NMOS transistors with an additional voltage booster, which we refer to as NST-VB, is proposed. To evaluate the circuits' radiation resilience, we identify the most sensitive nodes by analyzing the critical charges at the various latches' internal sensitive nodes. We also examine the linear energy transfer (LET) of the essential latches and observe that the NST-VB latch has an improved LET of $0.386\text{MeVcm}^2/\text{mg}$ as compared to $0.231\text{MeVcm}^2/\text{mg}$ and $0.365\text{MeVcm}^2/\text{mg}$ for unhardened latch and ST latch, respectively. For the process variation analysis, we further examined 5k Monte Carlo simulations to analyze the impact of device variability on our design and observe that the proposed NST-VB latch has $1.96\times$ less variability critical voltage concerning the ST latch. Further, the logic flipping probability for NST-VB latch is 48.32% compared to 53.04% for ST latch. Also, the critical charge to power delay area product ratio (QPAR) is calculated and evaluated for the proposed latch's effectiveness compared to other considered latches.

Keywords Transient faults · soft errors · Single event transient · Radiation hardened latch · Robust design

1 Introduction

The advances of the semiconductor industry over recent decades has to transistors with highly optimized device geometries. With the scaling of the MOS technology, integrated circuits (ICs)' performance gets essentially improved. However, as the dimensions of devices employed in ICs have become reduced to a few tens of nanometers only, reliability issues become more severe for circuit designers [1]. In nanoscale CMOS technologies, circuit node capacitance becomes decreased due to continuous shrinking of supply voltage and transistors' feature size. Consequently, the respective charge stored at a node in the circuit becomes reduced, which has the disadvantage that the circuit gets more sensitive to the external noise sources, like neutron strikes or alpha particles stemming from the terrestrial environment [2].

In this context, the drain-bulk junction of transistors in the off-state connected to a node in a circuit can be very sensitive to radiation effects [3]. When high-energetic particles strike to the bulk of the transistor, they generate secondary electron-hole pairs collected at the drain region of the transistor. Those drain terminals act as a sensor node in the circuit and result in a glitch at the output of circuits, and this erroneous behavior is known as a transient fault (TF) [4]. The glitches may act as an electrical pulse and commonly referred to as single event transient (SET), which may be transferred through the combinational

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circuits if not appropriately masked. If elements such as latches and flip-flops are sequentially connected after the combinational circuits, these SETs can alter the logic states [5]. Also, the SET affects the stored charge at a specific node of storage elements. If the amount of charge exceeds the critical charge, the stored logic flipped, and this behavior is referred to as a single event upset (SEU) [6].

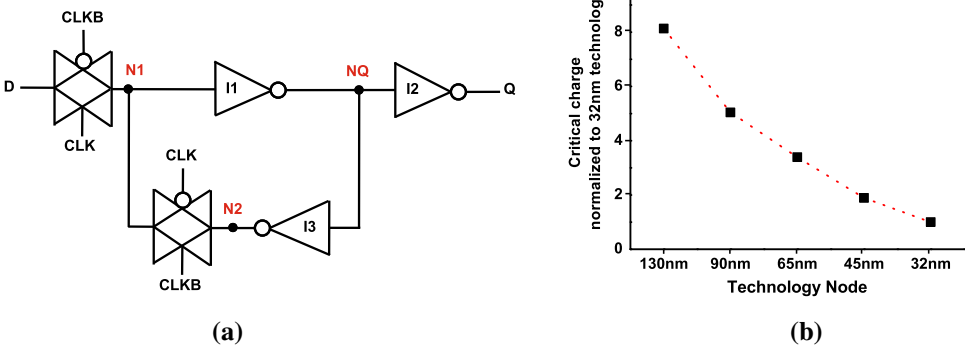
The general prediction of single event effect rates is typically based on event cross-sections as a function of the incident particle's stopping power and are known as linear energy transfer (LET). In electronic materials, the LET is a measure for the energy required to generate single electron/hole pairs per path length [7]. Historically protons have been expected to induce SEUs in memory circuits by indirect ionization when the particle's energy is higher than certain threshold energy, below which no upset is observed [8]. However, with the improvements of the integrated devices, the amount of charges stored on a single node in a circuit has been significantly reduced, so also low energy protons could generate sufficient amount of charge by direct ionization to cause SEU. Thus for modern technologies, low energy protons can potentially be considered a major contributor to soft errors [9]. Nowadays, terrestrial neutrons radiation is considered one of the primary sources of soft error in microelectronics circuits at sea level [10]. Especially neutrons below 10MeV build a large portion of the terrestrial neutron spectrum [11]. Even though neutrons are incapable of direct ionization, they produce energetic secondary ions by interacting with semiconductor materials, which can induce enough ionizing energy to cause SEUs. A recent report shows that the neutrons with energy below 10MeV can be made responsible for SEU in SRAMs and latches [12].

Several approaches have been proposed to enhance the soft error tolerance for logic circuits like latches. However, such designs typically affect performance, power consumption, chip area, and the operational speed significantly of the circuit. The radiation hardening methods for latches can be roughly classified into two categories [13]. (i) The hardened circuits are considered independent of the size of transistors and the node capacitances. The DICE [14] latch is one of the examples for the first category of radiation hardening. This latch tolerates the soft error for its internal nodes without increasing the node capacitance and the transistor geometry. The node voltage, which the SEU affects, can be driven back to its previous voltage by the other transistors in the cell. (ii) The hardening of the circuit is increased by increasing the node capacitance. In this context, increasing the gate capacitance of the critical sensitive node is one of the common methods to increase circuits' radiation hardening. A soft error masking using Schmitt trigger circuit (SEM latch) [15] and conventional Schmitt trigger based latch [16, 17] are the examples for the second category of the radiation hardening [18].

The illustration of a conventional unhardened latch is given in Fig.1(a). In this work, the conventional unhardened latch is used as a reference latch. According to [19], the internal nodes N1, N2, and NQ are more sensitive to soft errors than the other nodes. Therefore, we focus more on analyzing the soft error vulnerability by evaluating the circuit's electrical properties at the internal nodes N1, N2, and NQ. Figure 1(b) shows the critical charge normalized values at the internal nodes of the unhardened latch with the different technology nodes. The result shows that the critical charge reduces with device scaling because of reduced supply voltage and node capacitance. Therefore, it is essential to design highly robust latches for scaled technologies, mainly in harsh environments.

Several methods have been proposed recently to improve the soft error robustness of the latches. For instance, the feedback mechanism in the Sin-LC radiation-hardened latch [19] gives strong protection to internal nodes but is not able to shield the output nodes of the latch from external radiations. A second example is the soft error masking (SEM) latch is proposed in [15, 20] as shown in Fig. 2(a). In the SEM latch, two additional transistors are added to the feedback inverter to achieve an Schmitt trigger (ST) arrangement to improve the critical charge at the internal node N2. A modified SEM (M-SEM) proposed in [21] shown in Fig. 2(b) to improve the critical charge at the internal node N1. It requires two additional inverters and two transistors in the forward path to improve the internal node critical charge. A high-efficiency time redundant hardened latch (HETR-HL) is proposed in [22] which uses the combination of SIN-LC and ST based structure. To circumvent the issue of unprotected output node, a ST based radiation-hardened latch design has been suggested in [16], as shown in Fig. 2(c). This circuit relies on introducing an ST inverter [23] in place of the inverter I1 of the unhardened latch to shield the internal nodes against TF. This latch demonstrates enhanced hardening performance against radiation as compared to its unhardened counterpart. The only drawback is that the ST-based latch shows an increased delay ST circuit's hysteresis effect.

To further improve the ST-based solution concerning radiation hardening, we recently proposed a Schmitt trigger with voltage booster which is entirely based on nMOS transistors (NST-VB) [24, 25] which provides a soft error tolerant inverter circuit, and has been simulated considering the 32nm PTM technology model [26] using HSPICE [27]. To compare our results with the hardened design, we replace the inverter I1 of the unhardened latch is replaced by NST-VB inverter similar to the I1 is replaced by the ST inverter in [16]. Subsequently, we perform extensive simulations, and the results are discussed and



(a) (b)

Fig. 1 **a** Circuit of an unhardened reference latch. The input node is D and the output is Q. The nodes N1, N2, and NQ are considered as the internal nodes. The signals CLK and CLKB are for the system clock, **b** Normalized critical charge for several technology nodes. The given amount for the critical charge is normalized to the 32 nm CMOS technology

compared to the unhardened latch and ST based latch designs. Further, we analyzed the most sensitive nodes, process variation, temperature variation, and supply voltage variation in terms of critical charge (Q_{crit}) for the considered latches.

2 Soft error modeling

The soft error occurs when the collected charge generated by radiation noise at the sensitive node exceeds a specific critical charge (Q_{crit}). The critical charge represents the minimum amount of charge required at a sensitive node to flip the circuit's logic state. It is a widely used parameter to analyze the impact of soft error issues on devices and circuits.

The transient fault modeling or equivalent circuit, which is typically used for charge injection, is shown in Fig. 3, and discussed in [28] in more detail. A soft error can be generated by a current pulse with a high amplitude in the simulations with a short pulse duration. The amplitude of the current pulse represents the strength of the single event upset and depends on the environmental conditions and radiation noise strength. Figure 3(a) gives the equivalent circuit if the logic high is stored at the internal node, and the α particle generates a negative glitch. To simulate the impact of soft error on an NMOS transistor, the current pulse is injected at the drain contact of the NMOS transistor which can cause a negative glitch. This glitch forces the output voltage to get pulled down to logic low. Similarly, Fig. 3(b) gives the equivalent circuit to model the soft error affecting a PMOS transistor for a logic low stored at the internal node. In this case, a positive glitch can get generated, and the output state gets pulled up to the logic high state.

2.1 Radiation hardening analysis methodology

To analyze the SEU in the circuits, the current induced by α-particles gets modeled by a double exponential (DE) current source [29] is expressed as

$$I_{inj}(t) = I_{peak} \times (e^{-t/\tau_f} - e^{-t/\tau_r}). \quad (1)$$

However, SEU fault simulation using the DE current model is not sufficiently accurate for latches based on advanced technologies [30]. Thus this model is extended to the dual DE (DDE) current model [31] for the various phases as

$$I_{inj}(t) = \begin{cases} 0; & \text{if } t < t_{d1} \\ I_{peak} \times \left(1 - e^{\frac{-(t-t_{d1})}{\tau_r}}\right); & \text{if } t_{d1} < t < t_{d2} \\ I_{peak} \times \left(e^{\frac{-(t-t_{d2})}{\tau_f}} - e^{\frac{-(t-t_{d1})}{\tau_r}}\right); & \text{if } t > t_{d2} \end{cases} \quad (2)$$

where the peak value of the current injected at the respective sensitive node is given byI_{peak}. The parameters τ_f and τ_r are material dependent time constants. t_{d1} and t_{d2} are the onset of the rise and fall of the current, respectively. According to [32], we use $\tau_r = 1$ ps and $\tau_f = 50$ ps in our simulations.

The critical charge Q_{crit} is calculated after injecting the current pulse equivalent to particle strike at the circuit's sensitive node. We evaluate the minimum duration and magnitude of the caused current pulse, which is needed to flip the output logic of a latch circuit. So the Q_{crit} is extracted by integrating the current pulse over the time interval $t = 0$ to $t = T_{crit}$, and is given by

$$Q_{crit} = \int_0^{T_{crit}} I_{inj}(t)\mathrm{d}t \quad (3)$$

where $I_{inj}(t)$ is the injected current pulse at the sensitive node used for SEU analysis.

The detailed flow for calculating the soft error rate of different inverters and latches considering various supply voltages and operating temperature is depicted in Fig. 4.

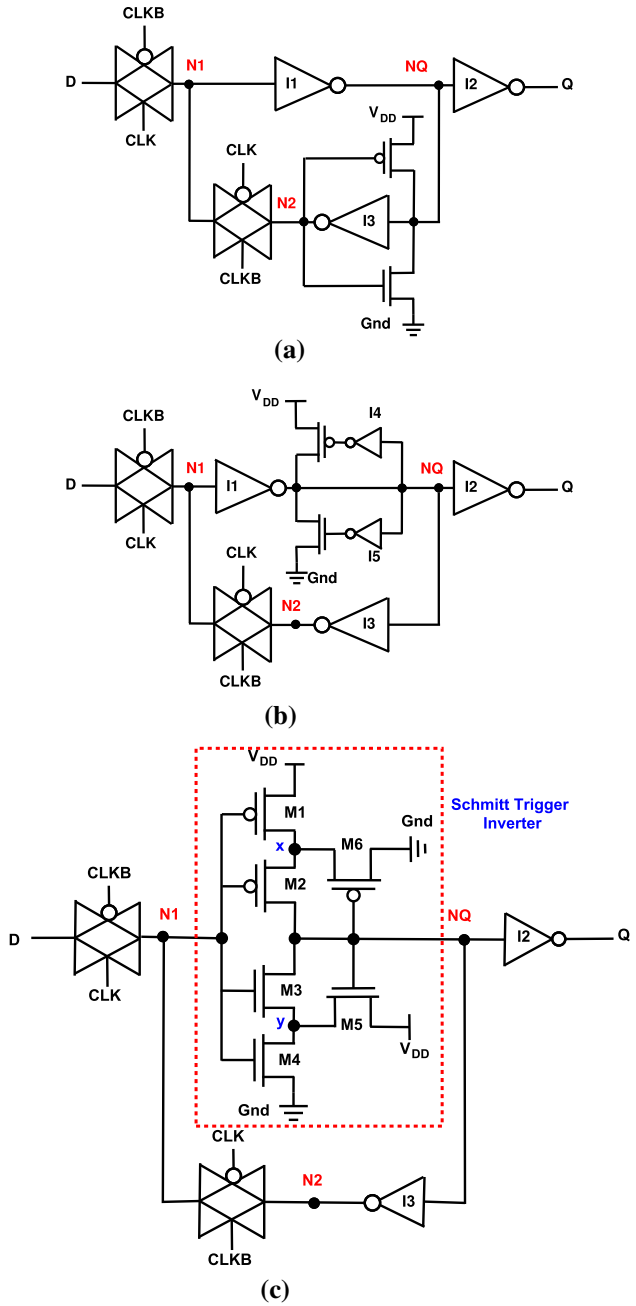


Fig. 2 Schematic circuit diagram of **a** soft error masking (SEM) latch, **b** modified soft error masking (M-SEM) latch, and **c** Schmitt trigger (ST)-based latch

2.2 Soft error rate

In the case of a high energy particle inducing a charge, it can be collected at one of the sensor nodes of the circuit. In the most unfortunate case, this can cause a sudden change of the logic value of the respective circuit node. The flipping of logic levels due to the above issues is known as the soft error. The soft error robustness of the circuits is analyzed with the soft error rate. At deep submicron

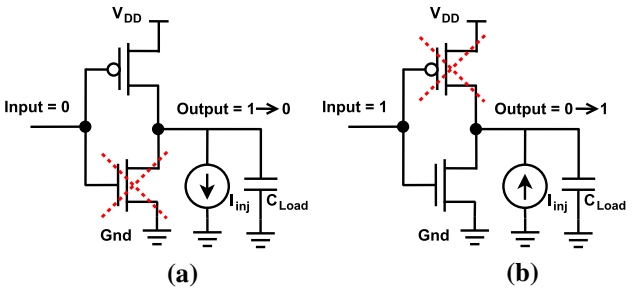


Fig. 3 SET injection model for a CMOS inverter: **a** negative tranisent pulse for the soft error at the NMOS transistor **b** positive transient pulse for the soft error at the PMOS transistor. The transistors marked with the red cross are considered affected by an α particle

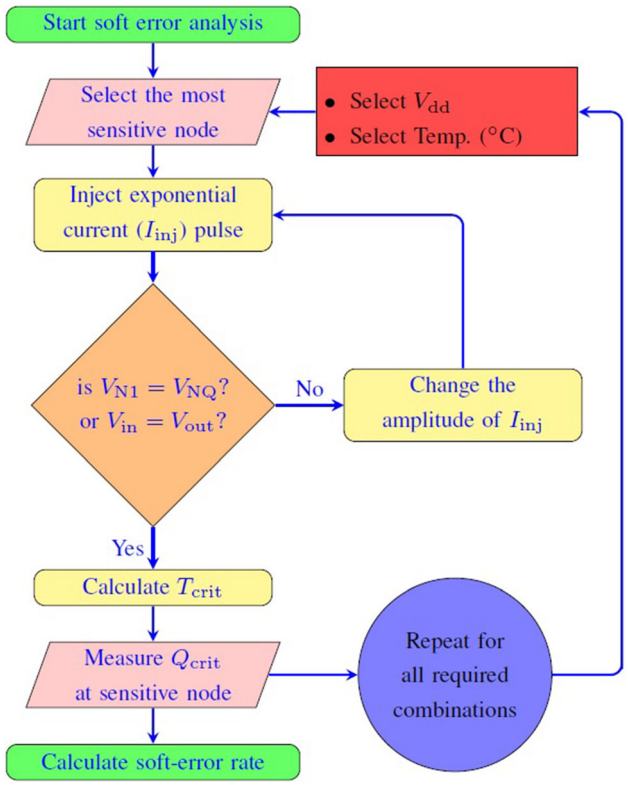


Fig. 4 Simulation flow of radiation hardening analysis with different supply voltages and operating temperatures. The conditions $V_{in} = V_{out}$ and $V_{N1} = V_{NQ}$ are used during the soft error hardening analysis of inverters and latches, respectively

technology, the circuits are highly sensitive to soft errors because smaller node capacitances and small critical charges are attributed to the lower supply voltages. The critical charge is used to analyze the soft error tolerance of the circuits. The soft error rate (SER) exponentially depends on the Q_{crit} and observed that the SER decreases with a higher value of Q_{crit} [33]. The SER can be expressed as

$$\mathrm{SER} \propto N_{\mathrm{flux}} A e^{-\frac{Q_{\mathrm{crit}}}{Q_S}} \tag{4}$$

where N_{flux} is the neutron flux intensity in particles per ($\text{cm}^2 \times$ s), A is the cross-section area of the sensitive node in cm^2, and Q_S is the charge collection efficiency of the device in fC. The above equation shows that only a small increase in Q_{crit} can significantly reduce the SER.

To analyze the soft error rate of the various latches compared to unhardened latch (UL), an inter-latch SERR is calculated for different supply voltages and operating temperature conditions [34]. The approximate inter latch soft error rate ratio ($\text{SERR}_{\#}$) for the considered latch is introduced assuming all other parameters unaffected except Q_{crit} for particular operating temperature and supply voltage. The $\text{SERR}_{\#}$ is normalized to the unhardened latch and is given as

$$\text{SERR}_{\#} = \left.\frac{\text{SER}_{\#}}{\text{SER}_{\text{UL}}}\right|_{@\text{V}_{\text{DD}}\text{andT}} \tag{5}$$

or alternatively as

$$\text{SERR}_{\#} \approx \text{Antilog}_{\text{e}}\left[Q_{\text{crit}}^{\text{UL}} - Q_{\text{crit}}^{\#}\right]\Big|_{@\text{V}_{\text{DD}}\text{andT}} \tag{6}$$

where $\text{SER}_{\#}$ and SER_{UL} are the soft error rates, and $Q_{\text{crit}}^{\#}$ and $Q_{\text{crit}}^{\text{UL}}$ is the amount of the critical charges for the considered latch and reference unhardened latch, respectively. The latch for which SERR needs to be analyzed is indicated with '#'. Note that a smaller $\text{SERR}_{\#}$ of any latch leads to a smaller impact of the soft error on the proper functionality of the examined latch.

3 Analysis of the radiation resilience of inverters

As previously mentioned, in our work, we propose to consider an NST-VB to inverter I1 in the unhardened latch. This topology achieves a further improvement of the soft-error hardening of the latch. Before analyzing latches in detail, we have to perform a hardening analysis of inverter circuits, an essential component for designing latches. For our radiation hardening analysis of the inverters, we consider the circuits of a CMOS inverter, an ST inverter, and an NST-VB based inverter.

The main feature of the NST-VB circuit is that entirely NMOS transistors are used in the most critical circuit paths. This can be achieved by replacing the PMOS transistors from the pull-up network (PUN), which are M1, M2, and M6 from Fig. 5(a). The schematic of the inverter's circuit considering the NST-VB is shown in Fig. 5(b), which is the combination of an NMOS inverter and ST based inverter. The NMOS inverter has the problems of reduced maximum output voltage ($V_{\text{DD}} - V_{\text{th,n}}$), small noise margin, and short circuit current from V_{DD} to ground. In the NMOS inverter,

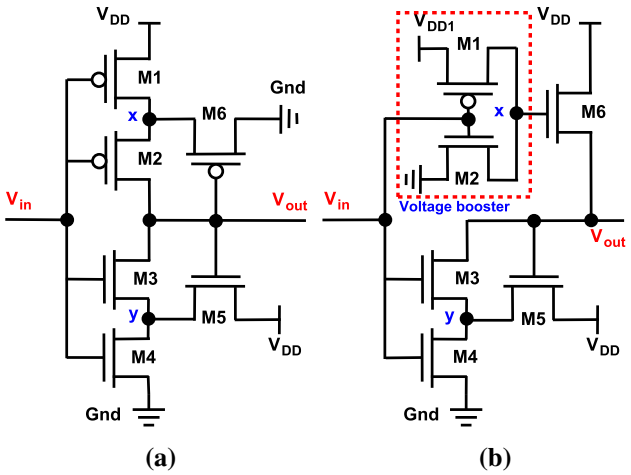


Fig. 5 Schematic of **a** classical Schmitt trigger based inverter circuit and **b** NMOS only Schmitt trigger with voltage booster (NST-VB) based inverter circuit. The voltage booster is the pass transister logic with a slightly higher supply voltage $V_{\text{DD1}} = V_{\text{DD}} + V_{\text{th,n}}$

the PUN is always ON, which leads to the short circuit current when the pull-down network (PDN) becomes turned ON. To avoid potential circuit short-cuts, a voltage booster (VB) is utilized to control the PUN, as shown in Fig. 5(b). The voltage booster's benefit is to increase the output voltage swing and overcome the direct current problem. Additionally, the voltage booster's supply voltage $V_{\text{th,n}}$ is intentionally selected higher than the V_{dd}, which provides the complete voltage swing.

The analysis considering radiation hardening of the ST based inverter is slightly more complicated than the CMOS inverter as the new design exhibits two additional internal storage nodes. In the case of V_{in} being at logic low, node V_{out} is logic high, which puts transistor M5 in its conductive state. Thus node y will get charge. If now a TF causes a node to flip from logic low to logic high, the charge stored at node y has to be removed to change the state of output node V_{out}. Similarly, in case of a negative pulse strike at the input node V_{in}, the charge stored at node x has to be removed. As a consequence, the ST circuit provides better robustness to the soft error due to the charges at the internal nodes x and y.

If we consider the circuit from Fig. 5(b) from the radiation hardening perspective, the situation is different for the CMOS and ST-based inverter. As only NMOS transistors drive the NST-VB circuit's output, the only critical condition that needs to be considered is the input state logic '0', and the corresponding output state logic '1'. In this case, the only sensitive region is the drain junction of the transistor M3, where a high energy particle hit could induce a negative glitch at the output of the inverter. In the opposite case, when the input is logic '1' and the output is logic '0', the transistors M4 and M3 are in the ON state,

whereas transistor M6 is in the OFF state. If now a SET occurs at node x, a glitch could turn ON transistor M6 and get so propagated to the output of the circuit. But in this case, a large amplitude of the SET is required to generate the glitch at the output, because due to the feedback-controlled PDN the glitch recovers very fast and suppresses a SET at the circuit output. In this case, the only potential sensitive region is the drain junction of M6. However, no electric field in this region could lead to a separation of generated electron-hole pairs to enforce a net charge that alters the output voltage. The voltage drop across this junction remains negligible as the drain and substrate are both held at ground potential [25].

The critical charge of different sensor nodes for CMOS, ST, and NST-VB based inverter circuits are shown in Table 1. Here, NA indicates no flipping of logics or no critical charge, and *Z* indicates the high impedance state. For specific sensor nodes of the circuits, the critical charge can not be calculated because there is no logic flipping at the output when SETs occur at the respective sensor nodes. From the simulations, we can observe that the sensitive node V_{out} of the inverter circuit has a lower critical charge compared to all other sensitive nodes. It has to be noted that the critical charge for the NST-VB circuit is 78.09% and 47.8% higher as compared to the CMOS and ST circuits, respectively. Further, we also analyze the critical charge at the sensitive node of the considered inverters with the supply voltage variation ranging from 0.3V to 0.9V, as shown in Fig. 6. Results show that the critical charge increases with supply voltage for the investigated inverter circuits because the higher supply voltage provides more conduction current, which increases the charge at the sensitive node. It is also observed that the critical charge for the NST-VB inverter is higher than for the other circuits; hence it can be beneficial for designing latches with better radiation hardening than ST-based latch.

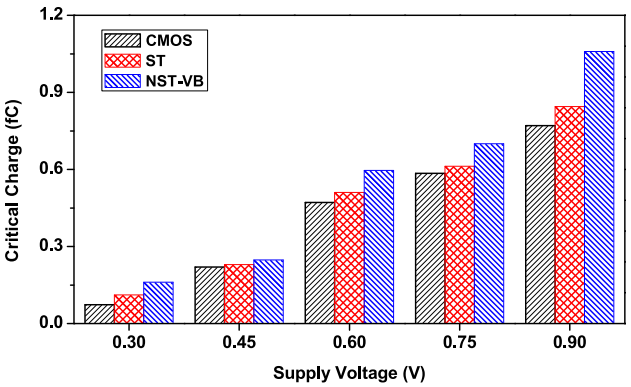


Fig. 6 Critical charge extracted at the most sensitive nodes (V_{out}) of the different inverter circuits at the elevated temperature (125 °C) considering V_{in} = 1

4 Proposed NST-VB based latch

As previously discussed, the NST-VB inverter has better radiation hardening than the CMOS inverter and ST based inverter. This improvement can be beneficial for the design of radiation-hardened latches and SRAM cells. In this work, we are utilizing the benefits of NST-VB against the radiation hardening to design the soft error tolerant latch, which can be of interest for applications in harsh environments. Figure 7 shows the proposed NST-VB inverter-based radiation-hardened latch [35]. To improve the radiation hardening of the NST-VB circuit, an inverter is added to the transparent path of the latch.

When the N1 is logical low, the node NQ is logically high, which sets transistor M5 in its ON state, and charges node *y*. If a TF on a node goes from low to high, the charge at node *y* needs to be removed first to change the state of node NQ. Similarly, when there is a negative pulse strike at node N1, it transfers to node *x*, which needs to be discharged. As the voltage booster has a higher supply voltage, the node voltage at *x* will not wholly discharge, which withstands the logic value at the node NQ. Therefore, the NST-VB circuit provides better robustness to the soft errors due to the charges stored at the internal nodes *x* and *y*.

Table 1 Critical charge extracted at all possible sensitive nodes of different inverter circuits

Logic circuits	Sensitive flipping	Logic nodes	Critical charge (fC)	
			V_{in} = 0	V_{in} = 1
CMOS	V_{out}	Yes	0.857	0.776
ST	V_{out}	Yes	2.605	0.935
	x	No	NA	NA
	y	No	NA	NA
NST-VB	V_{out}	Yes	2.628	1.382
	x	No	Z	NA
	y	No	NA	NA

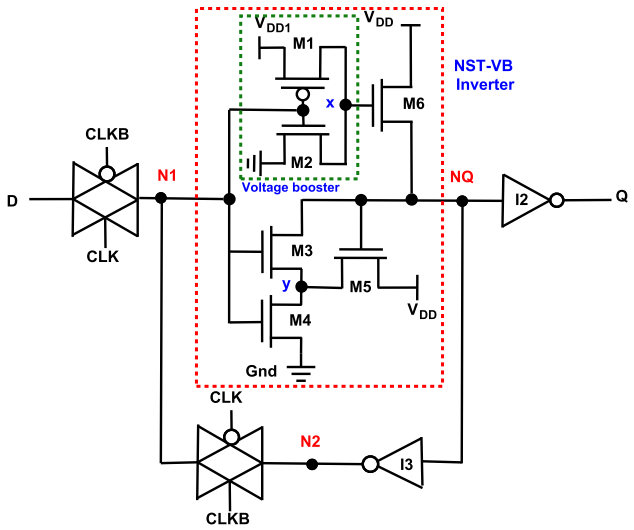


Fig. 7 Schematic circuit diagram of the proposed NST-VB based hardened latch

For further radiation-hardened improvement, it would be conceivable that all three inverters in the unhardened latch can be replaced with the NST-VB inverter. However, this would significantly increase the circuit complexity. In the latch circuit, if the CLK is at logic '0', the circuit operates in latch mode, whereas when the CLK is at logic '1', the circuit is in transparent mode. We have considered all the analysis in the latch mode because the radiation's impact is more severe in this mode [16].

5 Evaluation and comparison of latches

In this section, the effectiveness and performance of latches considering radiation-hardening are investigated using the PTM 32nm CMOS model [26]. All simulations are performed using HSPICE [27] considering a supply voltage of V_{DD} = 0.9 V and the operating temperature is set to room temperature $T = 25\,^{\circ}\mathrm{C}$.

Table 2 shows the different performance parameters of various latches discussed in the manuscript. The inverter circuit is the basic building block to design a latch. To improve the latches' soft error robustness, a different variant of inverter circuits, including various type of Schmitt trigger circuits are used. NST-VB based inverter is the improved version of the ST circuits reported in [16, 20, 21] to improved the soft-error robustness and used in the proposed NST-VB based latch to enhance the robustness further. From results, it is observed that the critical charge for ST based latch [16] is higher than the SEM [20], M-SEM [21], and SIN-LC [19]; hence we considered unhardened latch, ST based latch, and proposed NST-VB based latch for further analysis.

5.1 Critical charge analysis

We started our analysis by evaluating the critical charges at all possible internal nodes N1, N2, and NQ for the reference latch, the ST latch, and the proposed NST-VB latch, as illustrated in the Fig. 8. Results demonstrate that the node N1 exhibits the smallest critical charge for all the considered latches. Further, we analyze that node N1 is having around two times lower critical charge than the node N2 for all three latches. Likewise, node N1 of latches having 5.31×, 4.12×, and 6.28× lower critical charge than at the node NQ for the unhardened latch, ST latch, and NST-VB latch, respectively. As node N1 shows the smallest critical charge for all considered latches, it is most sensitive to the radiations and higher chances of soft errors. Based on the above discussions, we discussed node N1 precisely for the rest of the analysis.

Figure 9 shows the transient fault injection at the most sensitive node N1 of the proposed NST-VB based latch. From our results, it can be observed that the proposed NST-VB latch requires a higher transient fault injected charge (7.961fC) to flip the stored logic of the latch.

5.1.1 Linear energy transfer

In many cases, instead of critical charge, effective linear energy transfer (LET) is used to express the device SEU [36]. These critical charges and the LET are related by

$$Q_{\mathrm{crit}} = \frac{\mathrm{LET_{th}} \times T_{\mathrm{BOX}} \times d \times e}{X} \tag{7}$$

where Q_{crit} is the critical charge (in pC), $\mathrm{LET_{th}}$ is the threshold effective LET (in $\mathrm{MeVcm^2/mg}$), T_{BOX} is the device thickness (in μm), d is the material density ($2.32\mathrm{g/cm^3}$ for Si), e is the electronic charge (1.602×10^{-7} pC) and X is the energy needed to create one electron-hole pair (3.6eV in Si).

In our study, the injection of charge at a sensitive node is considered equivalent to an α-particle having the energy of <10MeV, which gives a LET of less than $1\mathrm{MeVcm^2/mg}$. Figure 10 shows the LET at the sensitive node of different latches considering two operating temperatures of $T = 25\,^{\circ}\mathrm{C}$ and $T = 125\,^{\circ}\mathrm{C}$. Results demonstrate that the LET of the proposed NST-VB latch is higher than for the unhardened latch and ST latch. The LET for the NST-VB latch at $T = 25\,^{\circ}\mathrm{C}$ is $0.386\mathrm{MeVcm^2/mg}$ as compared to $0.231\mathrm{MeVcm^2/mg}$ and $0.365\mathrm{MeVcm^2/mg}$ for the unhardened latch and ST latch, respectively. Similarly, the LET for the NST-VB latch at $T = 125\,^{\circ}\mathrm{C}$ operating temperature is $0.324\mathrm{MeVcm^2/mg}$ as compared to $0.182\mathrm{MeVcm^2/mg}$ and $0.306\mathrm{MeVcm^2/mg}$ for the

Table 2 Comparison of various performance parameters for different latches

Performance parameters ↓	Latches						
	Reference	SEM [20]	M-SEM [21]	SIN-LC [19]	HETR-HL [22]	ST [16]	NST-VB
Critical charge (fC)	4.755	5.855	6.609	7.916	8.678	7.539	7.961
Dynamic Power (μW)	6.425	5.810	6.118	6.530	8.401	5.978	0.141
t_{setup} (ns)	0.750	0.750	0.750	0.750	0.750	0.750	0.750
t_{CLK-Q} (ns)	0.166	0.182	0.188	0.173	0.276	0.201	0.387
t_{delay} (ns)	0.916	0.932	0.938	0.923	1.026	0.951	1.137
Area (μm^2)	2.295	3.505	4.007	1.826	7.094	2.726	3.275
PDP (fJ)	5.885	5.413	5.736	6.026	8.620	5.685	0.160
QPAR	0.352	0.309	0.288	0.720	0.142	0.486	15.163

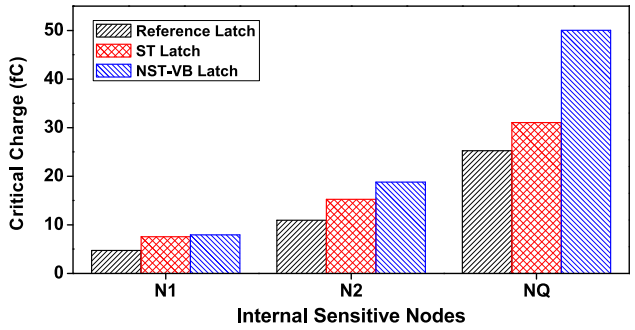


Fig. 8 Critical charge at the internal sensitive nodes of three different latches

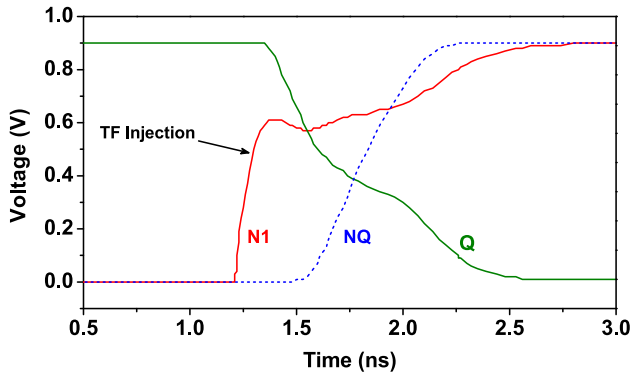


Fig. 9 Characteristics of the transient fault injection at the sensitive node N1 of the proposed NST-VB based latch

unhardened latch and ST latch, respectively. The results show that the LET of all the considered latches decreases with increasing operating temperature . Also the improvement in LET for the proposed NST-VB latch is higher at $T = 125\,^{\circ}C$.

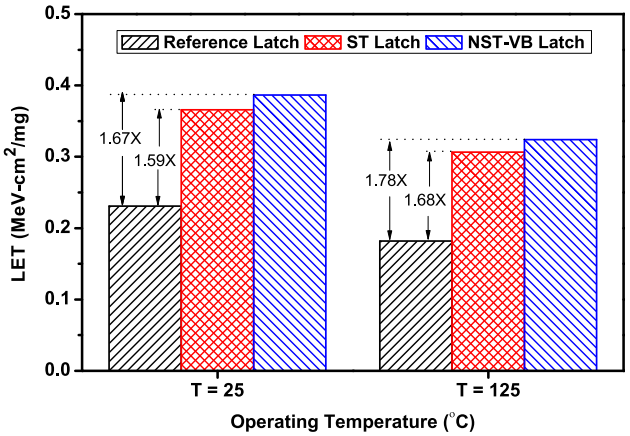


Fig. 10 LET threshold for the sensitive node N1 of different latches at operating temperatures $T = 25\,^{\circ}C$ and $T = 125\,^{\circ}C$

5.1.2 Soft error rate ratio

For the effectiveness of the soft error hardening of the proposed NST-VB latch compared to the unhardened latch, we analyze the inter latch SERR for all the considered latches, as shown in Fig. 11. The inter latch SERR for all

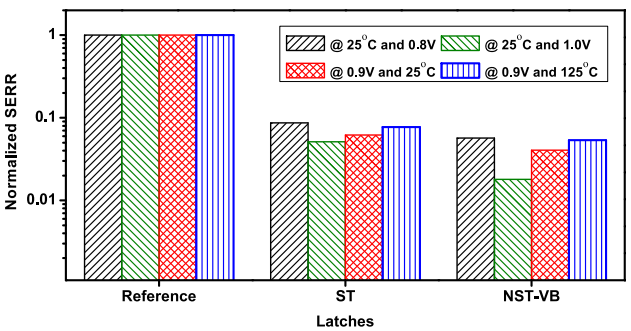


Fig. 11 Inter-latch soft error rate ratio for different latches at the four extreme combinations of supply voltage and operating temperature. The SERR is normalized to unhardened reference latch for all the combinations

the considered latches are normalized to the unhardened latch for different combinations of operating temperature and supply voltage. In this work, we have calculated SERR considering supply voltages of 0.8V and 1V at the operating temperature of 25 °C. The SERR is also calculated for the operating temperatures 25 °C and 125 °C at the supply voltage of 0.9V. The results show that the SERR for the proposed NST-VB latch is minimum for all the combinations as compared to the unhardened and ST based latches for all the considered combinations of operating temperatures and supply voltages.

The results demonstrate that the SERR improves when the circuit operates at the lower operating temperature and higher supply voltage. In our analysis, the maximum improvement in SERR is when the supply voltage is 1 V, and the operating temperature is 25 °C. Higher supply voltage increases the current flowing through the circuit and increases the critical charge at the sensitive node. Similarly, the critical charge at the sensitive node decreases with the increase in operating temperature, which leads to increased SERR at a higher temperature. The proposed latch has better radiation hardening from the above discussions if we operate them in super-threshold conditions and at room temperature.

5.1.3 Effect of supply voltage and temperature variations

The impact of voltage and temperature variations on the soft error tolerance is an important measure for stable circuit operation. We analyze the effect of supply voltage and temperature variations on the critical charge at the sensitive node of the previously mentioned latches.

The effect of supply voltage and temperature variations on the critical charge of node N1 is shown in Fig. 12. Figure 12(a) gives the evolution of the critical charge with supply voltage variation in the range of 0.8–1 V for different circuits. The results show that the critical charge at the sensitive node increases with the supply voltage. It is because the node capacitance increases with the supply voltage. We also observed that the critical charge for proposed NST-VB based latch is higher than the unhardened latch and ST based latch. It indicates that the proposed NST-VB based latch has better soft error hardening caused by supply variations. The critical charge of the proposed NST-VB latch is 1.74× and 1.07× higher than the unhardened latch and ST based latch, respectively, at the supply voltage of 0.8 V. Similarly, the critical charge at 1 V supply voltage is 1.75× and 1.12× higher for NST-VB latch as compare to reference latch and ST latch, respectively.

Figure 12(b) shows the trend of the critical charge within the temperature range from 25 to 125 °C. The critical charge of all the latches decreases with the increasing operating temperature. The absolute decrease of the critical charge of NST-VB based latch has the smallest decrement of 16.11% with temperature changing from 25 to 125 °C. Further, the proposed NST-VB latch's critical charge is 1.67× and 1.06× higher than the unhardened latch and ST based latch at $T = 25$ °. Similarly, the critical charge at $T = 125$ °C is 1.78× and 1.06× higher for NST-VB latch compared to reference latch and ST latch, respectively. Based on the above discussions, the variation on the critical charge of the proposed NST-VB based latch is less with the change in operating temperature. Further, the NST-VB latch has a higher critical charge than the unhardened latch and ST-based latch, indicating that the proposed latch has better soft error robustness.

5.2 Analysis of power dissipation

We also analyze the dynamic power dissipation of the latches within the voltage range of 0.8–1 V at $T = 25$ °C and for the temperature range $T = 25$ °C to $T = 125$ °C at a supply voltage of 0.9 V, as shown in Fig. 13. The result shows that the power dissipation increases with the supply voltage and operating temperature for all three latches. Figure 13(a) shows the power dissipation for the supply voltage range from 0.8 to 1 V for different latches, and we can observe that the power dissipation for the proposed

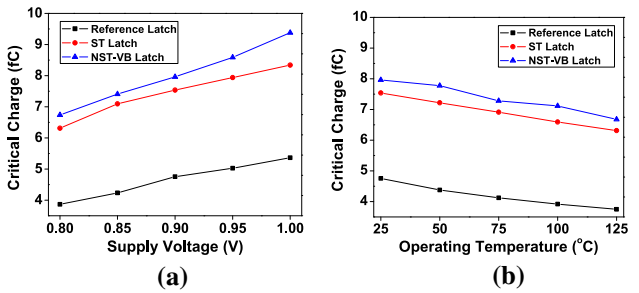


Fig. 12 Critical charge at the most sensitive node N1 of different latches for **a** different supply voltages at room temperature $T = 25$ °C and **b** different operating temperatures at $V_{DD} = 0.9$ V

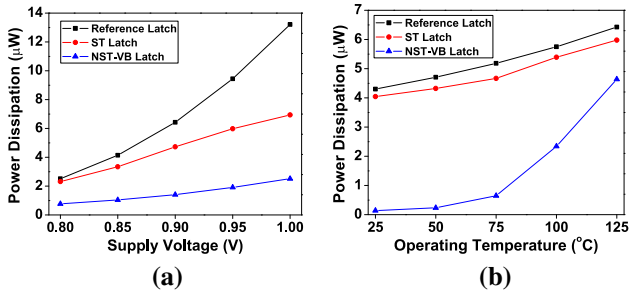


Fig. 13 Power dissipation of different latches for **a** different supply voltages at $T = 25$ °C and **b** different operating temperatures at $V_{DD} = 0.9$ V

NST-VB latch is the lowest compared to the unhardened and ST based latches. It is also observed that the power dissipation changes if the supply voltages is switched from 1 to 0.8 V for an unhardened latch, ST latch, and NST-VB latch with values of $10.7W$, $4.62W$, and $1.74W$, respectively. Further, the NST-VB latch has $3.26\times$ and $3.01\times$ lower power dissipation as compared to reference latch and ST latch, respectively, at the supply voltage of 0.8 V. Also, the power dissipation at 1 V for NST-VB latch is $5.25\times$ and $2.76\times$ lower as compared to the reference latch and ST latch, respectively. The above discussion indicates that the proposed latch is power efficient even with the supply voltage variations. The lower power dissipation for the ST latch and NST-VB latch is because of the use of stacked transistors and feedback network used in the inverter circuit. Further, the faster transition in the NST-VB inverter reduces the short-circuit power dissipation, which leads to reduce the dynamic power dissipation effectively.

Additionally, Fig. 13(b) shows the power dissipation with temperature variations from $T = 25\,^{\circ}\mathrm{C}$ to $T = 125\,^{\circ}\mathrm{C}$ for various latches and observed that the power dissipation with temperature variation is less for NST-VB based latch as compared to the unhardened and ST based latch. The power dissipation of the NST-VB latch is $1.38\times$ and $1.29\times$ lower as compared to the unhardened latch and ST latch, respectively, at $T = 125\,^{\circ}\mathrm{C}$. Further, we also evaluated the leakage current of the considered latches during latch mode. The leakage current for the unhardened latch, ST latch, and NST-VB latch is 18.3nA, 18.4nA, and 20.9nA, respectively. The leakage current of the NST-VB is slightly higher than the unhardened and ST based latches due to the dual supply voltage is used in the NST-VB latch.

5.3 Timing and delay

Figure 14 shows the timing diagram and the transient response of the proposed NST-VB based latch. The signals CLKB and CLK are the system clocks, D is the data input, Q is the data output, and N1, N2, and NQ are the internal sensitive nodes of the latches. The parameters $t_{\mathrm{D-Q}}$ and $t_{\mathrm{CLK-Q}}$ are the propagation delay of the latch from data input D to output Q, and CLK to output Q, respectively. The value for t_{setup} is the minimum time between a change in the data signal D and the trailing edge of the CLK in a way that the new value of D can propagate to the output Q of the latch [16]. Hence, the total latch propagation delay is given by

$$t_{\mathrm{delay}} = t_{\mathrm{setup}} + t_{\mathrm{CLK-Q}}. \tag{8}$$

The various delay and timing components for all the considered latches are summarized in Table 2, considering $T = 25\,^{\circ}\mathrm{C}$ and a supply voltage of 0.9 V. Results show that t_{delay} for the NST-VB based latch is higher as $t_{\mathrm{CLK-Q}}$ is more extensive than for the reference circuit. The total latch delay is $1.24\times$ and $1.19\times$ higher than the reference latch and ST latch, respectively. The increase in $t_{\mathrm{CLK-Q}}$ for NST-VB latch is due to no feedback mechanism in the pull-up network of NST-VB inverter, whereas the ST inverter has the feedback mechanisms in both PUN and PDN, which provides the fast transitions. However, $t_{\mathrm{D-Q}}$ for the proposed NST-VB latch is lowest compared to the unhardened latch and ST based latch.

We also analyze the effect of supply voltage and temperature variations on the propagation delay for various latches. The propagation delay decreases with the supply voltage because higher supply voltage provides a higher current through the devices, leading to effectively faster switching, which reduces the delay. However, the propagation delay increases with the rise in operating temperature because the carrier mobility decreases with the temperature increases [2]. Figures 15 and 16 show the $t_{\mathrm{CLK-Q}}$ and $t_{\mathrm{D-Q}}$, respectively, at different supply voltages and temperatures. Results demonstrate that the delay components decrease with the supply voltage, whereas the delay components $t_{\mathrm{CLK-Q}}$ and $t_{\mathrm{D-Q}}$ increase with increasing temperature. It is also observed that the effect of supply

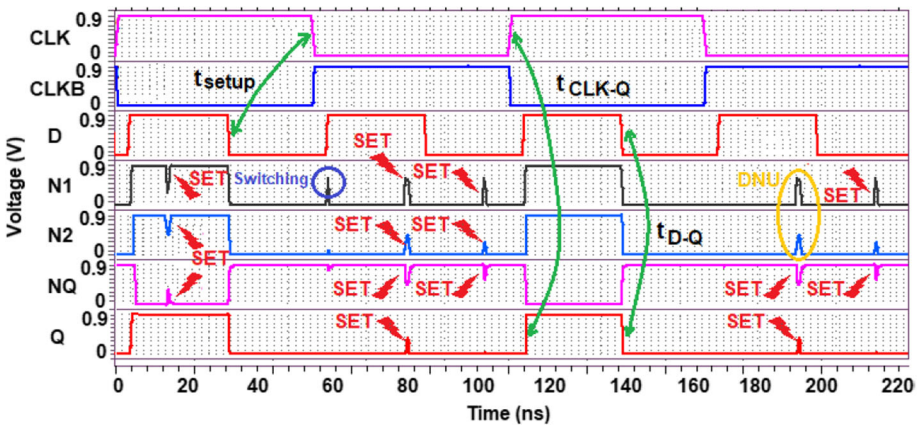


Fig. 14 Transient response and timing diagram of the NST-VB based latch

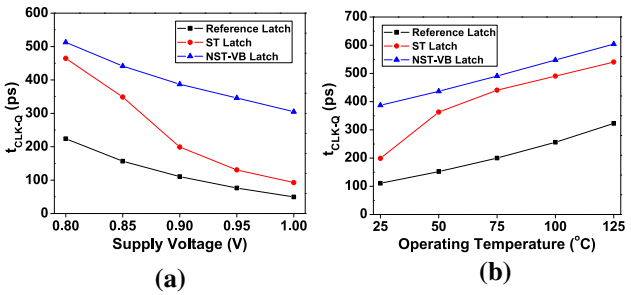


Fig. 15 Propagation delay of the different latches from clock signal *CLK* to the output *Q* with **a** different supply voltages at room temperature and **b** different operating temperatures at $V_{DD} = 0.9$ V

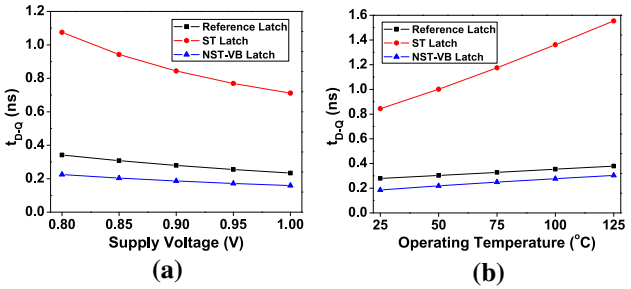


Fig. 16 Popagation delay of the different latches from data signal *D* to the output *Q* with **a** different supply voltages at room temperature and **b** different operating temperatures at $V_{DD} = 0.9$ V

voltage variation and temperature variation on t_{CLK-Q} is higher compared to the t_{D-Q}. Further, we also observe that the t_{CLK-Q} for the proposed NST-VB latch is higher as compared to the unhardened and ST based latch. This is because the proposed NST-VB circuit has unbalanced PUN and PDN. The higher t_{CLK-Q} for the proposed NST-VB latch effectively increases the overall delay of the latch but is comparable with the ST based latch.

5.4 Circuit area and power delay product

The layout of the reference latch, ST based latch, and proposed NST-VB latch is shown in Fig. 17. The NST-VB and ST inverters have an equal number of transistors; still, the ST inverter required larger transistor sizing to achieve the same characteristics as the NST-VB inverter. However, the NST-VB latch requires slightly more area as compared to the ST latch because NST-VB based inverter needs two supply voltages to improve the noise margin. The area of ST latch and NST-VB latch is 1.19× and 1.43× more as compared to the unhardened reference latch. Power delay product (PDP) and circuit area of different latches are given in Table 2. Further, we evaluate the PDP for different latches, considering the dynamic power and the delay. From the results we observe that the PDP for the proposed NST-VB latch is minimum compared to the unhardened and ST based latches. The lower dynamic power for the NST-VB latch is the deciding factor for reducing the PDP.

5.5 Charge to PDAP ratio

The improved soft error robustness can be achieved by increasing critical charge with critical node capacitances. However, this may require an increase of transistor sizing and thus increased area overhead. Reasonably increasing the supply voltage increases the critical charge, but the power dissipation also increases. To consider all the above important factors, a new performance metric considering critical charge, power dissipation, delay, and area can be introduced and referred to as a charge to PDAP ratio (QPAR) [16]. The QPAR can be given as

$$\text{QPAR} = \frac{\text{Critical Charge}}{\text{Power} \times \text{Delay} \times \text{Area}}. \tag{9}$$

A more significant value of QPAR indicates the higher soft error tolerance, high performance, and low power consumption of the latch. From Table 2, the QPAR of the proposed NST-VB based latch is higher than the reference latch and ST based latch, demonstrating the advantages of the proposed NST-VB based latch circuit.

5.6 Impact of process corners on critical charge

The process corners represent the extreme parameter variations in which the proper circuit functionality can be guaranteed. A circuit running on devices fabricated at these process corners may run faster or slower than specified. The TT process corner is normally considered for the

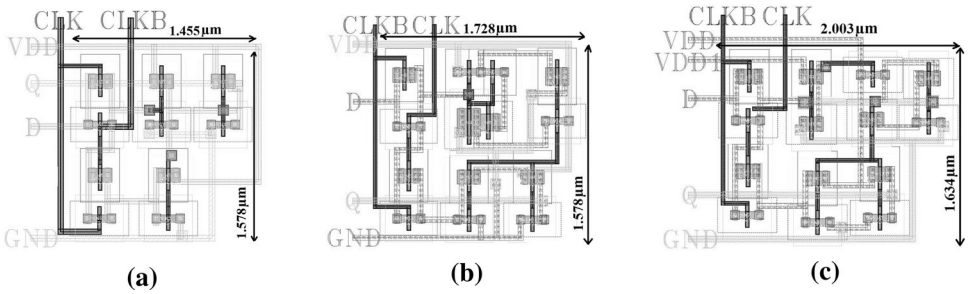


Fig. 17 Layout of the different latch circuits **a** Reference latch **b** ST-based latch **c** NST-VB based latch

analysis. However, the SS and FF process corners are considered if we have to calculate the worst-case propagation delay and power dissipation, respectively. TT, FF and SS process corners affect evenly on both PMOS and NMOS transistors, but FS and SF are the skewed corners which affect the PMOS and NMOS oddly and becomes the major concern for the correct functionality of the circuits. The effect of different process corners on the critical charge for all the considered latches has been calculated, as shown in Fig. 18. The result shows that the critical charge at the sensitive node of NST-VB latch is higher for all the process corners as compared to the unhardened latch and ST based latch. The results show that the critical charge at the SF process corner is highest compared to the other process corners. At the SF process corner, the faster PMOS and slower NMOS transistor increase current, and the node charge does not discharge, which leads to s higher critical charge. Similarly, for the FS process corner, the condition is opposite and has a lower critical charge at the sensor node.

5.7 Process variation analysis

To investigate process variations on the considered latches, we perform 5000 Monte Carlo simulations by varying the threshold voltage of the transistors. The threshold voltage of the transistors is generated randomly using a normal distribution with $\pm 10\%$ maximum deviations from its original value [16].

We perform Monte Carlo simulations for the unhardened reference latch and observe that it has a 100% flipping probability if the SET is injected at the most sensitive node. As the reference latch has 100% flipping with all the MC samples, we have not considered it for the critical voltage deviation analysis. Figure 19 shows the Monte Carlo simulations for the logic flipping probability at the node

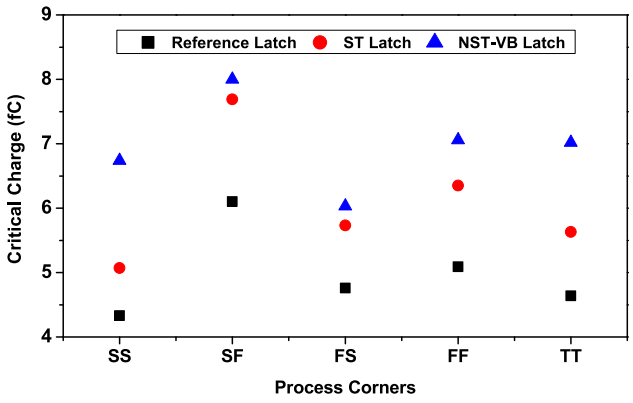


Fig. 18 Critical charge at the sensitive node N1 of different latches with various process corner variations. The operation corners are SS = slow-slow, SF = slow-fast, FS = fast-slow, FF = fast-fast, and TT = typical-typical for the NMOS-PMOS transistors

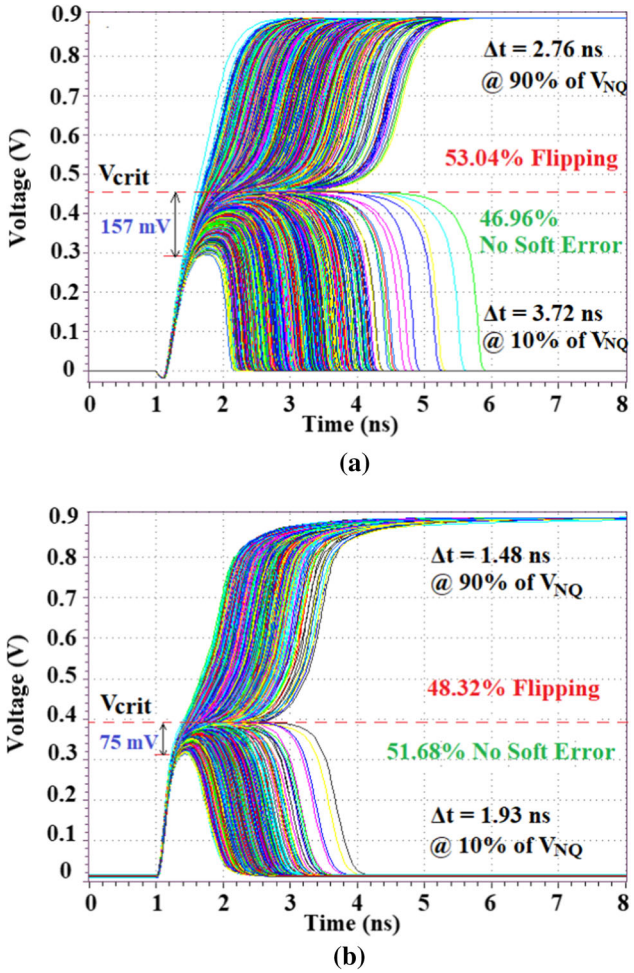


Fig. 19 5000 Monte Carlo simulations for the node voltage V_{NQ} for **a** ST based latch **b** NST-VB based latch

voltage V_{NQ} is SET is injected at the most sensitive node N1 of the ST based and NST-VB based latches. We have considered respective I_{inj} (at which the Q_{crit} is calculated) for both the latches to analyze the logic flipping probability at the critical value of I_{inj} and observe that the NST-VB latch has less effect of process variations as compared to the ST latch. Results demonstrate that the flipping probability for the unhardened latch, ST based latch, and NST-VB based latch are 100%, 53.04%, and 48.32%, respectively. This clearly indicates that, if a SET is injected at the sensitive node of latches and analyze the process variation effects on the logic flipping, the proposed NST-VB latch has better control for soft errors.

Further, we also analyze the signal scattering during non-flipping and flipping regions at the 10% and 90% values of node voltage V_{NQ}, respectively, as given in Table 3. As the unhardened latch has no non-flipping region, we have considered only the flipping region at the 90% value of node voltage V_{NQ}. The result indicates that the scattering of node voltage is less for the proposed NST-

Table 3 Scattering time range of node voltage V_{NQ} with 5000 MC during logic flipped/unflipped regions for different latches

Latches	Signal scattering (Δt)	
	@ 10% of V_{NQ}	@ 90% of V_{NQ}
Reference	NA	2.21 ns
ST	3.72 ns	2.76 ns
NST-VB	1.93 ns	1.48 ns

Table 4 Process variation parameters for critical voltages during no flipping region for different latches

Latches	Process variation parameters		
	Mean (μ)	SD (σ)	Variability (σ/μ)
Reference	NA	NA	NA
ST	397.7 mV	30.95 mV	0.0778
NST-VB	355.3 mV	14.09 mV	0.0396

VB latch as compare to the unhardened and ST based latches. The signal scattering during the flipping region for NST-VB is 1.49× and 1.86× less compared to the unhardened and ST based latches, respectively. Also, the signal scattering during the non-flipping region is 1.93× less for NST-VB latch than the to ST based batch.

Additionally, we also perform 5000 Monte Carlo simulations for the critical voltages (V_{crit}) of ST and NST-VB based latches during the non-flipping region, as shown in Fig. 20. We could not evaluate process variability for the reference latch because it does not exist in the non-flipping region and has a 100% flipping probability. Results demonstrate that the effect of process variation on the critical charge of NST-VB latch is less as compared to the ST based latch. The deviation range for NST-VB latch is 75mV compared to 157mV for the ST based latch.

We calculate the standard deviation considering $\pm 3\sigma$ deviation from the mean (μ) value. The calculation formula of standard deviation (σ) for the critical voltage of the latches are given as

$$\sigma = \sqrt{\frac{\sum (X_i - \mu)^2}{N}} \tag{10}$$

where σ is the standard deviation, N, X_i, and μ denotes the number of sample values that is 5000, the sample value, and mean value, respectively. The mean and standard deviation of critical voltage from the mean value for ST based latch is higher as compared to NST-VB based latch. The ST based latch has 2.2× more deviation as compared to NST-VB based latch.

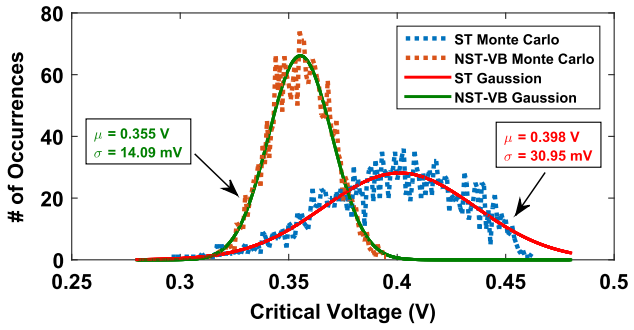


Fig. 20 5000 Monte Carlo simulations for the critical voltage for the ST and NST-VB circuit considering no flipping of logic state during SET injection at the sensitive nodes

This process variability for the critical voltage gives information about the uncertainty of logic flipping. Higher variability has more uncertainty and results in increased flipping probability. The process variation parameters for various latches are given in Table 4. The result shows that the variability of proposed NST-VB latch is less as compared to the ST based latch. Lower the process variability indicates less effect of process variations in the circuit. The above discussions indicate that the effect of process variations is less for the proposed NST-VB latch as compare to the unhardened reference latch and ST based latch.

6 Conclusion

In this paper, we propose a new NST-VB based radiation-hardened latch. Initially, we analyze the radiation hardening of different inverter circuits, an important component to design a latch. We clearly observe that the NST-VB inverter has better performance in terms of radiation hardening as compared to CMOS and ST inverters. Later, we utilize the benefit of NST-VB inverter to implement the radiation-hardened latch. We analyze the critical charge, power dissipation, and delay of all the latches under the PVT variations, and NST-VB latch performs significantly better as compared to other latches. For the process variations analysis of different latches, we performed 5000 Monte Carlo simulations and observed that the failure probability of NST-VB latch is less as compared to the reference and ST latches. This indicates the ability for the performance stability of NST-VB latch under a harsh environment. For validation of the proposed latch considering a broad set of performance parameters, the QPAR is analyzed. We observe that the proposed latch reveals improved performance compared to the unhardened latch. Due to its better radiation hardening capability, the proposed latch is suitable for the applications where external

radiation is significant, for instance, in the electronic circuits for aircraft and space environment.

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Data availability statement All data is provided in the results section of this paper.

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