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Impact of single-defects on the variability of CMOS inverter circuits

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ABSTRACT

Variations in the operational behavior of seemingly identical transistors pose a remarkable challenge for application engineers as integrated circuits have to be designed to be resilient against process and aging-related error sources. In small-area transistors, electrically active defects give rise to considerable device-to-device variations for instance of the threshold voltage. With the ongoing reduction of device dimensions, the impact of a single-defect becomes more and more relevant for the device behavior. While in circuit simulations, typically changes of mean values are considered, we thoroughly investigate the impact of variations of defect distributions on the signal propagation delay of an inverter circuit from the perspective of single oxide and interface defects. For this, the charge trapping kinetics of each defect is described using our stochastic charge trapping model. The impact of these single defects on the device behavior is extracted from detailed experimental studies. We demonstrate that the variation of the defect distributions between devices can lead to a signal propagation delay of several picoseconds for an inverter circuit. This can become a critical issue for circuits employing nanoscale transistors intended to operate at several hundreds of megahertz.

1. Introduction

The well-defined interplay of many different electronic devices determines the proper functionality and robustness of complex integrated electronic circuits. To ensure stable operation of such circuits, simulations employing compact models describing the behavior of the components are typically performed during the design process using SPICE tools. The compact models often rely on mean values for the characteristic electrical parameters, e.g. the threshold voltage, of a transistor [1–3]. However, in several simulation approaches also device-to-device variations are considered [4]. Instead of developing a full SPICE model which accounts for parameter variation, the combination of TCAD device simulations in conjunction with SPICE simulations is often used. For instance from TCAD simulations, the variability of the parameters of a transistor can be extracted and afterwards be considered to evaluate the variation of the circuit behavior employing a SPICE simulator [5].

2. Reliability aware circuit simulation

Two aging mechanisms have to be considered when designing an integrated circuit, hot-carrier degradation and bias temperature instabilities (BTI). I addition, process variations give rise to unexpected failure of circuits and components.

To consider for instance BTI, power-law-like models are often used to describe the observed change of a transistor's threshold voltage during operation [8]. By entering the nanoscale regime, single charge transitions become visible in the experimental data taken from nMOS and pMOS devices [9–12]. Consequently, the behavior of scaled devices cannot be solely described by a simple power-law function. Note that the impact of a defect on the device threshold voltage scales inversely with the device area. Thus, device-to-device variations are considerably more significant in scaled technologies than for their large-area counterparts, which emphasizes the importance of an accurate stochastic description of an entire technology's behavior [13,14].

In the recent past, considerable attention had been put on

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investigating single defects in small-area devices, primarily by thoroughly studying random telegraph noise [15–17], but also by employing the time-dependent defect spectroscopy [18–21]. By doing so, many peculiarities, like fixed versus switching trap behavior [22] or volatility of defects [23] have been observed. To model the charge trapping kinetics of defects observed from various technologies the non-radiative multiphonon model has been proposed and successfully applied [18,24]. Next to the charge capture and charge emission time, the impact of a defect on the device threshold voltage is statistically distributed, e.g. due to random variations of the dopant and defect distributions [25]. The average step height caused by defects has been evaluated by creating the complementary cumulative distribution function (CDF) of step-heights caused by charge emission events of single defects [13,26]. Initially, it has been observed that the complementary CDF follows a uni-modal exponential behavior for devices with a single insulating layer and a bi-modal exponential behavior for high-k gate stacks [13,20]. However, recent more detailed investigations have revealed that also for various SiON technologies, the complementary CDF exhibits two branches [27,28]. It has been further shown that the real impact of a defect on the threshold voltage is considerably larger than predicted by the charge sheet approximation (CSA) [27,28], which is, however, the commonly used estimator for the step-height in simulation tools [7].

To precisely evaluate the influence of the device-to-device variation caused by single defects, we use our defect simulator Comphy [7] to calculate the variations in the threshold voltage and employ the open-source SPICE simulator ngspice to study the consequences for electronic circuits. It has to be noted that established transistor models which are directly available in circuit simulators typically neglect the recovery of the device ΔV_{th} at low gate-source bias [29,30]. As a consequence, the values predicted by these tools are expected to seriously overestimate the ΔV_{th} behavior and thus could introduce overhead in the circuitry, which could be avoided otherwise. One way to circumvent the lack in the accuracy of the employed compact models is to consider the recovery behavior in a post-processing step [31]. In our simulations, we follow a similar approach to calculate the impact of the analog signals on the device threshold voltage. Our results show that when recovery is considered, a significantly lower degradation compared to the recovery-free simulations is obtained.

3. Calibration of the simulation tools

In our study, we consider the inverter circuit shown in Fig. 1. It can be seen that one of the two transistors is always in stress-mode (high applied gate bias), either positive BTI (PBTI) for the nMOS or negative BTI (NBTI) for the pMOS transistor. At the same time, the other transistor is in recovery-mode (zero gate-source bias). The subsequent application of stress and recovery phases to the transistors lead to altering of the threshold voltage of each of the devices which is determined by the corresponding charge trapping kinetics of a number of defects, see Fig. 2, and the corresponding macroscopic ΔV_{th} degradation as shown in Fig. 3. Each of the defects can become charged or discharge during operation, depending on the applied bias patterns.

To calibrate Comphy and to determine the defect parameters, a large set of extended measure-stress-measure (eMSM) experiments at various electrical stress/recovery fields and times and different temperatures are required for pMOS and nMOS devices [32]. From the measurements made on large-area devices, as shown in Fig. 3, trap-bands can be extracted, which enable accurate calculation of the device threshold voltage drift ΔV_{th} under arbitrary operating conditions, i.e. applied bias signals and temperature. Note that the extraction of the trap parameters can be dealt with in a semi-automatic fashion using our novel effective single defect decomposition (ESiD) extraction based on a non-negative least square estimator [6].

Next, the MSM scheme is applied to small-area devices of the same SiON technology. In nanoscale devices the experimental ΔV_{th} data exhibits discrete steps, representing charge transition events of single defects, as visible in Fig. 4. The results are consistent with the data for the large-area counterparts from Fig. 3, where the pMOS devices show a larger drift of the ΔV_{th} compared to the nMOS data. From this one might conclude that NBTI is more important than PBTI in circuit simulations. However, as we will see later, for the inverter circuit, PBTI can compensate for the signal propagation delay caused by NBTI, and thus leads to an improvement of the circuit degradation.

In small-area devices, the contributions of each of the defects to the total device degradation can be studied individually and can be statistically analyzed by calculating the complementary CDF, see Fig. 5.

For our devices, we observe a bi-modal and uni-modal exponential step-height distributions for nMOS and pMOS devices, respectively. Note that the maximum ΔV_{th} caused by a single defect according to the CSA is around 0.2 mV, which is more than a factor of two smaller than what is extracted from the experimental data for the pMOS and nMOS transistors. To replicate the real impact of the single-defects on ΔV_{th}, we have implemented a suitable model to Comphy to randomly draw defect distributions according to the measured complementary CDFs. This enables us to calculate the recovery behavior of the nanoscale devices, see Fig. 6. We observe an excellent agreement between the simulation results and the measurement data, which indicates the high accuracy of

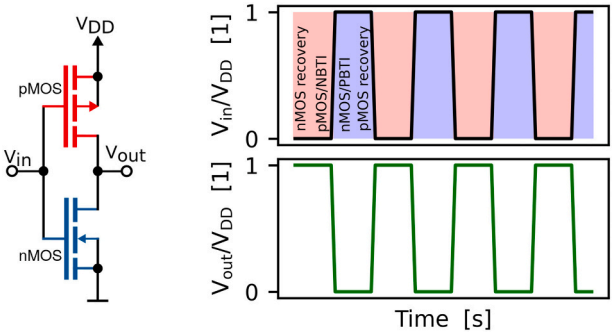

Fig. 1. (left) The circuit diagram of a CMOS inverter circuit is shown together with (right) the corresponding input and output bias signals. As can be seen, one of the transistors is always under stress, while at the other, no gate-source bias is applied. As demonstrated in this work, the device stress can alter the characteristics of the device, which leads to additional propagation delays of integrated circuits.

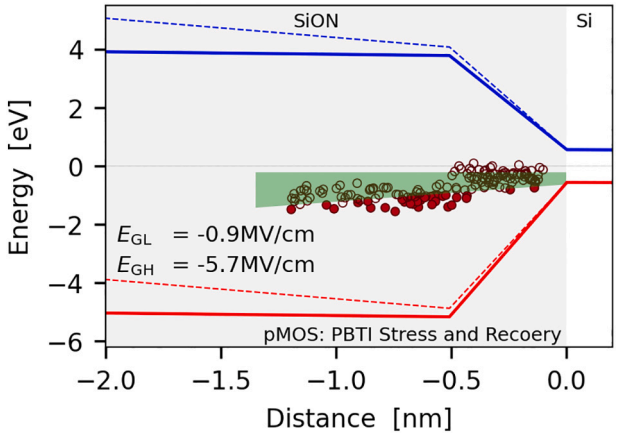

Fig. 2. The trap bands which have been extracted in [6] for the investigated SiON technology are schematically shown in the band diagram of a representative pMOS transistor. Instead of considering an abrupt transition region between the channel and the insulator, a gradual transition of the bands is considered in our defect simulator [7]. By applying our toolset to measure-stress measure sequences, defect distributions, i.e. trap levels, positions, and relaxation energies, can be extracted from the experimental data.

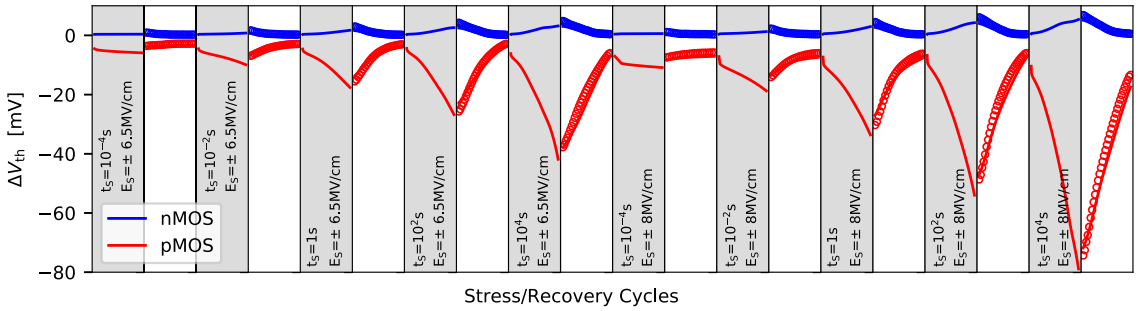

Fig. 3. A typical measure-stress-measure (MSM) sequence recorded on an nMOS transistor (blue) and a pMOS transistor (red) with $W \times L$=10 × 10 after PBTI, and NBTI stress has been applied, respectively, is shown. The measurement series (symbols) has been recorded at T=100 ° C and is measured without any interrupt. The stress conditions are indicated in the Figure and the recovery bias has been selected using a constant current criteria, i.e. V_G to achieve $I_{DS} = \pm$ 500 nA for the nMOS and pMOS devices. It can be observed that the pMOS device exhibits a considerably larger drift of the threshold voltage ΔV_{th}, even though the same electric oxide field has been applied to the devices during stress. Our simulations (lines) nicely explains the experimental data. Note that single MSM sequences are not sufficient for the accurate extraction of the defect band properties, but rather a series of measurements has to be performed at various temperatures and bias conditions. Further experimental details and a novel methodology to efficiently extract common trap properties for the entire technology considered here are given in [6]. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

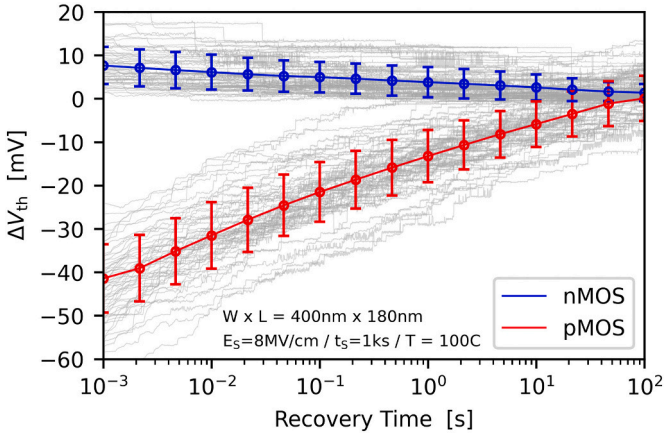

Fig. 4. Contrary to large-area devices, in nanoscale transistors, discrete steps can be observed for nMOS (blue) and pMOS (red) transistors when stress-recovery measurements are performed. Each of the steps corresponds to a charge transition event of a single-defect, giving rise to a shift of the device threshold voltage. Even more significant is the variation in the transient behavior of ΔV_{th}. This variation stems from the different charge trapping kinetics of the individual defects in the device. Additional variation is introduced due to different step-heights of electrically active defects and becomes even more severe in more scaled devices, i.e. scales inversely with active gate area [13]. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

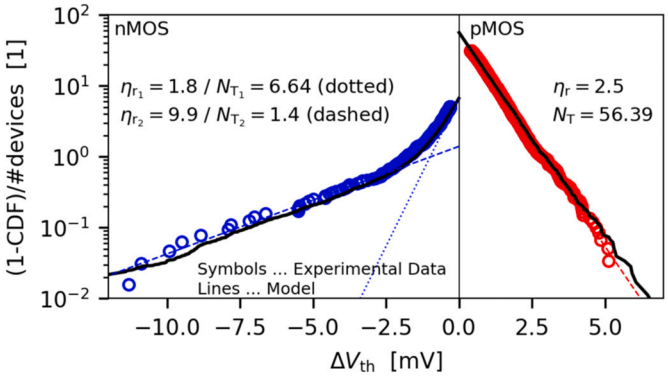

Fig. 5. The complementary CDF has been extracted from the recovery traces from Fig. 4 for both nMOS and pMOS SiON transistors (symbols). To investigate the device-to-device variations induced by the defects, we make use of these distributions for the selection of the step-heights of the defects instead of applying the commonly used charge sheet approximation CSA. The values for η_r are referred to the CSA by $\eta_r = \eta/\eta_{CSA}$ with $\eta_{CSA} = \varepsilon_0\varepsilon_r A/d$. As can be seen, with the CSA the impact of the defects on the ΔV_{th} is considerably underestimated [28].

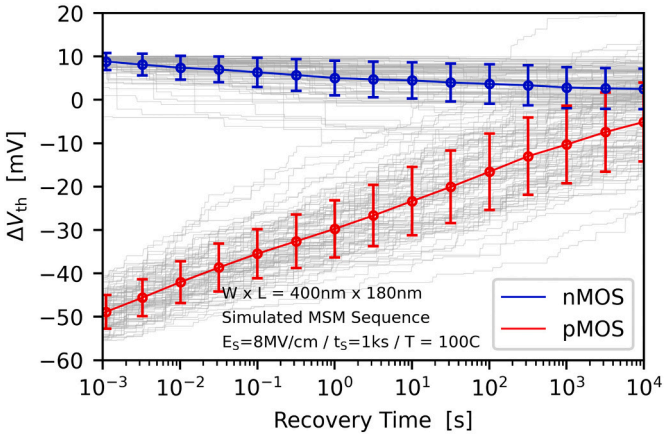

Fig. 6. The recovery traces computed with our calibrated defect simulator nicely reproduces the variations between the large data-set of devices shown in Fig. 4.

the reliability simulations and toolset.

Next to the contribution of a single trap to the overall ΔV_{th} the trap depth and trap level are additional crucial parameters of our model. Especially a good agreement of these parameters with values from theoretical studies is a strong indicator for the physical soundness of the extracted trap distributions. As for CMOS inverters both nMOS and pMOS transistors are important, our model has to be able to replicate the behavior of both electron traps that determine the ΔV_{th} characteristics of nMOS devices and hole traps that are dominant in pMOS transistors. While the electron traps are modeled to reside close to the conduction band edge of an nMOS transistor, the hole traps are considered to be located near the valence band edge of the pMOS counterpart [6]. It has to be noted that the trap levels of the defects used in our study are in good agreement with recent DFT calculations. There it has been discussed that the oxygen vacancy is a good candidate for an electron trapping site [33,34], while hydrogen-related defects, such as the hydroxyl-E' center, are likely candidates for hole traps [23,24].

4. Analog AC signal simulations

With the calibrated reliability tools at hand, we simulate the aging of the transistors when AC patterns are applied to the inverter circuit, see Fig. 7. As can be seen, the device degradation is on the order of several μV, when a total signal time of 0.1 is simulated. Note that when the recovery of the devices is neglected, a considerably larger is obtained, which would lead to an overestimation of the degradation of the circuit. For the simulations, 100 points per period of the AC signal have been computed to ensure high accuracy of the obtained ΔV_{th}. Also the transitions between low and high gate bias are simulated with $t_r = t_f$=10 to consider the dynamic behavior of the defects. At each simulation time step, the charge transition rates have to be evaluated for several hundreds of defects, and thus simulating long AC signals becomes computational inefficient.

An efficient approach has been developed in [35–37] where the ΔV_{th} obtained after N periods of the AC signal can be calculated from the change of the defect occupancy during the first period of the AC signal. With this method, the device threshold voltage degradation can be calculated even for very long AC patterns, see Fig. 8. Again, a very small ΔV_{th} can be observed for short stress times, but a considerable ΔV_{th} becomes visible for nMOS and pMOS devices when the operational time exceeds 1 ks. It can also be seen that the behavior is significantly affected by the statistical distribution of trap parameters. For both nMOS and pMOS devices, a considerable variation of the transient ΔV_{th}can be observed, which is further responsible for a significant variability in the signal propagation delay of the inverter circuit.

5. Results

A characteristic parameter of an inverter circuit is the signal propagation delay t_D. It is defined as the time difference when the output and input signal is equal to $V_{DD}/2$, see Fig. 9. To calculate the t_D, we consider the threshold voltage of the transistors distributed according to the variation observed in Fig. 8 and perform a transient simulation using NGSPICE. In the final analysis step, we focus on the impact of the considerable variation of the device threshold voltage drift caused by different distributions for the step heights of the defects in Fig. 5. The resulting values for signal propagation delay of the CMOS inverter t_D are summarized in Fig. 10, and are shown together with the individual contributions of the nMOS and pMOS devices to it. Considering the variability (black symbols), one can see that at short AC signal times, only a small variation can be observed for t_D, as most of the defects in the transistor are still in their initial charge state. However, at long operation times, a large ensemble of defects has become charged, and as a result, a considerable variation in t_D can be observed. The second aspect, i.e., the reliability of the inverter circuit, can be evaluated by considering the drift of t_D over AC signal time. This is calculated as the average of the t_D values extracted for nMOS and pMOS devices at the different time steps. It can be seen that as the ΔV_{th} for pMOS devices dominates over nMOS devices, the evolution of is mainly determined by the pMOS transistor. This follows from the fact that charge trapping in nMOS and pMOS devices leads to a different sign of the obtained t_D, which causes that BTI in both kinds of devices counteracts each other in terms of the t_D of the

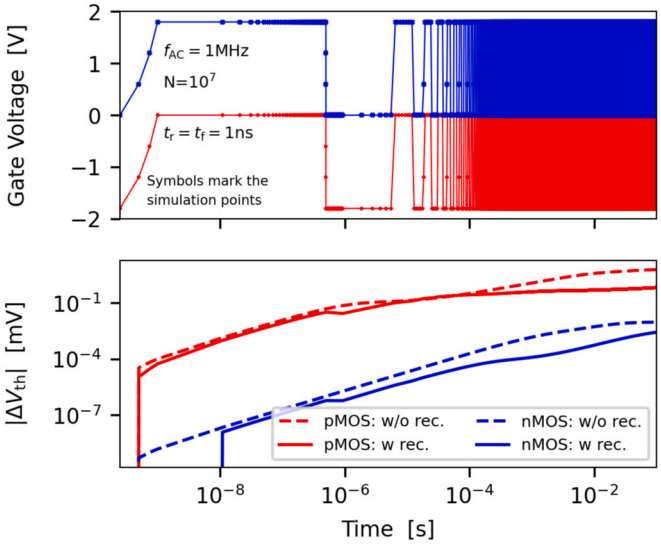

Fig. 7. Simulated impact of an analog AC signal (top) on the transient behavior of (bottom) which is applied to the nMOS (blue) and pMOS (red) transistor when operated in an inverter circuit. For the nMOS, a drift of ΔV_{th} by several μV can be observed, which is lower than for the pMOS transistors. In both cases, the degradation is calculated to be dramatically larger when recovery is neglected (dashed line). This emphasizes once more the importance of an accurate charge trapping model for circuit simulations. Note that direct calculation of the ΔV_{th} response is computationally very demanding and thus not suitable for the evaluation of long stress series considering AC signals. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

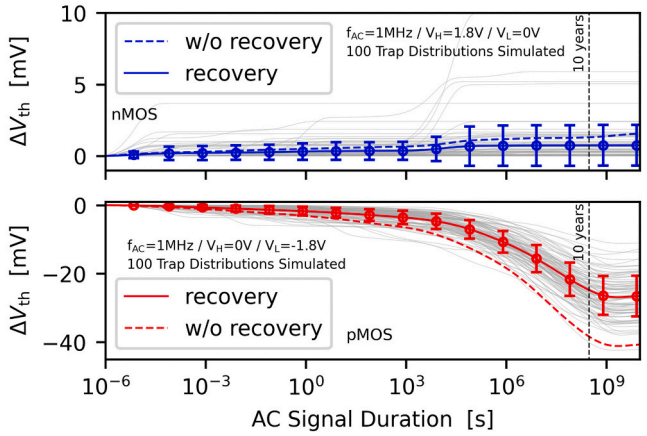

Fig. 8. Device-to-device variation and average device degradation of an AC pattern applied to nMOS (top) and pMOS (bottom) transistors. For the variation simulations, 100 trap distributions have been drawn according to the measured complementary CDF. A remarkable variation in the device behavior can be observed, which unavoidably leads to a variation of the signal propagation delay. Also shown here is the evolution of ΔV_{th} when device recovery is omitted, which leads to a twice as high ΔV_{th}, especially at high device operational times.

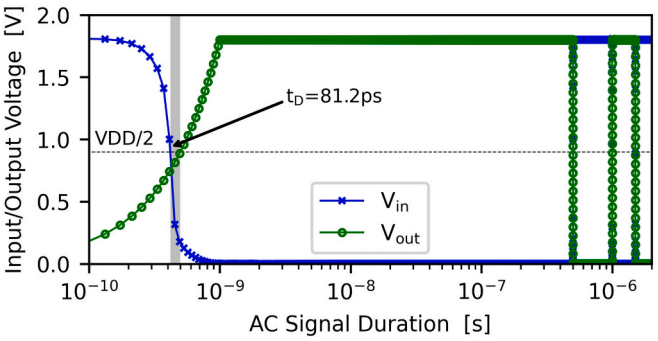

Fig. 9. The propagation delay is the time difference between the input and output signal when 50% of V_{DD} is reached. Note that in this schematic the time-zero t_D is positive, but in the case of matched transistors with an equal threshold voltage t_D would be zero. As we are entirely focusing on the impact of the defect distribution on the impact of t_D the V_{th} of the selected devices will not affect our results.

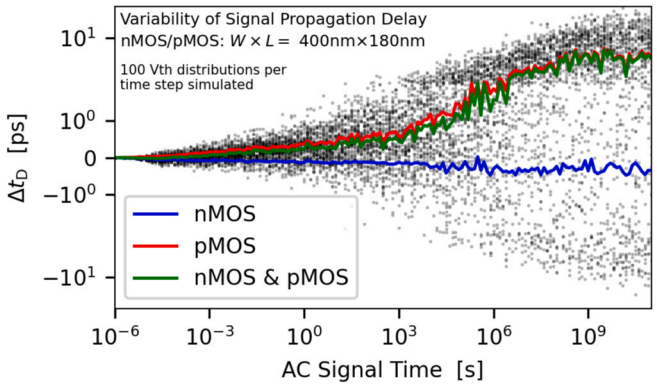

Fig. 10. The signal propagation delay of the CMOS inverter t_D is shown over the AC signal time. For each transistor, i.e. different trap distributions, leading to the recovery traces in 6 the resulting t_D has been calculated for AC operating conditions (black symbols). It can be seen that variations in the single-defect distributions cause a considerable distribution in t_D. The solid lines show the average t_D extracted from 100 distributions per time step. Quite interestingly, while charge trapping at nMOS devices leads to a positive t_D defects in pMOS transistors give rise to a negative t_D and thus counteract the degradation introduced by the other device kind. As can also be seen, the majority of t_D is caused by charge trapping in pMOS transistors. This is because the electron traps exhibit shorter trapping kinetics and thus can follow the dynamics of the AC signal. The hole traps that reside in the pMOS exhibit, on average larger emission times and thus lead to a build-up of t_D. It has further to be noted that, even at short total operational times of a circuit in the order of several tens of ks the variation of the defect distributions among small-area devices of the same technology can introduce an additional signal propagation delay t_D of several ps. While small variations may be negligible for AC signals in the 1 MHz range, considering the influence of the single-defects on t_D can become particularly important for operating frequencies in the order of several hundreds of MHz or the GHz range.

inverter. Thus, the overall t_D of the inverter circuit is smaller than the t_D introduced by the degradation of the pMOS devices only. Both the absolute value of the propagation delay and its significant variation can be on the order of several ps, and thus can result in a serious concern for circuits operating at several hundreds of MHz.

In summary, the accurate description of the charge trapping kinetics and the replication of the real step height distribution are of utmost importance for simulations to correctly estimate reliability and variability issues in electronic circuits. We found the variation of signal propagation delay caused by different defect distributions of seemingly identical devices is on the range of up to 10 ps for the investigated technology. Note that for technologies employing devices with geometries of a few tens of nanometers, device-to-device variations are more severe and will thus lead to more significant delays of inverter circuits.

6. Conclusions

Our study examines the impact of single-defects on the signal propagation delay of inverter circuits when an AC signal is applied. For the inverter, we consider small-area MOS transistors of the same SiON technology. We demonstrate the importance of the recovery behavior of each of the transistors, as otherwise an overly pessimistic device degradation would be obtained. Another important feature is the distribution of the step-heights of the defects, i.e. their impact on the drift of the threshold voltage. Typically statistically distributed step heights are not considered in circuit simulations. Furthermore, the step heights are typically underestimated by a factor of more than two by the charge sheet approximation, which is mostly used in simulators. We employ a suitable model for the distributions of the step-heights of the defects and evaluate their impact on the signal propagation delay of an inverter circuit. Our results indicate with the drawn trap distribution, additional delays up to 10 ps are introduced at large operational times. This can be a severe concern for the interplay of circuit components at operating frequencies of several hundreds of MHz.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] J.R. Brews, A charge-sheet model of the MOSFET, Solid State Electron. 21 (2) (1978) 345–355.
[2] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. Van Langevelde, G.D.J. Smit, A. J. Scholten, D.B.M. Klaassen, PSP: an advanced surface-potential-based MOSFET model for circuit simulation, IEEE Trans. Electron. Devices 53 (9) (2006) 1979–1993.
[3] Adelmo Ortiz-Conde, Juan Muci, Juin J. Liou, Ching-Sung Ho, Francisco J. Garc-Ãa-SÃ¡nchez, Alberto TerÃn. Barrios, Revisiting MOSFET threshold voltage extraction methods, Microelectron. Reliab. 53 (1) (2013) 90–104.
[4] H. Li, Z. Jiang, P. Huang, Y. Wu, H. Chen, B. Gao, X.Y. Liu, J.F. Kang, H.P. Wong, Variation-aware, reliability-emphasized design and optimization of RRAM using SPICE model, in: Design, Automation Test in Europe Conference Exhibition (DATE), 2015, pp. 1425–1430.
[5] S. Kurude, S. Mittal, U. Ganguly, Statistical variability analysis of SRAM cell for emerging transistor technologies, IEEE Trans. Electron. Devices 63 (9) (2016) 3514–3520.
[6] D. Waldhoer, C. Schleich, J. Michl, B. Stampfer, K. Tselios, E. Ioannidis, H. Enichlmair, M. Waltl, T. Grasser, Towards automated defect extraction from bias temperature instability measurements, IEEE Trans. Electron Devices (2021), https://doi.org/10.1109/TED.2021.3091966.
[7] Gerhard Rzepa, J. Franco, Barry J. O'Sullivan, A. Subirats, Marko Simicic, Geert Hellings, P. Weckx, Markus Jech, Theresia Knobloch, Michael Waltl, Philippe J. Roussel, D. Linten, Ben Kaczer, Tibor Grasser, Comphy – a compact-physics framework for unified modeling of BTI, Microelectron. Reliability 85 (1) (2018) 49–65.
[8] Ketul B. Sutaria, Jyothi B. Velamala, Athul Ramkumar, Yu. Cao, Compact Modeling of BTI for Circuit Reliability Analysis, Springer, New York, 2015.
[9] K.S. Ralls, W.J. Skocpol, L.D. Jackel, R.E. Howard, L.A. Fetter, R.W. Epworth, D. M. Tennant, Discrete resistance switching in submicrometer silicon inversion layers: individual Interface traps and low-frequency ($\frac{1}{f}$) noise, Phys. Rev. Lett. 52 (1984) 228–231.
[10] M. Waltl, W. Goes, K. Rott, H. Reisinger, T. Grasser, A single-trap study of PBTI in SiON nMOS transistors: similarities and differences to the NBTI/pMOS case, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2014, pp. XT18.1–XT18.5.
[11] R. Wang, S. Guo, Z. Zhang, J. Zou, D. Mao, R. Huang, Complex random telegraph noise (RTN): what do we understand?, in: Proc. Intl. Symp. on Physical and Failure Analysis of Integrated Circuits, 2018, pp. 1–7.
[12] B. Stampfer, F. Zhang, Yu.Yu. Illarionov, T. Knobloch, P. Wu, M. Waltl, A. Grill, J. Appenzeller, T. Grasser, Characterization of single defects in ultra-scaled MoS2 field-effect transistors, ACS Nano 12 (6) (2018) 5368–5375.
[13] B. Kaczer, P.J. Roussel, T. Grasser, G. Groeseneken, Statistics of multiple trapped charges in the gate oxide of deeply scaled MOSFET devices – application to NBTI, IEEE Electron Device Lett. 31 (5) (2010) 411–413.
[14] B. Kaczer, T. Grasser, P.J. Roussel, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simoen, G. Groeseneken, H. Reisinger, Origin of NBTI variability in deeply scaled pFETs, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2010, pp. 26–32.
[15] J.P. Campbell, J. Qin, K.P. Cheung, L.C. Yu, J.S. Suehle, A. Oates, K. Sheng, Random telegraph noise in highly scaled nMOSFETs, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2009, pp. 382–388.
[16] T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, Y. Hayashi, New analysis methods for comprehensive understanding of Random Telegraph Noise, in: Proc. Intl. Electron Devices Meeting (IEDM), 2009, pp. 1–4.
[17] D. Veksler, G. Bersuker, L. Vandelli, A. Padovani, L. Larcher, A. Muraviev, B. Chakrabarti, E. Vogel, D.C. Gilmer, P.D. Kirsch, Random telegraph noise (RTN) in scaled RRAM devices, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2013, pp. MY.10.1–MY.10.4.

[18] T. Grasser, H. Reisinger, P.-J. Wagner, B. Kaczer, The time dependent defect spectroscopy for the characterization of border traps in metal-oxide-semiconductor transistors, Phys. Rev. B 82 (24) (2010), 245318.
[19] H. Reisinger, T. Grasser, W. Gustin, C. Schluender, The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2010, pp. 7–15.
[20] M. Waltl, A. Grill, G. Rzepa, W. Goes, J. Franco, B. Kaczer, J. Mitard, T. Grasser, Superior NBTI in high-k SiGe transistors - part I: experimental, IEEE Trans. Electron Devices 64 (2017) 2092–2098.
[21] G. Rzepa, M. Waltl, W. Goes, B. Kaczer, T. Grasser, Microscopic oxide defects causing BTI, RTN, and SILC on high-k FinFETs, in: Proc. Simulation of Semiconductor Processes and Devices, 2015, pp. 144–147.
[22] T. Grasser, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, B. Kaczer, The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2010, pp. 16–25.
[23] T. Grasser, K. Rott, H. Reisinger, M. Waltl, P.-J. Wagner, F. Schanovsky, W. Goes, G. Pobegen, B. Kaczer, Hydrogen-related volatile defects as the possible cause for the recoverable component of NBTI, in: Proc. Intl. Electron Devices Meeting (IEDM), 2013.
[24] T. Grasser, W. Goes, Y. Wimmer, F. Schanovsky, G. Rzepa, M. Waltl, K. Rott, H. Reisinger, V.V. Afanas'ev, A. Stesmans, A.-M. El-Sayed, A.L. Shluger, On the microscopic structure of hole traps in pMOSFETs, in: Proc. Intl. Electron Devices Meeting (IEDM), 2014.
[25] A. Asenov, R. Balasubramaniam, A.R. Brown, J.H. Davies, RTS amplitudes in decananometer MOSFETs: 3-D simulation study, IEEE Trans. Electron Devices 50 (3) (2003) 839–845.
[26] M. Waltl, Ultra-low noise defect probing instrument for defect spectroscopy of MOS transistors, IEEE Trans. Dev. Mat. Rel. 20 (2) (2020) 242–250, invited.
[27] M. Waltl, B. Stampfer, G. Rzepa, B. Kaczer, T. Grasser, Separation of electron and hole trapping components of PBTI in SiON nMOS transistors, Microelectron. Reliab. 114 (2020), 113746.
[28] Konstantinos Tselios, Bernhard Stampfer, Jakob Michl, Eleftherios Ioannidis, H. Enichlmair, M. Waltl, Distribution of step heights of electron and hole traps in SiON nMOS transistors, in: Proc. Intl. Integrated Reliability Workshop (IIRW), 2020, pp. 1–6.
[29] J. Fang, S.S. Sapatnekar, The impact of BTI variations on timing in digital logic circuits, IEEE Trans. Device Mater. Reliab. 13 (1) (2013) 277–286.
[30] H. Amrouch, S. Mishra, V. van Santen, S. Mahapatra, J. Henkel, Impact of BTI on dynamic and static power: from the physical to circuit level, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2017, pp. CR-3.1–CR-3.6.
[31] J. Diaz-Fortuny, J. Martin-Martinez, R. Rodriguez, M. Nafria, R. Castro-Lopez, E. Roca, F.V. Fernandez, TARS: A toolbox for statistical reliability modeling of CMOS devices, in: International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2017, pp. 1–4.
[32] B. Kaczer, T. Grasser, J. Roussel, J. Martin-Martinez, R. O'Connor, B.J. O'Sullivan, G. Groeseneken, Ubiquitous relaxation in BTI stressing - new evaluation and insights, in: Proc. Intl. Rel. Phys. Symp. (IRPS), 2008, pp. 20–27.
[33] A.-M. El-Sayed, M.B. Watkins, V.V. Afanas'ev, A.L. Shluger, Nature of intrinsic and extrinsic electron trapping in SiO2, Phys. Rev. B 89 (2014).
[34] A.V. Kimmel, P.V. Sushko, A.L. Shluger, G. Bersuker, Positive and negative oxygen vacancies in amorphous silica, ECS Trans. 19 (2009) 2–17.
[35] K. Giering, A. Lange, B. Kaczer, R. Jancke, BTI variability of SRAM cells under periodically changing stress profiles, in: Proc. Intl. Integrated Reliability Workshop (IIRW), 2016, pp. 1–5.
[36] K. Giering, C. Sohrmann, G. Rzepa, L. Heiß, T. Grasser, R. Jancke, NBTI modeling in analog circuits and its application to long-term aging simulations, in: Proc. Intl. Integrated Reliability Workshop (IIRW), 2014, pp. 29–34.
[37] K.U. Giering, K. Puschkarsky, H. Reisinger, G. Rzepa, G. Rott, R. Vollertsen, T. Grasser, R. Jancke, NBTI degradation and recovery in analog circuits: accurate and efficient circuit-level modeling, IEEE Trans. Electron Devices 66 (4) (2019) 1662–1668.