Curvature-Based Feature Detection for Hierarchical Grid Refinement in Epitaxial Growth Simulations

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***Abstract*—We present a feature detection algorithm for selective grid refinement in hierarchical grids based on the curvature of the wafer topography in level-set process simulations. The proposed algorithm enables high-accuracy simulations while significantly reducing the run-time, as the grid is only refined in regions with high curvatures. We evaluate our algorithm by simulating selective epitaxial growth of silicon-germanium fins in narrow oxide trenches. The performance and accuracy of the simulation is assessed by comparing the results to experimental data showing good agreement.**

Keywords - Topography simulation, level-set method, curvature, hierarchical grid, non-planar epitaxial growth

Many non-planar semiconductor device geometries (e.g., FinFETs) are fabricated by employing strongly anisotropic processing techniques [1]. During selective epitaxial growth (SEG), wafer topographies emerge, which are characterized by crystal facets and thus a combination of high-curvature and essentially flat regions materialize [2]. Local high resolutions of the underlying grids are thus required to accurately resolve high-curvature features and material interfaces during a process simulation, while keeping the overall run-time as low as possible to maximize applicability.

The level-set method is a widely used tool for simulating fabrication processes of semiconductor devices [3]. The propagation of the wafer surface is described with the level-set equation

$$\frac{\partial \phi(x,t)}{\partial t} + V(x)|\nabla \phi(x,t)| = 0\,, \tag{1}$$

for the level-set function ϕ and the velocity field V, which models the growth or etch rates during a process step [3]. The level-set equation is typically solved on a regular grid with resolution Δx. The previously hinted need for local high grid resolutions can be realized by using hierarchical grids, offering a *base* grid covering the entire simulation domain. The base grid is complemented by *sub*-grids with higher resolutions, covering areas of interest (e.g., sharp ridges) [4] [5].

In this work, we present a curvature-based feature detection algorithm which enables optimal placement of these sub-grids. We evaluate the performance of the algorithm with a representative cutting-edge process simulation, i.e., selective epitaxy. The proposed algorithm has been implemented into Silvaco's *Victory Process* simulator [6] which is used to simulate selectively grown silicon-germanium (SiGe) fins and compare the results with recent experiments presented in [2].

The feature detection is based on the local curvature κ of the wafer surface, i.e., the level-set function, during the simulation process

$$\kappa = \frac{\phi_y^2\phi_{xx} - 2\phi_x\phi_y\phi_{xy} + \phi_x^2\phi_{yy}}{|\nabla\phi|^3}, \tag{2}$$

where ϕ_i denotes the partial derivative of ϕ with respect to the coordinate $i \in \{x, y\}$, which is calculated with finite differences. Surface points with a curvature of $|\kappa| = 0$ describe a flat part of the wafer surface. In contrast, points with a larger value of $|\kappa|$ indicate a feature on the wafer surface. Consequently, topography features are detected based on the curvature threshold parameter $C > 0$, which is problem specific. If the curvature of a surface point is larger than C the point is flagged as a feature. Furthermore, interfaces between stationary material regions are always detected as features, which enables a well-resolved level-set description of interfaces.

After the feature detection step the flagged surface points are grouped into rectangular *patches*. If patches overlap they are merged together until no more overlaps exist. New sub-grids with a, e.g., four-times smaller Δx (facilitating locally increased resolutions) are then created according to these patches. The level-set values for the sub-grids are calculated with a hierarchical re-distancing step [7].

The proposed feature detection algorithm is evaluated by simulating the SEG process presented by Jang *et al.* [2]. In an initial dry etching step, $[\bar{1}\,1\,0]$-aligned SiO_2 trenches are formed. A cyclic SEG step follows, leading to the formation of high-quality $\{3\,1\,1\}$ and $\{1\,1\,1\}$ crystal facets. The proposed algorithm is employed during the SEG step, where we utilize the numerical stability-enabling level-set method for selective epitaxy [8]. The growth of the SiGe crystal is modeled with a crystal

orientation dependent V which is constructed from experimentally characterized growth rates [2], see TABLE I.

TABLE II shows the utilized grid resolutions: The results shown in Fig. 1 are based on the *Multi-Grid* parameters, i.e., a base grid (Grid 1) complemented by one additional grid hierarchy level (Grid 2). The results are in good agreement with the data obtained from the experiment. Fig. 2 compares the results after the final time step (47 deposition cycles) of the simulation using the parameters shown in TABLE II. The *Coarse* result does not sufficiently match the result from the experiment (i.e., the *Multi-Grid* result, see Fig. 1), as evident from the mismatch of the peak positions of the SiGe crystal. As to be expected, the *Fine* result shows excellent agreement, however, with the added disadvantage of significantly increased simulation run-times due to the higher resolution of the base grid. This unnecessarily increases the resolution of many irrelevant, i.e., flat, areas. The *Multi-Grid* result is based on the empirically chosen threshold parameter $C = 0.9$. As discussed, *Multi-Grid* enables excellent agreement with the experimental data but with the advantage of a considerable reduced performance penalty as compared to the *Fine* case. An example of the flagged grid points and thus generated sub-grids after 24 SEG cycles is shown in Fig.3.

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TABLE I. Simulation parameters employed for the SEG in trench arrays [2]. The number of deposition cycles P_i refers to the number of SEG cycles needed to achieve the topography

Rates [nm/cycle]				Deposition cycles		
R_{100}	R_{110}	R_{311}	R_{111}	P_1	P_2	P_3
13	5	3.1	1.6	5	24	47

TABLE II. Grid parameters and run-times (Intel Xeon E5-2680v2) for the entire simulation.

Simulation	Grid 1 Res	Grid 2 Res	Run-Time
Coarse	0.002µm	-	28s
Fine	0.0005µm	-	19min 54s
Multi-Grid	0.002µm	0.0005µm	13min 38s

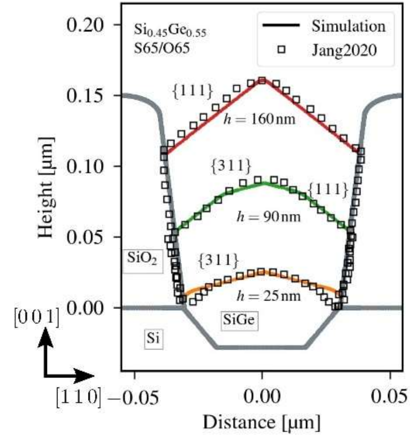

Figure 1. Simulated surface of the SiGe crystal (*Multi-Grid*) compared with the experimental results from [2] after 5 (orange), 24 (green), and 47 (red) SEG cycles.

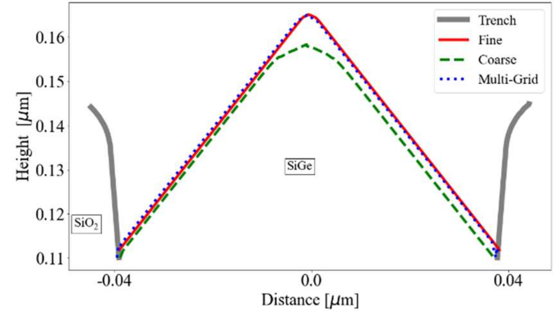

Figure 2. Surface for the final simulation result of the SEG process after 47 cycles using *Coarse*, *Fine*, and *Multi-Grid* resolutions.

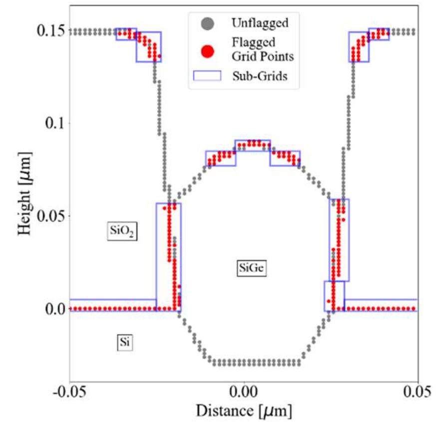

Figure 3. Grid points near the level-set function for Grid 1 (i.e., base grid) of the *Multi-Grid* simulation after 24 SEG cycles. The flagged grid points and placed sub-grids for this time step are shown.