# Physical Modeling of Charge Trapping in 4H-SiC DMOSFET Technologies

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***Abstract*—Silicon carbide (SiC) MOSFETs still exhibit higher drifts of the threshold voltage than comparable silicon devices due to charge trapping, especially regarding small time scales. Understanding this behavior and the consequences in application relevant conditions is therefore of high research interest. Since charge trapping at different defects close to the SiC/$SiO_2$ interface and in the bulk oxide is strong bias and temperature-dependent, the phenomenon is referred to as bias temperature instability (BTI). It has been shown that drifts caused by BTI vary both in transient shape and magnitude for commercially available devices. These differences arise from defect densities and properties in the respective technologies. A physical model together with defect parameters that explain the charge transfer reactions at the defects is essential to understand all peculiarities of the transient degradation. In this work, we use a novel method to semiautomatically extract defect parameters within a two-state nonradiative multiphonon model framework. Our work reveals properties of defects responsible for shifts of the threshold voltage for both short-term ac and long-term dc stress conditions which are accurately reproduced for three different DMOS technologies. Our calibrated simulation framework is further used to extrapolate device degradation at operation relevant ac bias conditions to typical device lifetimes.**

***Index Terms*—4H-SiC MOSFET, bias temperature instability (BTI), charge trapping, defects in SiC/$SiO_2$, power switch.**

## I. Introduction

THE continuous improvement of the SiC/$SiO_2$ interface has enabled the development of power MOSFETs which exploit the superior material properties of SiC as substrate material. Subsequent recent advances over a few generations have led to the wide availability of commercial SiC power devices. A keystone for this progress has been the optimization of the post oxidation annealing (POA) processing step after oxide deposition, which has reduced the amount of electrically active defects in the vicinity of the conducting channel [1], [2]. Despite this improvement, SiC/$SiO_2$ MOSFETs still often exhibit increased shifts of the threshold voltage $\Delta V_{\mathrm{th}}$ as compared to Si-based devices. Such $V_{\mathrm{th}}$ drifts are due to charge trapping in the SiC/$SiO_2$ interfacial region and can be observed both on short and long time-scales in SiC MOSFETs [3], [4]. Since the amount of trapped charge leading to these instabilities strongly depends on bias and temperature, it is commonly referred to as bias temperature instability (BTI). Contrary to mature Si/$SiO_2$ MOSFET technologies, the resulting $V_{\mathrm{th}}$ shifts vary widely for SiC devices manufactured by different vendors as well as between consecutive device generations [5], [6]. The extraction of the temporal evolution of the $\Delta V_{\mathrm{th}}$ is typically performed at dc bias stress conditions at elevated temperatures, however, operation-relevant ac bias conditions can severely affect the degradation both in magnitude and transient shape of $\Delta V_{\mathrm{th}}$ [7], [8]. For device understanding and modeling, e.g., reproduction of the transfer characteristics, detailed knowledge of defect parameters and distributions is obligatory to account for and reproduce the transient charge capture and emission events. Typically, defects are accounted for by introducing normally distributed interface state densities $D_{\mathrm{it}}$, which are dynamically occupied using the Shockley–Read–Hall (SRH) model or simple elastic tunneling models [9]. However, such a modeling approach does not account for structural transformations of the defect site upon the charge transfer reaction. A correct derivation of the charge transition times requires to account for this effect, as has been demonstrated extensively in Si technologies [10]. Recently the degradation of $V_{\mathrm{th}}$ in SiC MOSFETs at dc bias temperature stress has been explained in detail by charge capture and emission in preexisting structural defects [11] employing a two-state nonradiative multiphonon (NMP) defect model [10], which does take structural relaxation of the defect site into account. This physical modeling approach has been shown to reproduce the $\Delta V_{\mathrm{th}}$ recovery peculiarities in large-area transistors over many decades in time. In this work, we extend this modeling approach to explain short-term ac stress and long-term dc stress consistently for three different DMOS technologies. To determine our defect distributions, we employ a recently developed Effective Single Defect Decomposition (ESiD) method [12], which allows us to extract physical defect parameters, as schematically shown in Fig. 1, efficiently and

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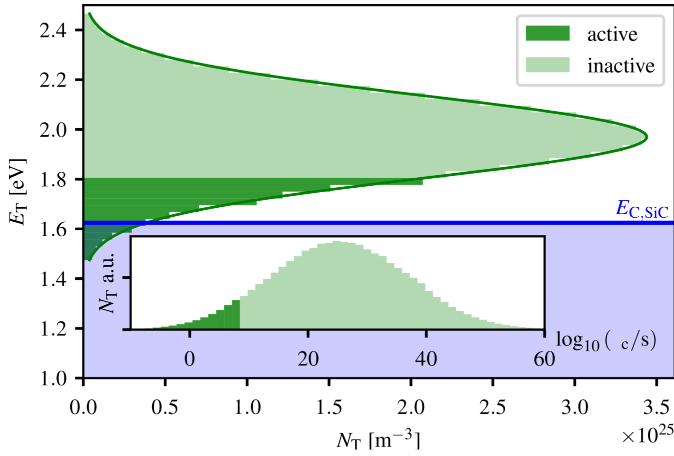


Fig. 1. For defect extraction based on an ESiD algorithm only defects that contribute to the $\Delta V_{th}$ response at the applied gate bias and temperature and fully reproduce the experimental observation in the simulation are considered. As shown schematically, this leads to a significant reduction of the total number of defects used in the simulation compared to the typically assumed Gaussian distributions. Only defects with reasonable capture and emission times $\tau_c$, $\tau_e$ (inset) are considered. The application of this method results in smaller effective defect densities and more physical trap levels $E_T$ and relaxation energies $E_R$.

in a semiautomated manner to reproduce the experimental observation. We further compare the differences and similarities of the extracted defect parameters for the devices under test. In particular, the extracted defect parameters can be compared to such derived from *ab initio* studies of potential defect candidates. Our calibrated simulation framework is then used to extrapolate static bipolar ac stress to typical device lifetimes, which clearly reveals the superposition of electron and hole trapping at operation relevant bipolar bias conditions in SiC-based MOS technologies.

## II. Experimental

We compare three different planar DMOSFET technologies, two of which are subsequent generations of the same vendor (T1/G2, T1/G3) and the third (T2/G1) is the first generation of a different manufacturer. These Si-face channel SiC/$SiO_2$ DMOSFETs have similar nominal oxide thicknesses within a few nm, thus the applied stress voltages result in comparable oxide fields. In order to extract the long-term behavior of $\Delta V_{th}$ at elevated stress gate biases and temperatures, typically constant voltage measure-stress-measure (MSM) sequences [14] are used as illustrated in Fig. 2. Our experiments cover stress times $t_{str}$ in the range of 100 ns to 10 ks at stress gate voltages up to 25 V. To calibrate short-term degradation at operating $V_G$, we use data recorded by employing an adapted bipolar ac stress measurement [13], [15]. In this scheme, a short ac stress signal is applied for $t_{str} = 100$ ms repeatedly. Within the last ac cycle of the stress signal, the stress is interrupted at $t_{ac,interrupt}$ and a $\Delta V_{th}$ recovery trace is recorded for $t_{rec} = 10$ ms by forcing a fixed $I_D = 1$ mA through the channel. The constant recovery current is achieved by employing a feedback loop of an operational amplifier circuit [16], which controls the gate voltage $V_G$ at fixed $V_D$. A minimal measurement delay of $t^{read} = 1.4\ \mu$s for recording $V_G$ after stress can be reached with this setup. The measured $V_G$ is compared to the initial value of the pristine device for the calculation of $\Delta V_{th}$. The interruption point within the ac cycle is altered after each stress phase to obtain short-term stress and recovery at multiple points of the

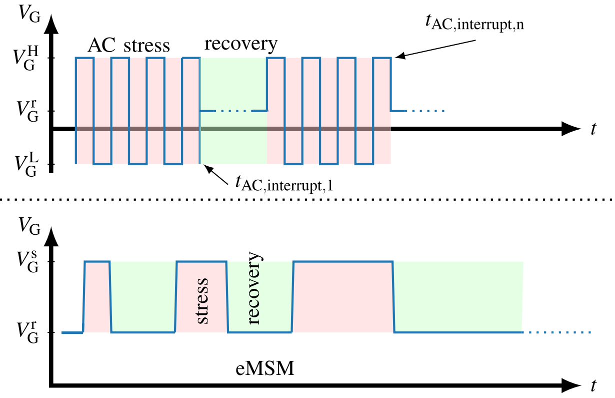


Fig. 2. Applied schemes to extract short-term ac $\Delta V_{th}$ **(top)** and long-term dc PBTI degradation **(bottom)** are shown. Note that the short ac stress is repeatedly interrupted at different points of the ac cycle during the high/low ($V_G^H$/ $V_G^L$) phase, as indicated in the scheme. The shift of $V_{th}$ is recorded during the recovery phase by enforcing a fixed $I_D = 1$ mA through the channel via controlling $V_G$ with a feedback loop [13].

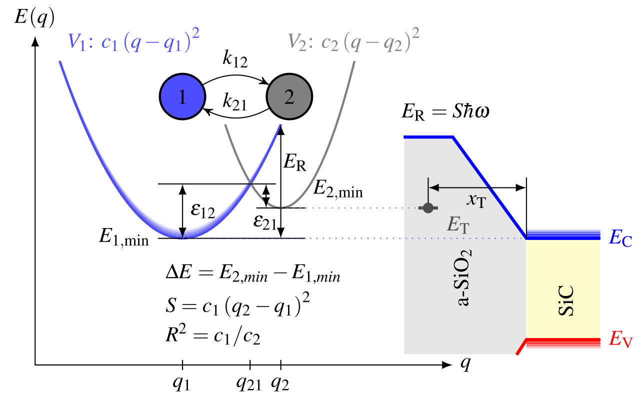


Fig. 3. Transition times for charge transfer reactions at single defects are calculated by employing the NMP model. The configuration coordinate diagram shows the harmonic approximation of the PES of the two defect states. In order to change the defect state, an energetic barrier $\varepsilon_{12}$, $\varepsilon_{21}$ has to be overcome. These barriers are computed from the intersection point of the two harmonic oscillators which change their relative position with gate bias.

ac stress signal. To capture the temperature activation of the charge trapping process all measurements have been conducted at temperatures $T = 25$ °C and 175 °C.

## III. Modeling and Simulation

Our 1-D BTI simulator Comphy [17], which employs a two-state defect model based on NMP theory [10], is calibrated to derive the surface potential from a given gate voltage $V_G$ from the doping concentration in the channel, the oxide thickness and the work-function difference of an ideal device. Subsequently it is used to calculate charge capture and emission events at preexisting defects in order to explain the observed transient $\Delta V_{th}$. The charge transition times are given by [10]

$$\tau_{c/e}^{-1} = n v_{th} \vartheta_{WKB} \sigma \exp\left(-\frac{\varepsilon_{12/21}}{k_B T}\right) \quad (1)$$

with the electron concentration in the channel $n$, the thermal carrier velocity $v_{th}$, a tunneling factor calculated by a Wentzel–Kramers–Brillouin (WKB) approximation $\vartheta_{WKB}$, and a capture cross section $\sigma$, which was chosen constant

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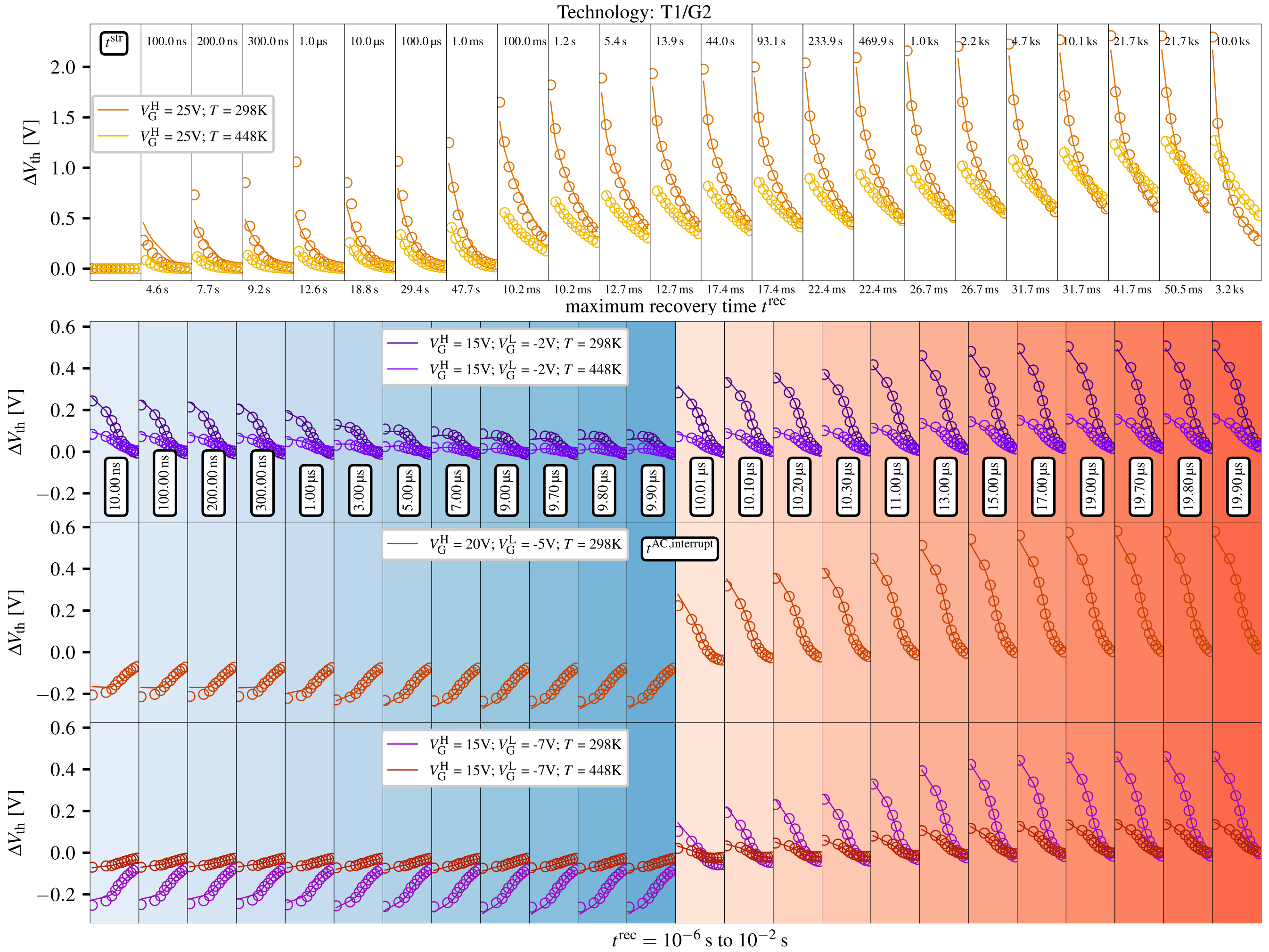


Fig. 4. Comparison of simulation **(lines)** and experimental $V_{\rm th}$ recovery **(circles)** of T1/G2 at long-term dc stress bias **(top)** with stress times $t_{\rm str}$ = 100 ns to 10 ks and recovery times after each stress phase from $t_{\rm rec} = 1$ $\mu$s up to maximum values shown in the horizontal axis. A detailed time resolution of dc traces is shown in Fig. 6. **Bottom** three figures show recovery traces for short-term ac stress ($f$ = 50 kHz, $t_{\rm str}$ = 100 ms) for different interruption times $t_{\rm ac,interrupt}$ during the ac cycle for different $V_{\rm G}^{\rm L}$, $V_{\rm G}^{\rm H}$, and $T$. The simulations can accurately explain the recovery behavior for all applied stress conditions. The leftmost trace of the dc MSM sequence shows an initial readout phase of the pristine device with no stress applied. Note that a higher degradation at *lower* $T$, an effect unknown in Si technologies is observed in all three technologies and is shown in detail in Fig. 6.

at $10^{-15}$ cm$^2$. The capture- and emission barriers $\varepsilon_{12}$ and $\varepsilon_{21}$ are computed from the intersection points of two harmonic oscillators that approximate the potential energy surface (PES) of the two respective defect states, as shown in the configuration coordinate diagram in Fig. 3. Contrary to the frequently used SRH-like models, which are only suitable for describing interface defects without considerable structural relaxation of the defect site, this model accounts for the inelastic tunneling process arising from thermal relaxations due to coupling of the defect to a heat bath. Using this framework, it has been demonstrated for SiC MOSFETs that charge capture and emission at electron traps (conventional MSM) and hole traps (negative pulse MSM) can be accurately explained [11]. Typically, the experimental data are reproduced in the simulation by placing energetically normal and spatially uniform distributed defect bands with the parameters $\langle E_{\rm T}\rangle$, $\sigma_{E_{\rm T}}$, $\langle E_{\rm R}\rangle$, $\sigma_{E_{\rm R}}$, $x_{\rm T}$, and $N_{\rm T}$. These parameters have to be adapted and optimized by a minimization scheme for each defect band to match the measurement data. As mentioned, extraction of these defect parameter distributions is time-consuming, especially in the SiC/SiO$_2$ system with many potential defect bands present, and a good initial guess for the defect parameters is required for this optimization method. To mitigate these challenges, in this work, we employ a novel Effective Single Defect Decomposition (ESiD) approach as presented in [12] to extract physical defect parameters in a semiautomated manner. In this method, the measurement signal is compared to the calculated response of defects within the gate insulator that are sampled across a predefined parameter grid. The measured $\Delta V_{\rm th}$ is therefore reproduced as the superposition of the linear response of the defect grid points with the coefficients proportional to the respective defect density $N_{\rm T}$. The least-square algorithm is applied to find the optimum weights, $N_{\rm T}$, respectively. Defect parameters which produce artificial high $N_{\rm T}$ are further filtered out, until a maximum error criterion for the simulation signal deflection from the measurement signal is achieved. This optimization problem is further regularized with a Tikhonov scheme [18] in order to avoid artificial high defect densities as well as to ensure a smooth density distribution function. The decisive advantage of this method is that barely any assumption about the defect distribution has to be made, and so the calculation of defects with unrealistic high tran-

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TABLE I
GRID PARAMETERS

| Layer | $E_T$ range | $\Delta E_T$ | $E_R$ range | $\Delta E_R$ | $x_T$ range | $\Delta x_T$ |
|---|---|---|---|---|---|---|
| oxide | −3–3 eV | 50 meV | 0.1–5 eV | 70 meV | 0.6–3 nm | 0.1 nm |
| interface | −2.2–2.2 eV | 34 meV | 0.1–3 eV | 70 meV | 0.0–0.5 nm | 0.1 nm |

The grid parameters have been chosen to account for different distributions of defect parameters in the vicinity of the interface and for bulk oxide.

TABLE II
FIXED OXIDE CHARGE

| Symbol | Quantity | T1/G2 | T1/G3 | T2/G1 | Unit |
|---|---|---|---|---|---|
| $Q_f$ | fixed Charge | $2 \times 10^{11}$ | $1.4 \times 10^{12}$ | 0 | $\mathrm{C\,cm^{-2}}$ |

Fixed oxide charge used for the individual technologies to model the device electrostatics at threshold voltage.

sition times is avoided, as schematically shown in Fig. 1. To further ensure physically meaningful defect distributions, different grid parameter spaces have been used as presented in Table I. The twofold parameter constraints represent two layers, one in the vicinity of the interface and one deeper in the oxide. This selection allows us to account for higher defect densities, as well as different defect parameters in the interface layer, which can be justified due to the different stoichiometric composition in the material transition region. Defect densities are uniformly distributed in spatial dimension ($x_T$) within the respective layers. Another major advantage of the ESiD method is that defect distributions can be extracted automatically from recorded $V_{th}$ shifts with little manual effort, which allows us to calibrate our model to a comprehensive input dataset in order to compare different technologies. To extrapolate $\Delta V_{th}$ at bipolar ac bias conditions to typical device lifetimes of $t = 1 \times 10^8$ s (≈10 years) at given operating conditions, an analytical expression [19], [20] is used. As proposed by Ito *et al.* [21], a fixed charge $Q_f$ has been placed at the interface to rebuild the pristine electrostatics, as shown in Table II. The introduction of fixed positive charges at the $SiC/SiO_2$ interface during device manufacturing is discussed in [22]. However, this charge is not accessible within our experimental $T$ and $V_G$ range.

## IV. RESULTS AND DISCUSSION

### A. Simulation Results

Our simulation framework has been calibrated simultaneously to both dc and short-term ac data for all three technologies. It accurately replicates the data considering a large variety of stress/recovery times and bias combinations at the two studied temperatures as is exemplary shown for T1/G2 in Fig. 4. Fig. 5 shows the first points of each recovery trace of the short-term ac stress measurement data compared with the simulation for all technologies. Note that T2/G1 shows the largest degradation for the applied stress conditions when the ac cycle is interrupted during the $V_G^L$ and $V_G^H$ phase and for long-term positive BTI (PBTI) stress, respectively. While T1/G2 shows more negative $\Delta V_{th}$ at more negative $V_G^L$, this behavior cannot be observed for T1/G3, which does not exhibit noticeable negative $\Delta V_{th}$ for any $V_G^L$. The observed maximum positive $\Delta V_{th}$ is comparable for both technologies. Quite interestingly, at 448 K a lower $\Delta V_{th}$ at recovery times smaller than 1 ms can be observed for all three technologies, which can be explained by the faster emission of captured negative charge during the recovery phase, while the degradation of

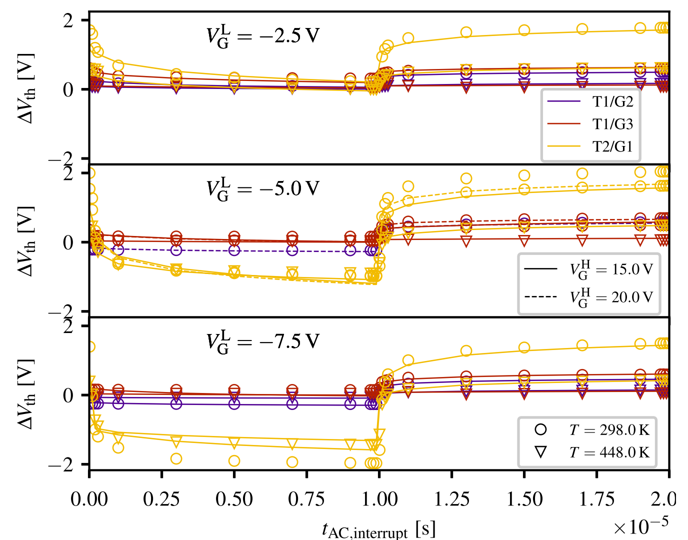


Fig. 5. First points of the measured **(symbols)** and simulated **(lines)** recovery trace after interruption of a short-term ac stress (duty cycle = 0.5, $f$ = 50 kHz, $t_{str}$ = 100 ms) at $t_{ac,interrupt}$ after start of an ac cycle are shown for varying $V_G^L$ and $V_G^H$. The simulation can accurately reproduce all recovery $\Delta V_{th}$ for the shown stress conditions. The technology comparison reveals large $\Delta V_{th}$ for T2/G1 at both polarities, while T1/G3 exhibits no negative $\Delta V_{th}$ at more negative $V_G^L$.

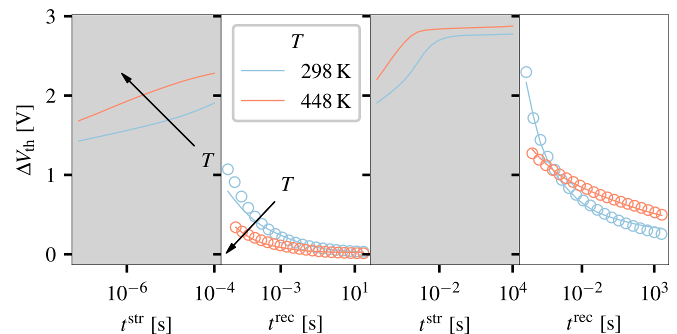


Fig. 6. Stress/recovery simulation is shown for T1/G2 after $t_{str}$ = 100 $\mu$s and $t_{str}$ = 10 ks together with the recovery measurement data. It can be seen that more defects can capture a charge at the higher $T$ resulting in larger positive $\Delta V_{th}$, but at the same time most defects emit faster at elevated $T$, resulting in lower visible degradation during the recovery measurement. In the last recovery phase a turnover after $t_{rec} \approx 1$ ms is observed, in which the measured $\Delta V_{th}$ becomes larger at the higher $T$.

$\Delta V_{th}$ during the stress phase is larger than at 298 K, compare Fig. 6.

### B. Defect Parameters

As shown in Fig. 7 by comparison of the relevant defect parameters ($E_T$,$E_R$), acceptor-like defects are necessary to describe the PBTI behavior which reside in the upper half of $E_G$ in T1/G3. Additionally, donor-like defects in the lower half of the SiC bandgap are prevalent in T1/G2 and T2/G1 leading to visible negative BTI (NBTI) degradation. Also T2/G1 shows defect distributions with larger defect densities $N_T$ in both halves of $E_G$ and the donor-like defects are spread more widely in the energetic dimensions $E_R$ and $E_T$, thereby exhibiting several peaks. Particularly noteworthy is that the relaxation energies $E_R$ of the defects extracted for all three device generations are significantly lower compared to [11], which is a result of setting the curvature ratio between the two

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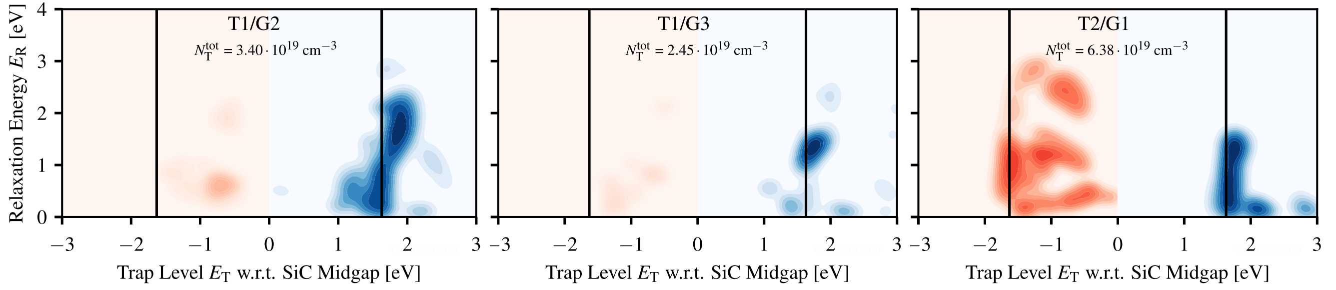


Fig. 7. Extracted defect distributions for the different technologies are shown. While electrically active defects are present in T1/G2 in the lower half of the bandgap **(left)**, their concentration is significantly lower for T1/G3 **(center)**. T2/G1 **(right)** shows larger defect densities for both electron traps close to $E_C$ and hole traps spread widely over the lower half of $E_G$. The relaxation energies show small values for both trap types, similarities are especially observed for acceptor-like defects close to $E_C$ across all technologies. The densities $N_T$ are normalized to the maximum total density of the respective technology and have been scaled by $\log_{10}(1 + \kappa N_T/N_T^{max}) / \log_{10}(1 + \kappa)$ with $\kappa = 10$ to visualize defects with smaller densities.

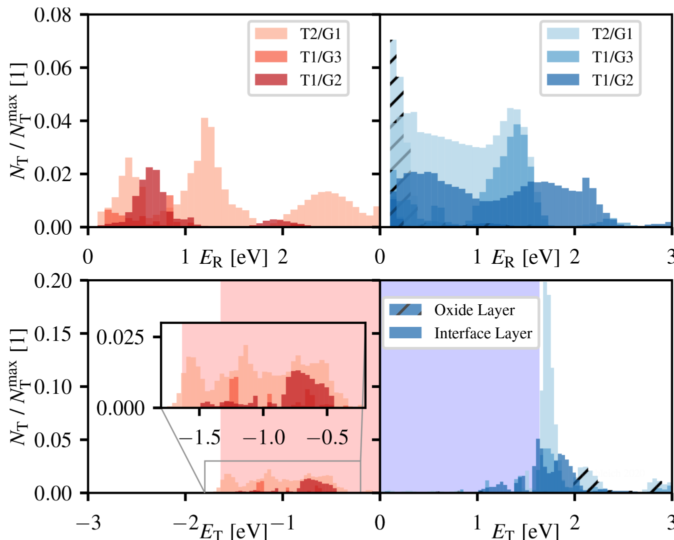


Fig. 8. Comparison of the extracted defects is shown. The distributions are normalized to $N_T = 6.38 \times 10^{19}$ cm$^{-3}$, i.e., the largest extracted defect density for T2/G1. All technologies show a peak of $N_T$ close to $E_C$ **(bottom, right)**. The majority of defects show low relaxation energies $E_R$ **(top)** and are located within 0.5 nm distance to the channel (hashed bars) and therefore assigned to the interface'. T1/G3 shows a negligible amount of defects in the lower half of the bandgap **(bottom, left)**.

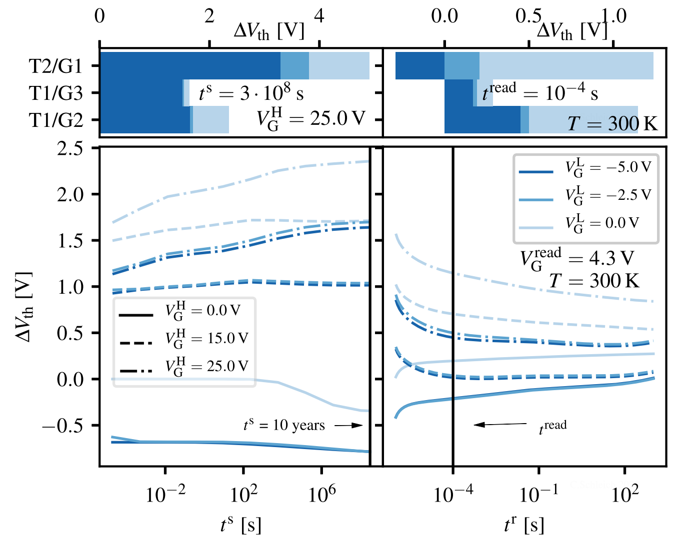


Fig. 9. **(left)** Extrapolation of bipolar ac stress by analytic calculation for T1/G2 is shown **(bottom, left)**. At a device lifetime of $t = 3 \times 10^8$ s (10 years) $\Delta V_{th} \approx 2$ V is reached for the applied operating conditions (duty cycle = 0.5, $f$ = 50 kHz). Simulated recovery traces **(bottom, right)** at constant initial $V_{th}$ show the strong dependence of $\Delta V_{th}$ measurements on the readout time. A comparison of the degradation of all three technologies after $t_{str} = 3 \times 10^8$ s and $t^{read} = 10^{-4}$ s is shown **(top)**.

defect states $R = 1$. This selection is supported by *ab initio* calculations considering defect candidates in a-$SiO_2$ [23]. Note that a large fraction of the defects in all technologies show relatively low $E_R$ values, which is not typically observed in Si technologies for oxide defects [12] but does apply for interface defects, such as $P_b$-centers [24]. The majority of defects are spatially located within a small distance from the SiC/$SiO_2$ interface, which is confirmed by our simulations for all three cases, see Fig. 8 and in line with previous investigations [11]. Both observations support the hypothesis that the vast majority of structural defects is due to the $SiO_xC_y$ transition layer between SiC and $SiO_2$ due to a stepped (off-axis cutting) interface [25], e.g., dangling bonds [26] with potentially low relaxation energies. Consistent among the studied technologies are acceptor-like defects with $E_T$ close to $E_C$ of SiC that lead to positive $\Delta V_{th}$ when charged. The highest density among these defects is found in T2/G1, by a factor of two compared to T1/G2. A possible explanation could be that those defects a related to an enhanced density of N complexed defects, as suggested by electrically detected magnetic resonance (EDMR) measurements [27]. Also, a larger amount of N deposited at the interface during POA employing N containing precursors has been correlated with a higher number of electron traps [28]. In all technologies also trap levels are extracted in the range of $E_T$ with respect to midgap of 2 to 3 eV with comparably low $N_T$, which can most probably be assigned to bulk oxide defects [29]. The distributions of donor-like defects can be tentatively assigned to C complexed structures [30], which exhibit charge transition levels in the same energetic range based on ab-initio calculations.

## C. Extrapolation

The extrapolation of digital ac stress up to a maximum lifetime of 10 years as presented in Fig. 9 shows the strong dependence of the observed degradation on the bias combination ($V_G^L$,$V_G^H$) and on the readout time $t^{read}$ of $\Delta V_{th}$. While comparable degradation can be observed for T1/G2 and T1/G3 during stress, the latter recovers faster and shows lower $\Delta V_{th}$ at $t^{read}$. T1/G3 also shows the lowest variation in $\Delta V_{th}$ both during stress and recovery for all bias combinations and is therefore extrapolated as the most stable device. T2/G1 shows a pronounced overall degradation, but comparably low readout

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values for more negative $V_G^L$ at the selected $t^{read} = 100\,\mu s$, which is a result of the interplay of electron and hole trapping. All technologies show a decreased positive $\Delta V_{th}$ at a readout voltage of $V_G \approx V_{th}$ for the most negative $V_G^L$, which is both due to hole capture in donor-like defects that compensate negative charge at the interface and pronounced electron emission in acceptor-like defects close to $E_C$.

## V. Conclusion

A wide range in $V_{th}$ drifts can be observed for different SiC DMOSFET technologies and described with defect distributions that vary in both the energetic and spatial dimension, as well as their respective defect densities. The majority of the electrically active defects in these devices is located within a small distance to the interface and in the vicinity of $E_C$ and $E_V$ of SiC, respectively, which is clearly revealed by our simulations. Elimination of one defect component (e.g., donor-like traps) leads to unipolar degradation of $V_{th}$ for bipolar stress as observed in T1/G3, and higher stability of $V_{th}$ when extrapolating the device degradation. The diverse degradation behavior in all technologies and its peculiarities can be fully explained by charge trapping at oxide defects employing an NMP model. The wide range of defect distributions is presumably a result of the different interface quality. To identify the impact of process parameters (e.g., POA ambient), characterization and simulation after each manufacturing process step can be conducted with our approach. Finally, our lifetime extrapolation appears to be dominated by superposition of charge transitions in both acceptor- and donor-like defects at bipolar operating conditions, demonstrating that both electron and hole trapping has to be considered to consistently explain $V_{th}$ shifts in SiC-based MOSFETs.

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