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# Crystalline insulators for scalable 2D nanoelectronics

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#### ABSTRACT

Despite the breathtaking progress already achieved for electronic devices built from 2D materials, they are still far from exploiting their full theoretical performance potential. Many of these problems are due to the lack of suitable insulators which would go along with 2D materials as nicely as SiO<sub>2</sub> goes with Si. For instance, amorphous oxides known from Si technologies contain numerous defects which degrade the device performance and stability, and hBN is not suitable for nanoscale devices due to limited dielectric properties. Thus, we suggest that an intensive search of beyond-hBN layered 2D insulators and other crystalline insulators such as CaF<sub>2</sub>, other fluorides and native oxides is required for the further development of next-generation 2D nanoelectronics.

### 1. Introduction

For more than half a century, microelectronics has been driven by Moore's law, which predicts a doubling of the integration density every 18 months and thus exponential growth, which is highly beneficial for economical and performance reasons. Despite many premature claims that Moore's law is at an end, according to the IRDS [1] scaling will continue during the next decade. However, numerous challenges will have to be surmounted, many of them related to the fact that material scaling has reached atomic dimensions, particularly in the vertical direction. For instance, the mobility of silicon starts to deteriorate below 5 nm [2], which can be expected for other 3D materials. Thus, the IRDS lists layered 2D semiconductors as a promising option for ultra-scaled FETs and memory devices after 2028. In line with these requirements, several groups have reported FETs with graphene [3], silicene [4], black phosphorus [5] and transition metal dichalcogenides [6,7] exhibiting excellent transistor characteristics. Research efforts have been mostly focused on finding the best channel materials with the highest mobilities and decent bandgaps. Also, some attempts on circuit integration of MoS2 FETs have been undertaken [8].

However, 2D FETs also need suitable insulators to separate the controlling gate from the channel, which should be scalable and ideally go along with 2D semiconductors as nicely as SiO<sub>2</sub> goes with silicon. The lack of these insulators makes it complicated to fully exploit the predicted performance potential of 2D electronic devices, even despite the

breathtaking progress already achieved in this field. As a result, there is still no commercially competitive 2D transistor technology available today.

# 2. Results and discussion

The selection of suitable insulators for 2D nanoelectronics represents an enormous challenge. However, this problem is of key importance, since scaling of 2D semiconductors towards sub-10 nm channel lengths is only possible with gate insulators scalable down to sub-1 nm equivalent oxide thicknesses (EOT). In order to achieve competitive device performance, these insulators need to meet stringent requirements regarding (i) low gate leakage currents, (ii) low density of interface traps, (iii) low density of border insulator traps and (iv) high dielectric strength [9]. Thus, careful selection requires the analysis of available insulators with respect to these four criteria, which are valid for scalable FETs with 2D channels. As for other devices such as optoelectronics and sensors which do not require aggressive scaling, only the requirements on clean interfaces and low densities of border insulator defects are of key importance. This is because high mobility and stable operation under applied gate bias stress are still required for these devices.

Most widely used insulators for 2D electronic devices are amorphous 3D oxides known from Si technologies (SiO<sub>2</sub>, HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>), while native 2D oxides (MO<sub>3</sub>, WO<sub>3</sub> and Bi<sub>2</sub>SeO<sub>5</sub>), layered 2D crystals (hBN, mica) and ionic 3D crystals (CaF<sub>2</sub> and other fluorides like SrF<sub>2</sub>, MgF<sub>2</sub>) have been

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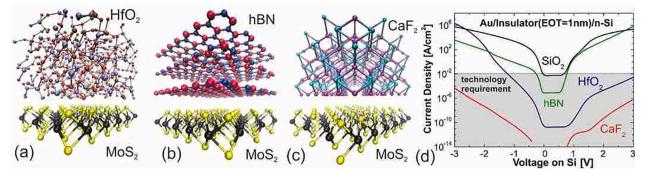


Fig. 1. Schematic structure of  $MoS_2/HFO_2(a)$ ,  $MoS_2/hBN$  (b) and  $MoS_2/CaF_2$  (c) interfaces. (d) Theoretical leakage currents through these insulators for EOT = 1 nm simulated using a simple WKB tunneling model [10].

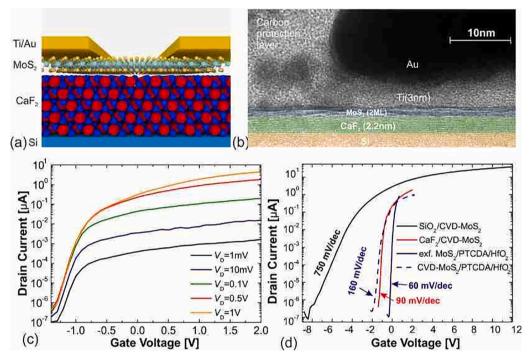


Fig. 2. (a) Schematic cross-section of the van der Waals interface of CaF<sub>2</sub>(111) and an MoS<sub>2</sub> channel in our FETs. (b) TEM image confirming the device structure. (c) Typical gate transfer characteristics of MoS<sub>2</sub> FETs with CaF<sub>2</sub> [18] and comparison with other MoS<sub>2</sub> FETs [19,20] (d).

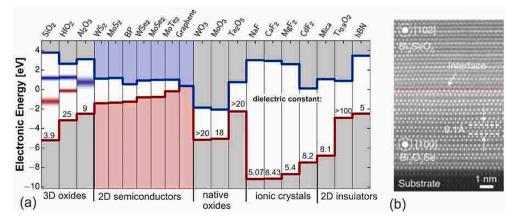


Fig. 3. (a) Band diagrams showing energetic alignments of different insulators relatively to most frequently used 2D semiconductors. For amorphous oxides defect bands are shown. (b) Atomically sharp interface between the 2D semiconductor Bi<sub>2</sub>O<sub>2</sub>Se and its native oxide Bi<sub>2</sub>SeO<sub>5</sub> [13].

also used or considered as promising candidates. However, 3D oxides form poor quality interfaces with 2D semiconductors (Fig. 1a), especially when grown in thin layers, and contain border traps which severely perturb stable device operation [11]. The latter is also valid for some native oxides such as MO<sub>3</sub> and WO<sub>3</sub>, which are non-stoichiometric [12]. As a result, they have a limited dielectric stability which makes it hard to use them in real devices. Nevertheless, other native oxides such as crystalline Bi<sub>2</sub>SeO<sub>5</sub> appear to be more promising and have been already applied in FETs [13], though still require an in-depth analysis of their dielectric properties. The layered 2D insulator hBN, on the other hand, forms excellent van der Waals interfaces with 2D semiconductors (Fig. 1b), but has mediocre dielectric properties ( $E_G = 6 \text{ eV}, \varepsilon < 5$ ) [14] which result in excessive leakage currents for sub-1 nm EOT. The potential of other 2D insulators is currently unclear, in part due to the absence of scalable growth techniques. For instance, only exfoliated flakes of mica have been used in FETs so far [15].

Thus, we suggest that for now the most promising insulators for 2D electronics are 3D ionic crystals like CaF2 which form well-defined interfaces (Fig. 1c). In contrast to hBN, fluorides have good dielectric properties (e.g.  $E_G = 12.1$  eV,  $\varepsilon = 8.43$  for CaF<sub>2</sub> [16]) and thus exhibit low gate leakage currents (Fig. 1d). Also, these insulators have excellent dielectric strength [17] and low density of border traps [18]. Furthermore, fluorides can be epitaxially grown on large-area wafers, thereby enabling fully integrated nanoelectronic devices. Also, careful preparation of Si substrates and the growth temperature of 250 °C lead to very homogeneous CaF<sub>2</sub> films [10,18]. Owing to this, excellent performance of MoS<sub>2</sub> FETs with record thin epitaxial CaF<sub>2</sub> of only 2 nm (0.9 nm EOT) [18] has been achieved recently (Fig. 2a,b), which is barely possible with any other insulator discussed above. Even though these are bare channel back-gated prototypes, they exhibit promising performance (Fig. 2c) such as on/off current ratio up to 10<sup>7</sup> and SS down to 90 mV/ dec while outperforming more mature MoS2 FETs with SiO2 [19] and top-gated devices with PTCDA/HfO2 [20] (Fig. 2d). Thus, further research on these insulators appears a very promising pathway for the development of scalable 2D FETs and other 2D devices with similar structure such as photodetectors and sensors.

We also note that despite all the open challenges, an interesting solution could be still offered by native oxides of 2D materials assuming that they are crystalline. However, it is important to consider that some of them have very narrow bandgaps as compared to conventional oxides and fluorides (Fig. 3a). Nevertheless, recently demonstrated crystalline Bi<sub>2</sub>SeO<sub>5</sub> [13] already offers top-gate integration, while forming an atomically sharp interface with its semiconductor Bi<sub>2</sub>O<sub>2</sub>Se (Fig. 3b).

While the estimated key dielectric parameters of this insulator are  $E_G$ = 3.9 eV and  $\varepsilon$  = 21, further research is required to understand if this narrow bandgap can enable reasonable band offsets with the channel to maintain low gate leakage currents for sub-1 nm EOT. Also, the potential of other insulators of this type should be explored in more detail.

### 3. Conclusions

In summary, 3D oxide insulators appear barely suitable for integration into 2D devices while hBN is not suitable for nanoscale FETs. Thus, an intensive search of beyond-hBN layered 2D insulators and further development of 2D devices with crystalline fluorides and native oxides appears promising for next-generation 2D nanoelectronics.

# **Declaration of Competing Interest**

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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