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# The performance limits of hexagonal boron nitride as an insulator for scaled CMOS devices based on two-dimensional materials

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**Complementary metal–oxide–semiconductor (CMOS) logic circuits at their ultimate scaling limits place extreme demands on the properties of all materials involved. The requirements for semiconductors are well explored and could possibly be satisfied by a number of layered two-dimensional (2D) materials, such as transition metal dichalcogenides or black phosphorus. The requirements for gate insulators are arguably even more challenging. At present, hexagonal boron nitride (hBN) is the most common 2D insulator and is widely considered to be the most promising gate insulator in 2D material-based transistors. Here we assess the material parameters and performance limits of hBN. We compare experimental and theoretical tunnel currents through ultrathin layers (equivalent oxide thickness of less than 1 nm) of hBN and other 2D gate insulators, including the ideal case of defect-free hBN. Though its properties make hBN a candidate for many applications in 2D nanoelectronics, excessive leakage currents lead us to conclude that hBN is unlikely to be suitable for use as a gate insulator in ultrascaled CMOS devices.**

Research on using two-dimensional (2D) materials and van der Waals (vdW) heterostructures to create nanoelectronics is predominantly focused on semiconductors[1]. Semiconducting 2D materials could potentially outperform silicon at the ultimate scaling limit[2], but field-effect transistors (FETs) with dimensions scaled down to a few atomic layers also require suitable insulators. To fully exploit the options offered by vdW heterostructures, these insulators should ideally provide a layered 2D structure[3]. Hexagonal boron nitride (hBN) is widely considered to be the most promising 2D insulator[4]. Numerous studies have demonstrated the potential of hBN when used as a substrate and gate insulator in FETs at the proof-of-concept level, where thick insulators are employed[5–7]. There is, however, only a limited number of studies about the suitability of hBN as an insulator at the scaling limit of one to six atomic layers thickness (0.33–2 nm)[8–10]. A commonly held view is that this lack of attention is the result of the immaturity of this material system and the technological difficulties related to device fabrication based on only a few layers of hBN.

In this Perspective, we examine the performance limits of hBN in its ultrathin form. We first summarize the state of the art in the synthesis of hBN and illustrate the main technological challenges for batch fabrication of few-layer structures that are to be used as part of the gate stacks in nanoscaled FETs. One of the main benefits of including hBN in the gate stack is the perfectly clean vdW interface it can form with other 2D materials. This is an advantage over conventional 3D insulators such as $SiO_2$ or $HfO_2$, which typically exhibit large densities of dangling bonds and charged impurities at the interfaces with 2D materials. These interfacial defects act as scattering centres and severely degrade the mobility, in addition to causing various instabilities. However, like any other material, hBN is not free of atomic defects, and films grown using different methods show very different defect types and densities. Most importantly for FETs, these defects substantially increase the leakage currents through thin hBN layers via trap-assisted tunnelling (TAT).

We subsequently consider the material properties of hBN, and argue based on them that the comparatively high tunnel currents through thin hBN layers make it difficult for the material to satisfy the stringent requirements for scaled insulators. Insulators in modern FETs should be thinner than 1 nm equivalent oxide thickness (EOT), whereby 1 nm EOT means that 1 nm of $SiO_2$ would give the same electrostatic control over the channel. Owing to the low dielectric constant of hBN ($\varepsilon \approx 5$), this corresponds to thin hBN films of less than four layers (1.32 nm). This issue is analysed by studying experimental and theoretical tunnel currents through hBN. Calculations are performed for perfectly single-crystalline, defect-free hBN and provide a lower estimate for the best-case leakage current levels through thin hBN layers. We conclude that even in the most optimistic case, hBN is unlikely to be a good choice for a gate insulator in nanoscaled 2D complementary metal–oxide–semiconductor (CMOS) logic.

## Synthesis of hBN

At present, it is difficult to experimentally identify the scaling potential of hBN, as high-quality, single-crystalline multilayer films are difficult to fabricate. Besides, high-quality multilayer hBN is currently impossible to grow with batch-compatible processing, as requested by industry standards. At the same time, the strong variations in sample properties of hBN films show they are not yet

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competitive with mainstream silicon technology, which has been optimized for over half a century. To better understand whether the limitations of hBN are a consequence of its immature processing or of its intrinsic material properties, the state of the art of hBN synthesis is briefly summarized here.

Many studies use hBN flakes exfoliated from high-purity crystals. The quality of the single crystals from which few-layer samples are exfoliated is key as it determines the purity and crystal quality of the hBN samples after exfoliation. As for any high-purity material, the growth of high-quality, single-crystalline hBN is challenging. At present, the most successful method for growing hBN single crystals was developed by Taniguchi and Watanabe[11] and relies on high pressures of around 5 GPa and high temperatures of up to 1,650 °C. Equally important as starting from a highly pure crystal is the careful execution of the mechanical exfoliation. Soon after the demonstration of mechanical exfoliation using adhesive tape to thin down and isolate monolayer graphene, the method was applied to obtain mono- and few-layer samples of hBN[12]. However, mechanical exfoliation is an inherently random process where single 'good' flakes have to be selected out of hundreds of 'bad' flakes that do not meet the requirements regarding thickness homogeneity, size and shape. Therefore, this method is incompatible with the processing standards required by industrial applications, and scalable batch processes for the fabrication of hBN layers are heavily investigated[10,13,14].

The most widely explored scalable growth method is chemical vapour deposition (CVD), where hBN is deposited in a furnace under a wide range of low pressures of 0.01 Pa to 100 Pa at temperatures between 1,000 °C and 1,300 °C from the reaction of ammonia borane or borazine on a copper surface[15]. Recently, single-crystalline, large-area hBN monolayers have been grown on sputter-deposited crystalline Cu (111) surfaces on *c*-plane sapphire wafers[10]. During growth, hBN orients itself along the Cu (111) steps. However, one monolayer of hBN is too thin (0.33 nm) to act as an insulator in FETs as it will result in excessive leakage currents. Therefore, the growth of single-crystalline, multilayer hBN is required, but multilayer growth is even more challenging as the reaction can no longer be catalysed by the copper substrate. This limitation was overcome by using an excess partial pressure of the borazine precursor that, however, resulted in a polycrystalline layer[16]. A different approach to avoid the surface-mediated, self-limited growth of multilayer hBN on copper is to use a different substrate such as iron, which possesses high solubility for boron and nitrogen and can mediate a precipitation growth mechanism[17]. This approach was developed further by using a liquid iron-boron alloy as a catalyst for epitaxial precipitation of hBN on (0001) sapphire substrates[13]. This vapour–liquid–solid growth process was used to synthesize highly crystalline, multilayer hBN samples on areas of up to 10 $cm^2$.

In addition to CVD, three other growth techniques potentially offer epitaxial growth of single-crystalline, multilayer hBN on a large scale. These are metal–organic chemical vapour deposition, molecular beam epitaxy and atomic layer deposition. Metal–organic chemical vapour deposition is based on the same process as CVD but uses gaseous metal–organic compounds as precursors, for example, triethylborane and ammonia for hBN growth. Reasonable crystal quality at moderate growth rates can be obtained when growing hBN on *c*-axis sapphire[18]. Contrary to CVD, which relies on the catalytic effect of the substrate, molecular beam epitaxy allows for direct in situ growth of vertically stacked heterostructures[19]. Atomic layer deposition growth relies on gaseous precursors, for example, boron trichloride and ammonia, which are introduced in alternating pulses into the growth chamber where material is deposited on a heated substrate[14]. The growth temperature for this process, at 600 °C, is too high for good compatibility with standard CMOS processes but is already much lower than in all other studies where the growth temperature exceeds 1,000 °C.

While all four methods of depositing hBN have made progress over the past decade, the growth of single-crystalline, multilayered hBN on large areas remains highly challenging. Therefore, the exploration of the benefit of single-crystalline, bulk hBN as a substrate in nanoelectronics currently relies on the use of exfoliated flakes as a convenient test platform.

## Electronic transport in hBN-based heterostructures

The main advantage of hBN as a gate insulator is the clean vdW interface it forms with 2D semiconductors. In fact, the ultimate thinness of 2D semiconductors makes electronic transport through these layers particularly susceptible to the impact of interfaces and to the surroundings of the layers in general. Scanning tunnelling spectroscopy shows not only that the topography of 2D semiconductors is determined by the roughness of the underlying $SiO_2$ substrate but also that the charge density and the bandgap vary drastically depending on trapped charges in the $SiO_2$ (ref. [7]). If instead of $SiO_2$ an hBN substrate is used, the atomically flat vdW interface substantially reduces charge disorder in the system and minimizes extrinsic sources of charge carrier scattering, such as surface roughness, as well as scattering by charged impurities and remote phonons[20].

By performing temperature-dependent measurements of the mobility, two main sources of scattering can be identified and isolated, namely phonon scattering that dominates at temperatures >100 K and impurity scattering that determines the resistivity at low temperatures. It has been shown that the low-temperature, impurity-dominated mobility in $MoS_2$ samples is up to two orders of magnitude higher when $MoS_2$ is encapsulated with 10–30-nm-thick hBN layers than when placed directly on $SiO_2$ (ref. [21]). The reason for this is the reduced defect density in hBN compared with the $SiO_2$ interface.

For scattering at defects, two different mechanisms can be distinguished: long-ranged Coulomb scattering at charged impurities in the insulator and short-ranged scattering at interfacial imperfections such as dangling bonds. The densities of interfacial, charged impurities can be extracted by calculating the scattering rates at interfacial Coulomb potentials. In this way, the low-temperature mobility of hBN-encapsulated $MoS_2$ was modelled with a charged impurity concentration of $6\times10^9$ $cm^{-2}$ (ref. [21]), which is more than two orders of magnitude lower than the concentration of fixed interfacial charges of $10^{12}$ $cm^{-2}$ observed in $MoS_2$ on $SiO_2$ (ref. [22]). The Coulomb scattering model also shows that the mobility is enhanced when increasing the distance of the charge centroid, located in the centre of the semiconducting layer, from the Coulomb scatterers. This distance can be increased either by increasing the thickness of the semiconductor or by introducing an hBN interlayer in between the semiconductor and the conventional amorphous oxide. It has been shown that the mobility improves by one order of magnitude when the $MoS_2$ thickness is increased by 2 nm (ref. [21]) and it is expected that an hBN interlayer would have to be at least 3.3 nm thick (corresponding to ten hBN layers) to be able to effectively screen fixed charges at the underlying interface with $SiO_2$.

The dielectric environment influences not only the impurity-dominated, low-temperature mobility in 2D semiconductors but also the phonon-limited mobility at room temperature. In particular, electrons in ultrathin semiconductor layers can excite phonons in the surrounding dielectrics via long-ranged Coulomb interactions, if the dielectric supports polar vibrational modes[23]. This so-called remote phonon scattering or surface optical phonon scattering has been identified as the dominant phonon scattering mechanism in graphene devices[24]. If the dielectric interface has a high density of interfacial charged impurities, for example, above $10^{12}$ $cm^{-2}$, Coulomb scattering at these defects dominates. As a consequence, the mobility is higher when dielectrics with large dielectric constants (high-*k* dielectrics), such as $HfO_2$, are used because the enhanced dielectric screening reduces Coulomb

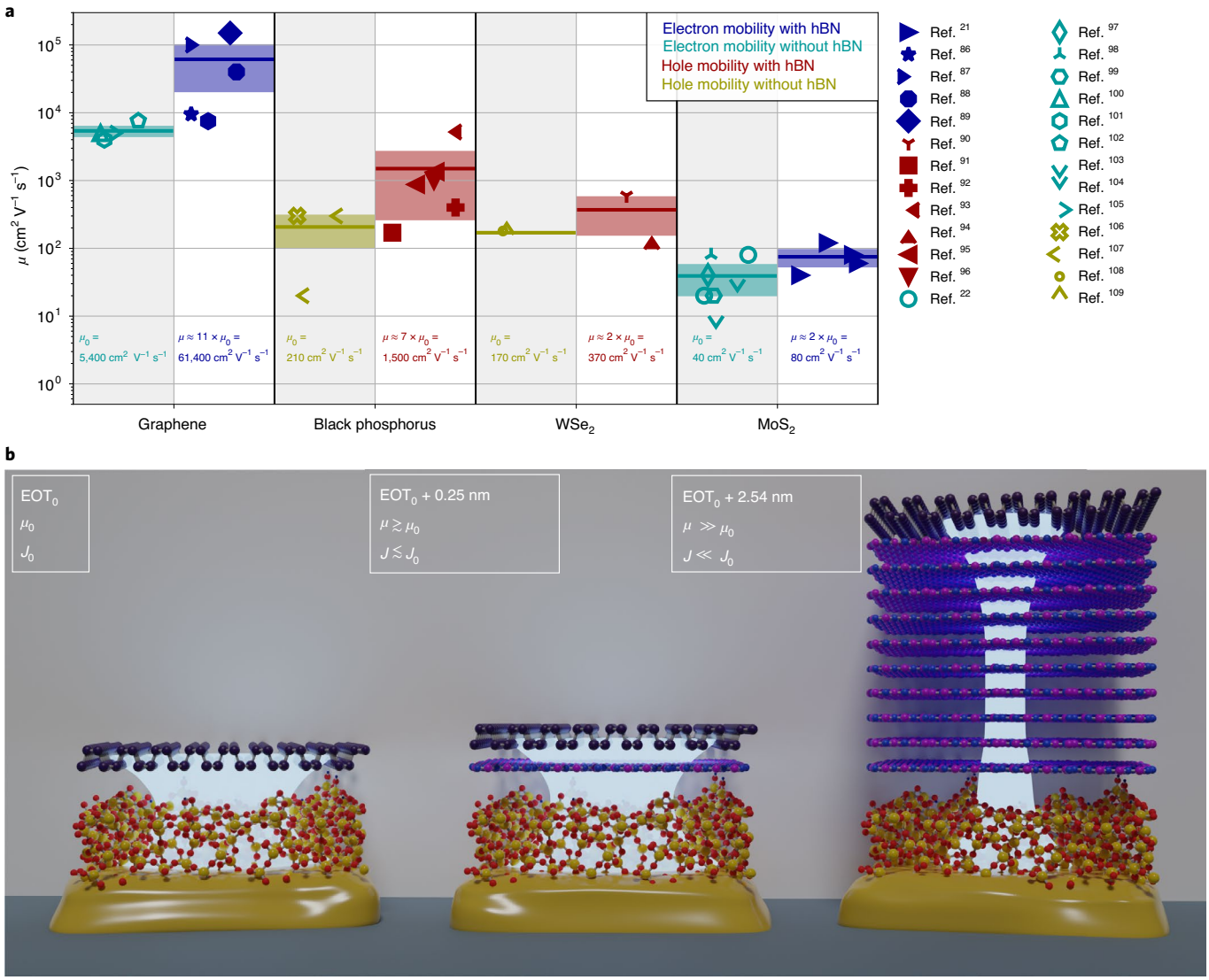


**Fig. 1 | hBN heterostructures. a**, Mobility in hBN heterostructures. For 2D materials, the mobility increases when hBN forms a direct interface with the 2D semiconductor. The mobility values are collected from refs. [21,22,86–109], where four-probe measurements, ideally Hall measurements, were performed, thereby ensuring the accuracy of the values. The lines indicate the mean values, which are also explicitly stated in the respective columns, and the shaded areas correspond to one standard deviation (1$\sigma$). Here $\mu_0$ is the mobility without an hBN substrate and $\mu$ is the mobility with hBN. **b**, Impact of hBN interlayers. The inclusion of several hBN layers (B, pink; N, blue) at the interface of black phosphorus (P, purple) with $SiO_2$ (Si, yellow; O, red) is shown, illustrating that only thick hBN interlayers ($d > 3.3$ nm, EOT > 2.5 nm) can sufficiently suppress Coulomb scattering and remote phonon scattering in the underlying oxide to assure high mobilities. In addition, the pillars illustrate the reduction of the current density through the insulating stack for increasing hBN interlayer thickness. $EOT_0$, $\mu_0$ and $J_0$ denote the EOT, channel mobility and current density for the gate stack on the left without hBN. Here, black phosphorus could be exchanged with any other 2D material and $SiO_2$ with any other amorphous oxide, for example, $HfO_2$.

scattering. If, however, the interface is clean and has a small density of charged impurities, surface optical phonon scattering dominates and the mobility is degraded the most if the 2D layer is surrounded by high-$k$ dielectrics, as they allow low-energy polar vibrational modes[23]. In theory, it is possible to form heterostructures of a high-$k$ dielectric and an hBN layer at the interface to the 2D semiconductor, which would improve the mobility without sacrificing the high permittivity of the overall stack. However, one might expect that to efficiently damp out the surface optical phonon scattering, several nanometres of hBN would be required, though this has to be investigated further.

A considerably improved mobility in FETs with a gate stack that includes high-quality, multilayer hBN at the interface to the 2D channel material has in fact been demonstrated in numerous experiments, as can be seen in Fig. 1a, where the mobility of metal–oxide–semiconductor FETs (MOSFETs) with and without an hBN interlayer is compared. To ensure the highest possible accuracy of the given values, only four-probe measurements of the mobility, and ideally Hall mobility measurements, at room temperature on devices fabricated from exfoliated layers are taken into account. The prospect of maintaining a high mobility (>100 $cm^2 V^{-1} s^{-1}$) is the key advantage of 2D materials at the ultimate scaling limit over ultrathin silicon layers[2], thus a high mobility is essential. In the schematic in Fig. 1b, it is illustrated that several nanometres of hBN are required to obtain the maximum performance benefit from including an hBN interlayer in terms of mobility increase.

In addition to an improved mobility, hBN enhances device performance in other ways as well. For instance, the reduced scattering

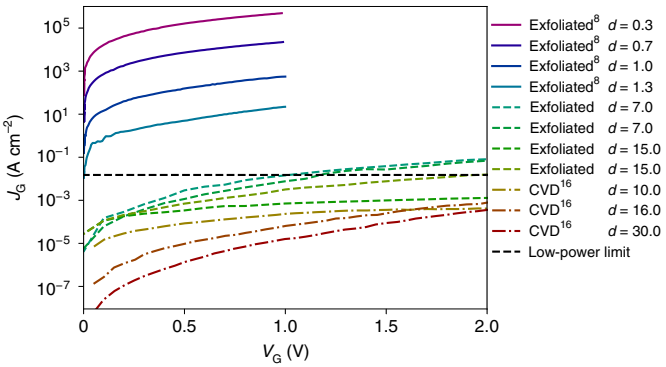


**Fig. 2 | Measured leakage currents through hBN.** A comparison of the experimental tunnel current densities through hBN as reported in literature[8,16] and measured on our samples. $J_G$, tunnel current density per area. Each line corresponds to a different device with the physical thickness $d$ of hBN given in nm. Some of the devices are based on exfoliated hBN while others rely on CVD-grown hBN, marked by dash-dotted lines. Dashed lines are for exfoliated samples of EOT > 8 nm and solid lines for EOT ≤ 1 nm.

in hBN-based heterostructures decreases the inhomogeneous broadening of the excitonic linewidth[25]. Furthermore, several physical phenomena, for example, superconductivity in magic angle graphene[26], rely on encapsulation in high-quality hBN multilayers. Beyond its use as a substrate, hBN is a promising material on its own for numerous applications. Capacitors based on multilayer hBN show a pronounced resistive switching behaviour that can be used in resistive random access memories, which in turn could serve as solid-state synapses in neuromorphic circuits[27]. The high mechanical strength and flexibility of hBN render it promising as a gate insulator of flexible FETs[28] and its small dielectric constant can be decreased further if it is deposited in amorphous form, thereby rendering it an ideal candidate for an interconnect isolation material[29].

## Impact of defects in hBN

Unlike optoelectronic devices and radio-frequency FETs, digital CMOS logic FETs require insulators with sub-1 nm EOT to be competitive with scaled silicon technologies. Moreover, these devices operate at high electric fields and so could benefit from the high dielectric strength of hBN[30]. However, hBN has a moderate bandgap ($E_G \approx 6$ eV) and a comparatively small dielectric constant ($\varepsilon \approx 5$), which requires the use of thin layers as, for example, only three atomic layers correspond to an EOT of 0.76 nm. As a consequence, the measured tunnel leakage currents through hBN are high ($J \approx 10^2$ A cm$^{-2}$ for an applied gate voltage ($V_G$) of $|V_G| \leq 0.7$ V)[8]. Furthermore, at the present state of the art, the reported currents through hBN typically vary over orders of magnitude (Fig. 2), which suggests that the leakage current strongly depends on the material quality and thus on the growth method used. This dependence on the defect density in hBN implies that the leakage current is dominated by TAT[31]. Such large leakage currents would render hBN unsuitable as a gate insulator of scaled CMOS technologies, as they would considerably increase the off-state currents of the FET. In the following, the origins of the large tunnel currents are discussed to evaluate whether these currents are purely defect-mediated and could be sufficiently reduced in hBN samples of high quality.

Localized defect states within the bandgap of hBN give rise to conductive channels in the hBN. As such, the density of defects and consequently the density of conductive channels determines the current density. To give a realistic estimate of the tunnel current density through an hBN layer, it is important to know the prevalent defect types and corresponding defect densities in the sample. In principle, point defects, local aggregates of point defects and line defects such as dislocations are distinguished. Every point defect is characterized by its vertical depth within the hBN stack, its energetic trap level within the bandgap of hBN and its atomic structure. The defect types can be characterized from two different angles, from purely theoretical calculations based on density functional theory (DFT)[32] or from defect spectroscopy on hBN samples[33]. Weston et al.[32] performed first-principles calculations on native point defects and atomic impurities in hBN. They found that atomic carbon, oxygen and hydrogen impurities in hBN have comparatively small formation energies and are expected to be present in notable concentrations in undoped hBN. Strand et al.[34] analysed divacancies and found that boron and nitrogen vacancies form stable configurations where adjacent layers are connected with interlayer molecular bridges. These interlayer connections could play a central role in current transport through the hBN layers in the vertical direction.

Greenaway et al.[33] studied resonant tunnelling through localized states within an hBN tunnel barrier between two graphene electrodes at low temperatures of a few kelvin. From the analysis of tunnelling via hBN defect states, an increased defect density in between adjacent hBN layers was found. This indicates the prevalence of defect clusters in between separate hBN layers, which connect via covalently bonded structures to the otherwise loosely vdW bonded layers. This observation confirms the hypothesis that defect clusters, where molecular bridges connect adjacent layers, play an important role for tunnelling processes through hBN[34]. Other experimental methods to analyse the defect density in hBN include high-resolution transmission electron microscopy on freestanding hBN layers[35] or scanning tunnelling microscopy using graphene as a capping layer to create a conductive surface[36]. However, all experimental methods to explore defect states in hBN layers reported so far have focused on identifying single atomic defect states, which is not sufficient for a comprehensive modelling of the impact of prevalent traps on the tunnel current. Recent large-scale synthesis of high-quality hBN samples[13] has opened up the path to performing non-destructive analysis of the defect densities throughout the whole bandgap of hBN using capacitance voltage or charge pumping measurements, where large device areas are required. In addition, most experimental defect analyses in hBN have focused on exfoliated hBN of the highest quality and only a few report on hBN grown using other methods. In fact, a reference comparing the logarithmic tunnel current density as a function of gate voltage for samples with given hBN thicknesses and electrode areas could provide valuable information about different defect densities in hBN synthesized with different methods. A comparison of available current densities in Fig. 2 may serve as a blueprint for future comparisons of differently synthesized hBN.

In light of the many unknowns related to defects in hBN, an analysis of the best-case scenario without any defects is more conclusive than a TAT model of the leakage current for one particular sample. In any material system, the introduction of defect states increases the gate leakage current density. Therefore, a comparison of the lower limit of the leakage current without accounting for the impact of defects can establish the theoretical performance potential of a material.

## Performance projections for scaled hBN

To estimate the performance potential of hBN, we establish a theoretical lower limit of how small tunnel leakage currents through hBN could be if there were no defects within the layer. An analysis of the ideal situation is of key importance as it relies on inherent material properties that cannot be addressed by improving the material quality via breakthroughs in the synthesis methods but only by developing a different material system. We therefore calculated the tunnel current through hBN based on the intrinsic material properties of single-crystalline, multilayer hBN. According to these theoretical

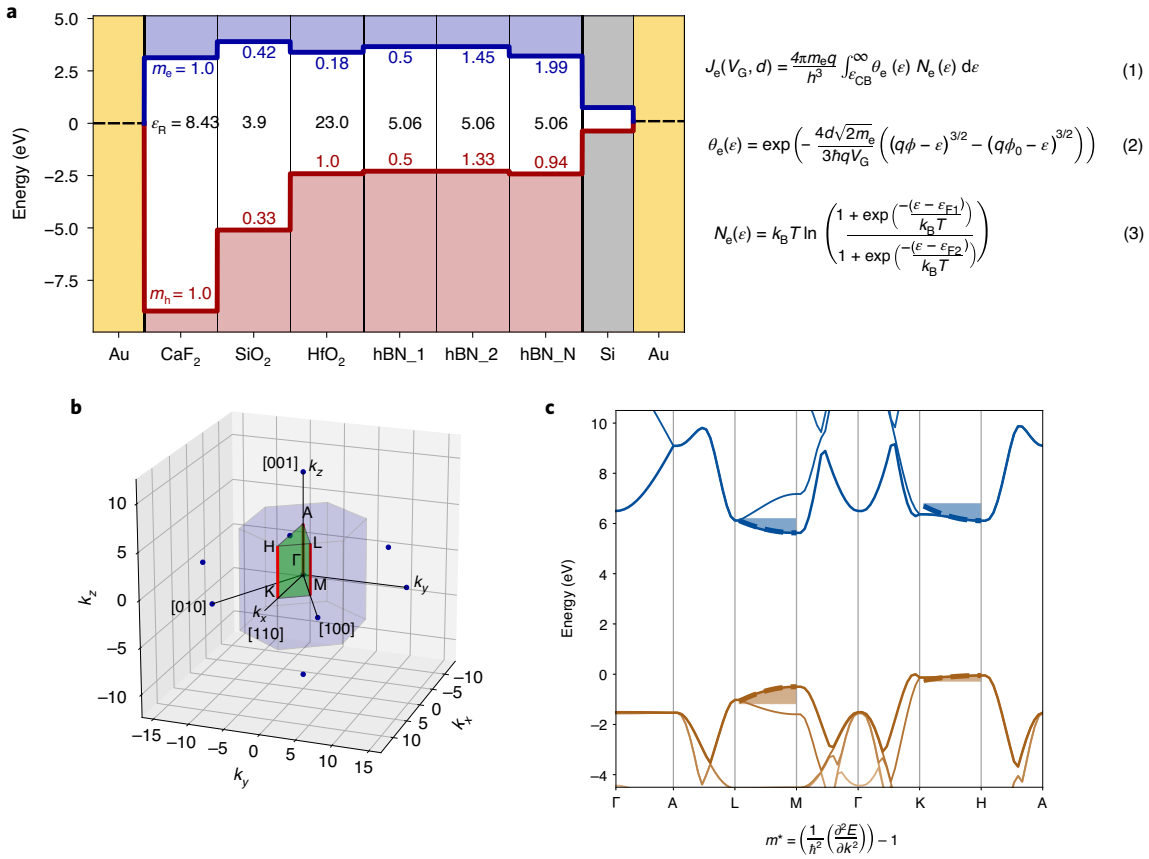


**Fig. 3 | hBN band structure. a**, Band diagram and Tsu–Esaki model. The Tsu–Esaki equations describe the electron contribution to the direct tunnel current density $J_e$ through an insulating barrier. Here $q$ is the elementary charge, $h$ the Planck constant, $\hbar$ the reduced Planck constant, $k_B$ the Boltzmann constant, $T$ the temperature, $\theta_e$ the electron tunnel coefficient, $N_e$ the electron supply function, $E_{CB}$ the conduction band edge energy, $E_{F1}$ the Fermi level in the left contact (the metal) and $E_{F2}$ the Fermi level in the right contact (the semiconductor). In addition, the band alignment of hBN is shown compared with other common dielectrics and several sets of plausible material parameters of hBN are given with hBN_N denoting the material parameters calculated and used in the DFT+NEGF calculations. **b**, Hexagonal Brillouin zone of hBN. The hexagonal symmetry of the hBN lattice causes a hexagonal Brillouin zone, which is shown in the momentum space spanned by $k_x$, $k_y$ and $k_z$ with all the high-symmetry points labelled. The red lines highlight the two valleys contributing to transport in the $z$ direction, the H → K and M → L valleys. **c**, hBN band structure. The band structure of hBN as calculated with HSE06 is shown. It can be seen that the bands along H → K and M → L, which contribute to vertical transport, are comparatively flat. The definition of the effective mass ($m^*$) is given as the second derivation of the energy ($E$) with respect to the momentum ($k$) and the parabolas corresponding to the effective masses are shown with dashed lines and a shaded background.

considerations, the tunnel current densities through hBN could be considerably smaller than the values experimentally reported, possibly even staying below the low-power limit ($J = 1.5 \times 10^{-2}\,\mathrm{A\,cm^{-2}}$ for $|V_G| \leq 0.7$ V). In the following analysis, we will consider this most optimistic scenario and focus on the TAT-free best case.

**Calculation of tunnel currents.** We performed simulations for a system of three layers of hBN corresponding to an EOT of 0.76 nm according to the current technology node[37]. The hBN layers were placed between a gold electrode with a work function of 4.7 eV and a bottom p-doped silicon layer (acceptor doping density $N_A = 10^{18}\,\mathrm{cm^{-3}}$, donor doping density $N_D = 10^{10}\,\mathrm{cm^{-3}}$), forming a metal–insulator–semiconductor structure. The current through this structure was calculated using the Tsu–Esaki model[38] as implemented in Comphy[39]. Within this model, the tunnelling transmission probability is approximated by a Wentzel–Kramers–Brillouin (WKB) factor and the expressions for the electron current are given in equations (1)–(3) in Fig. 3a. Similar expressions are also valid for the hole current, that is, for carrier transport between the silicon valence band and the metal. The tunnel current depends most strongly on the parameters in the exponential WKB factor, given in equation (2), and as such on the layer thickness ($d$), the applied voltage ($V_G$) and the material parameters of the energy barrier heights ($\phi, \phi_0$) and the effective tunnel masses for electrons ($m_e$) and holes ($m_h$). Another material parameter that indirectly affects the layer thickness is the dielectric constant ($\varepsilon_R$), which defines the equivalent oxide thicknesses ($\mathrm{EOT} = \frac{\varepsilon_R}{\varepsilon_{R,SiO_2}} d_{SiO_2}$). Here we use as a dielectric constant an experimentally determined value for hBN of $5.06\varepsilon_0$ that has served as a reference value for many years[40], even though DFT calculations recently obtained a smaller value of $3.76\varepsilon_0$ (ref. [41]). The discrepancy between these values is unclear and the use of the higher value aligns with the aim of presenting the best-case scenario and the lowest possible estimate for the tunnel leakage currents. The band diagrams for hBN according to various plausible sets of material parameters are shown in Fig. 3a compared with other commonly used insulators. In addition, in Table 1, the material parameters of hBN are listed and the parameter trends required for efficiently suppressing a direct tunnel current are included. For minimizing the tunnel current, the bandgap has to be large to ensure high energy barriers, the effective masses have to be large and the dielectric constant also has to be as high as possible, as this corresponds to a large physical layer thickness for a given EOT, even

though this needs to be balanced against high charge carrier mobilities in the semiconductor.

It is important to note that with this methodology we can only give a range of tunnel current estimates through hBN, shown as the blue shaded area in Fig. 4a. This is because the effective tunnel masses for electrons and holes are important but these empirical parameters have only barely been studied in the past. Here we used two sets of parameters. The first set of small tunnel masses, corresponding to high currents, was taken from ref. [8], where the tunnel masses were calibrated to experimental data. We hypothesize that the agreement achieved in this work was probably due to a severe underestimation of the effective tunnel masses that control the tunnel current which compensated for the neglect of TAT in the model. This set was used for the simulations of hBN_1. The second set of high tunnel masses, corresponding to small currents, was adapted from ref. [42], where the effective masses were extracted from DFT calculations of the band structure of bulk hBN. This set was used for the simulations of hBN_2. The calculation of the effective tunnel masses for out-of-plane transport through hBN from the DFT band structure is nearly impossible for two reasons. First, two valleys contribute to the out-of-plane transport in bulk hBN, the M → L and H → K valleys. These two valleys are highlighted in red in the depiction of the hexagonal Brillouin zone of hBN in Fig. 3b. Second, the band structure of hBN along the M → L and H → K orientations is nearly flat, which corresponds to high tunnel masses, but also leads to large uncertainties in the extraction of the effective masses from bands with a small curvature. The band structure as calculated by the HSE06 hybrid functional[43] is shown in Fig. 3c, where the comparatively flat bands along these two orientations can be seen and parabolas corresponding to the effective masses are shown. This small curvature directly originates from the layered structure of hBN and as such from the high inherent anisotropy of a layered material. Therefore, the effective electron mass is most likely overestimated in ref. [42] and was adapted here to a smaller, more plausible value based on the currents we simulated with ab initio methods, as explained below. The wide blue shaded area in Fig. 4a that spans in some regions more than four orders of magnitude demonstrates the importance of future studies on extracting effective tunnel masses for electrons and holes through hBN.

To avoid the problem of calculating effective masses and to increase the accuracy of the estimated currents through defect-free hBN, we simulated the current through Au–hBN–Si structures using a non-equilibrium Green's functions (NEGF) approach combined with DFT. In these full-band transport simulations, the Hamiltonian and overlap matrices of the considered devices were first calculated with the CP2K package[44] based on the HSE06 hybrid functional[43]. These matrices were then loaded into a quantum transport solver[45] to obtain the current–voltage characteristics of the metal–insulator–semiconductor stack using the same electrostatic potentials as in the WKB case.

**Performance projections.** The results of both approaches (DFT+NEGF and the Tsu–Esaki range) are in good agreement, as can be seen in Fig. 4a. Only for small gate voltages is the tunnel current underestimated by the range we obtain from the Tsu–Esaki model. When comparing the leakage currents through hBN with other insulators, it becomes clear that at a small EOT of 0.76 nm, the gate leakage through hBN is slightly lower than through $SiO_2$. However, both are orders of magnitude higher than through the high-$k$ dielectric $HfO_2$ and through crystalline $CaF_2$ (ref. [46]). We expect that in actual samples of any of these materials, the currents will probably be higher than calculated here because the impact of TAT has been neglected to establish the lower limit of theoretically attainable tunnel currents. This demonstrates that in the best-case scenario, tunnel currents through hBN will be orders of magnitude higher than, for example, through the high-$k$ dielectric $HfO_2$.

**Table 1 | Material parameters of hBN**

| Trend | Parameter | | Value | Reference | Used for |
|---|---|---|---|---|---|
| ↑ | Bandgap, $E_G$ | | 5.95 eV | 63,64 | hBN_1, _2 |
| | | | 5.63 eV | – | hBN (NEGF) |
| – | Electron affinity, $\chi$ | | 1.14 eV | 65 | hBN_1, _2 |
| | | | 1.30 eV | 34 | – |
| | | | 1.59 eV | – | hBN (NEGF) |
| ↑ | Dielectric constant, $\varepsilon$ | | 5.06 $\varepsilon_0$ | 40 | hBN_1, _2 |
| | | | 3.76 $\varepsilon_0$ | 41 | – |
| ↑ | Electron mass, $m_e$ | – | 0.50 $m_0$ | 8 | hBN_1 |
| | | – | 1.45 $m_0$ | – | hBN_2 |
| | | (M → L) | 2.21 $m_0$ | 42 | – |
| | | (M → L) | 2.31 $m_0$ | – | hBN (NEGF) |
| | | (H → K) | 1.45 $m_0$ | – | hBN (NEGF) |
| ↑ | Hole mass, $m_h$ | – | 0.50 $m_0$ | 8 | hBN_1 |
| | | (M → L) | 1.33 $m_0$ | 42 | hBN_2 |
| | | (M → L) | 1.48 $m_0$ | – | hBN (NEGF) |
| | | (H → K) | 4.38 $m_0$ | – | hBN (NEGF) |

In the leftmost column, the trends for suppressing tunnel leakage currents are highlighted, where ↑ stands for as high as possible and – for not specifiable in general. The tunnel masses are given as multiples of the electron mass ($m_0$).

In addition, we calculated the tunnel current as a function of EOT for a fixed electric gate field and a fixed applied voltage, corresponding to the two scaling laws for avoiding short-channel effects when decreasing device dimensions, Dennard scaling and constant voltage scaling. The tunnel currents as a function of the EOT are shown for a negative voltage of −0.7 V in Fig. 4d and for a positive voltage of 0.7 V in Fig. 4e, corresponding to a MOSFET with a p-type channel (pMOS) and an n-type channel (nMOS) of the 2020 technology node, respectively, where the supply voltage ($V_{DD}$) amounts to $V_{DD} = 0.7$ V (ref. [37]). In Fig. 4d, it can be seen that hBN is not suitable as a gate insulator in a pMOS for scaled devices with EOT < 1 nm, as the gate leakage current exceeds the low-power limit by more than one order of magnitude. If the leakage currents are above the low-power limit, the off-state currents and thus the power consumption of the device are too high for applications in consumer electronics. This observation, made for the current technology node, will be even worse for future nodes where the insulator thickness will be scaled down further. The conclusions are the same when comparing the tunnel current density as a function of EOT for constant electric gate fields of 2 MV cm$^{-1}$, as shown in Fig. 4b for negative voltages (pMOS) and in Fig. 4c for positive voltages (nMOS). There are substantial leakage currents even through defect-free hBN when negative voltages are applied due to the small band offset for holes of only about $\phi_h = 1.9$ eV and the comparatively small tunnel masses for holes in the M → L and H → K valleys of hBN.

These comparisons show that there is, in general, a shortage of insulators that provide sufficient leakage current blocking potential for continued down-scaling of devices and insulators. Among all insulators currently available, hBN is particularly ill-suited for being used as a scaled gate dielectric for pMOS devices and shows a performance slightly worse than most insulators for nMOS devices at operation voltages below 1.0 V; above this regime, the current through hBN dramatically increases.

One possible solution to this lack of scalable insulators would be to go to an operation regime of small supply voltages where only steep-slope devices can operate. In conventional MOSFET devices, the subthreshold swing cannot be smaller than the Boltzmann limit

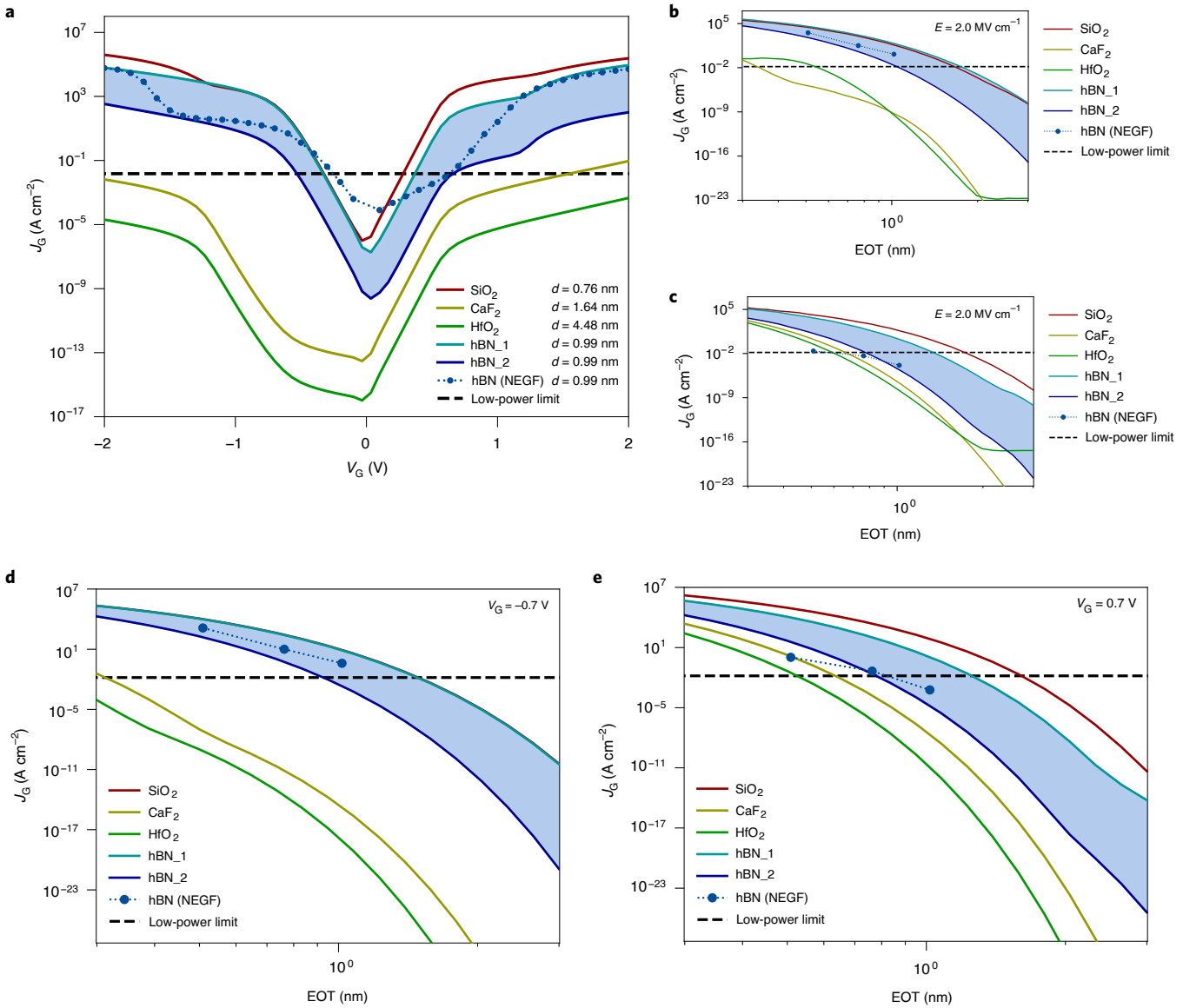


**Fig. 4 | Performance projection of the tunnel current through hBN in the defect-free case. a**, Currents at constant EOT. A comparison of the tunnel current densities through hBN and other dielectrics based on the Tsu–Esaki model for the metal–oxide–semiconductor stack of Au/dielectric/Si is shown for insulators with a thickness corresponding to an EOT of 0.76 nm. hBN_1 and hBN_2 stand for two different sets of material parameters used, as shown in Fig. 3a and explained in the section 'Performance projections for scaled hBN'. In addition, ab initio data are included as filled circles. The dotted lines connecting the circles are guides to the eye. **b**, Currents at constant gate field for a pMOS. The current density as a function of EOT is compared for different dielectrics at a fixed gate field and negative gate bias, $V_G < 0$ V, which illustrates Dennard scaling for a pMOS transistor. **c**, Currents at constant gate field for a nMOS. The current density as a function of EOT is compared at a fixed gate field and positive gate bias, $V_G > 0$ V. **d**, Currents at constant gate bias for a pMOS. The current density as a function of EOT is compared for different dielectrics at a constant negative gate bias, $V_G = -0.7$ V, which illustrates constant voltage scaling for a pMOS transistor. **e**, Currents at constant gate bias for a nMOS. The current density as a function of EOT is compared at a constant positive gate bias, $V_G = 0.7$ V.

of 60 mV dec$^{-1}$ at room temperature, determining a minimum operation voltage of about 0.7 V for sufficient on/off current ratios. To overcome this limit, the device operation principles have to be modified. Approaches that could achieve this goal exploit a constrained injection energy window for charge carriers such as tunnel FETs[47], a non-monotonic variation around the Fermi energy in the density of states as an energy filter[48], or an insulator that creates a negative capacitance of the gate stack, such as a ferroelectric, thereby amplifying the surface potential of the channel[49]. All these steep-slope devices allow for a supply voltage below 0.5 V where hBN also could serve as a gate insulator. In addition, hBN can also be used for applications where tunnelling through the layer is required as part of the device design, such as a tunnelling barrier in a tunnel FET based on a graphene/hBN heterostructure[50].

## Ideal gate insulators for scaled CMOS devices based on 2D materials

In general, a good gate insulator for FETs is characterized by four main properties. First, the insulator has to ensure a good gate control of the surface potential in the channel by the applied gate voltage,

**Table 2 | Comparison of the material parameters of potential gate insulators for 2D ultrascaled CMOS devices**

| Category | Material | Layered | VdW interface | Bandgap (eV) | Electron affinity (eV) | Dielectric constant ($\varepsilon_0$) | Electron mass ($m_0$) | Hole mass ($m_0$) |
|---|---|---|---|---|---|---|---|---|
| hBN | hBN_1 | Yes | Yes | 5.95 (ref. [63]) | 1.14 (ref. [65]) | 5.06 (ref. [40]) | 0.5 (ref. [8]) | 0.5 (ref. [8]) |
| | hBN_2 | Yes | Yes | 5.95 (ref. [63]) | 1.14 (ref. [65]) | 5.06 (ref. [40]) | 1.45 (ref. [42]) | 1.33 (ref. [42]) |
| 3D amorphous | $SiO_2$ | No | No | 9 (ref. [66]) | 0.9 (ref. [67]) | 3.9 (ref. [68]) | 0.42 (ref. [69]) | 0.33 (ref. [70]) |
| | $Al_2O_3$ | No | No | 6.5 (ref. [66]) | 1.7 (ref. [66]) | 9 (ref. [68]) | 0.45 (ref. [71]) | - |
| | $HfO_2$ | No | No | 5.5 (ref. [72]) | 1.75 (ref. [73]) | 23 (ref. [74]) | 0.18 (ref. [75]) | - |
| 2D layered | Mica | Yes | Yes | 7.85 (ref. [76]) | 3.26 (ref. [77]) | 8.1 (ref. [52]) | - | - |
| | $TiO_2$ | Yes | Yes | 3.8 (ref. [78]) | 3.72 (ref. [78]) | 60 (ref. [79]) | - | - |
| | GaS | Yes | Yes | 3 (ref. [54]) | 2.13 (ref. [54]) | 7.5 (ref. [80]) | 1.3 (ref. [80]) | - |
| Native oxides | $MoO_3$ | Yes | Yes | 3 (ref. [55]) | 6.6 (ref. [81]) | 35 (ref. [55]) | - | - |
| | $ZrO_x$ | No | Yes | 5.8 (ref. [68]) | 2.5 (ref. [67]) | 15 (ref. [82]) | - | - |
| | $Ta_2O_5$ | No | Yes | 4.4 (ref. [68]) | 3.3 (ref. [67]) | 15.5 (ref. [56]) | - | - |
| | $HfO_x$ | No | Yes | 5.5 (ref. [72]) | 1.75 (ref. [73]) | 23 (ref. [74]) | 0.18 (ref. [75]) | - |
| | $Bi_2SeO_5$ | Yes | Yes | 3.9 (ref. [57]) | 2.2 (ref. [57]) | 21 (ref. [57]) | - | - |
| Ionic fluorides | $CaF_2$ | No | Yes | 12.1 (ref. [83]) | 1.67 (ref. [84]) | 8.43 (ref. [85]) | 1 (ref. [84]) | 1 (ref. [84]) |
| Ideal | - | Yes | Yes | ≥12.5 | ≤0.8 | ~10 | ≥1.5 | ≥1.5 |

We include a fictional material with idealized properties for comparison. In the last two columns, '-' indicates that the respective tunnel mass is unknown to the best of our knowledge.

which is assured by a high permeability to electric fields ($\varepsilon > 8$). A good gate control is also the main driving force for the reduction of the insulator thickness $d$ in scaled devices, as in FETs with thick insulators and semiconductors the gate tends to lose control over a channel of reduced length, a phenomenon commonly termed short-channel effects. Second, the gate leakage current has to be small ($J < 10^{-2}$ A cm$^{-2}$ for $|V_G| \leq 0.7$ V)[37] to reduce the off-state current of the transistor and thereby the stand-by power consumption of the device. Third, the defect density at the interface and in the insulator should be as small as possible ($N < 10^{10}$ cm$^{-2}$) to maintain a high mobility in the semiconductor and to enhance device stability. A small defect density is also essential for achieving a subthreshold swing close to the 60 mV dec$^{-1}$ limit and for building stable devices with negligible hysteresis and long-term drifts[51]. Fourth, the dielectric stability should be as high as possible and assure a breakdown field $E_{BD}$ larger than 10 MV cm$^{-1}$.

An additional fifth requirement for the gate insulator could be formulated that is of special importance for devices based on 2D materials. The insulator should maintain a as high as possible room-temperature mobility in the semiconductor (ideally above 200 cm$^2$ V$^{-1}$ s$^{-1}$) by minimizing remote phonon scattering[23]. As discussed above, few-nanometre hBN is ideally suited for this purpose. However, hBN layers with a thickness of a few nanometres lead, together with the rather small dielectric constant of hBN, to a reduced gate control. The ideal value for the dielectric constant of the gate insulator in 2D material FETs is governed by a fundamental trade-off, as high values cause good gate control and small gate leakage currents, but small values, such as those in hBN, assure high mobilities.

In summary, there are five guidelines for an ideal gate insulator: excellent gate control, small gate leakage currents, low defect densities, high breakdown strength and an optimized mobility in the semiconductor. The question arises which of the materials that have been suggested for use as a gate stack for 2D FETs provides the best trade-off for all these requirements and how the different dielectrics perform in comparison to one another. Insulators that are being discussed include layered vdW crystals such as mica[52], $TiO_2$ (ref. [53]) or GaS (ref. [54]), crystalline ionic fluorides such as $CaF_2$ (ref. [46]), and native oxides such as $MoO_3$ (ref. [55]), $Ta_2O_5$ (ref. [56]), $Bi_2SeO_5$ (ref. [57]), $HfO_x$ (ref. [58]) or $ZrO_x$ (ref. [59]). In Table 2, the material parameters of these insulators are shown. One of the four requirements is evaluated by simulating the tunnel leakage currents with the same setup as introduced in the last section, only that the insulating layer is replaced by different materials all with an EOT of 0.76 nm. The leakage current densities are shown in Fig. 5b,c. While several materials exhibit lower leakage currents in ultrathin scaled layers than hBN, this comparison addresses only one out of the four requirements for a good gate insulator. Thus, many questions related to the best gate insulator for scaled 2D CMOS devices remain unknown and will have to be addressed in future studies.

## Conclusions

Hexagonal boron nitride is widely considered to be the most promising insulator for FETs based on 2D materials. In the past decade, considerable progress has been made in developing growth methods for hBN that are compatible with batch processing. However, the synthesis of single-crystalline, multilayer hBN with small impurity concentrations over large areas has not yet been achieved. In experimental studies based on exfoliated devices, and in theoretical calculations, it was shown that an interface of a 2D semiconductor and more than ten layers of hBN can provide charge carrier mobilities in the 2D semiconductor higher than for any other insulating layer used so far. This can be attributed to the small density of charged impurities that would act as Coulomb scattering centres and to the small dielectric constant of hBN, which reduces remote phonon scattering. These properties made the observation of novel physical phenomena possible[60] and make hBN an attractive material for application in analogue devices[61] and in nano- and optoelectronics[62].

Nevertheless, the excessive tunnel currents through ultrathin hBN are at present dominated by defect states in the hBN bandgap and defect clusters that form molecular bridges between hBN layers. A comprehensive picture of energetic trap levels and defect densities in hBN based on different synthesis methods, as well as a benchmark of the defect-dominated tunnel currents through layers of different qualities, is currently unavailable. Thus, to evaluate the theoretically attainable lower limit of the tunnel current through hBN, we assumed defect-free layers and calculated the tunnel currents using both a Tsu–Esaki and a DFT+NEGF based model.

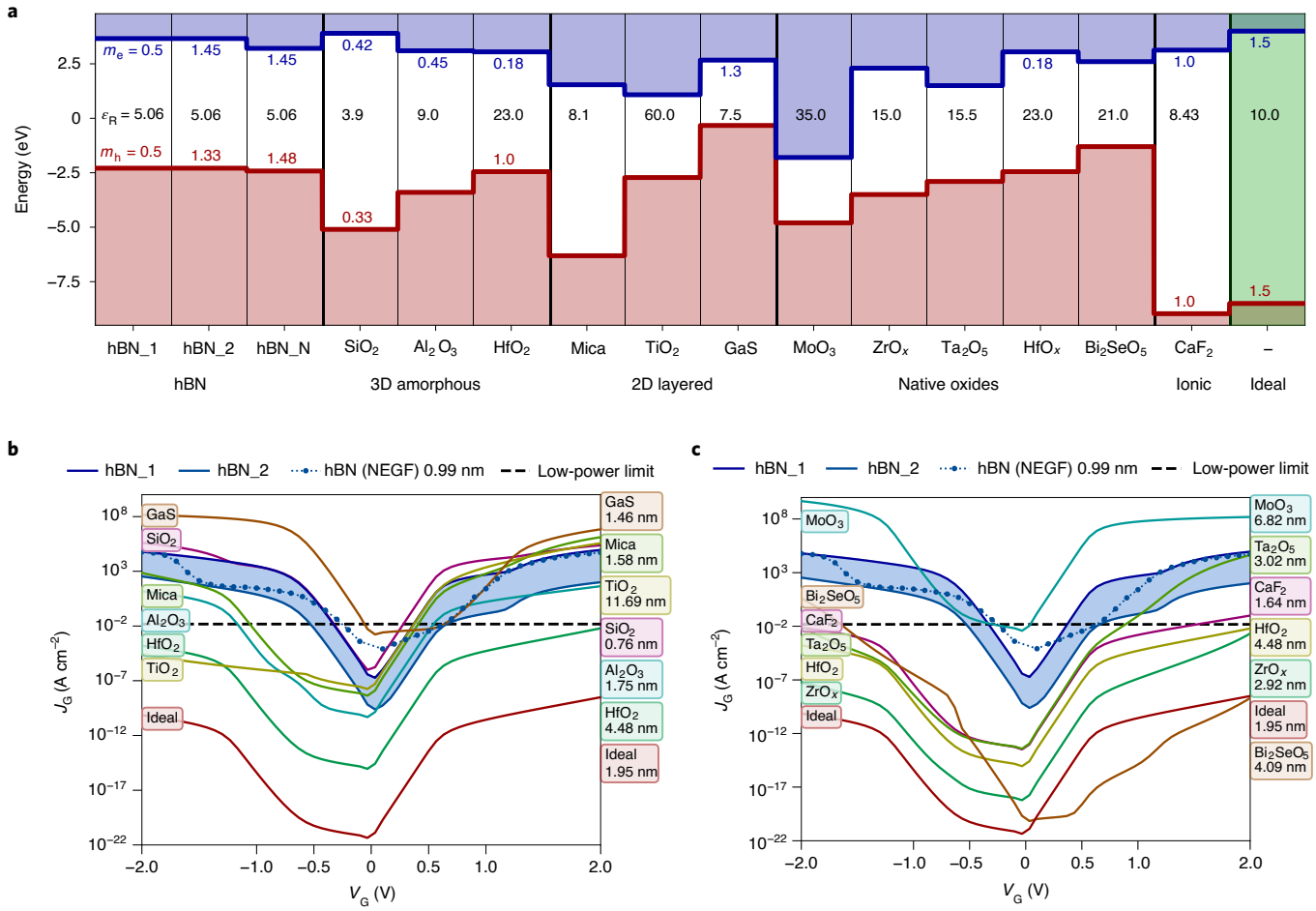


**Fig. 5 | Comparison of gate insulators for ultrascaled CMOS devices based on 2D materials. a**, Band diagram. The alignment of the bands is shown for insulators, which have been demonstrated as potential candidates for gate insulators in ultrascaled devices based on 2D materials. In addition, we include a fictional material with ideal properties for comparison, shaded in green. **b**, Currents at constant EOT for 3D oxides and layered insulators. The leakage currents as calculated with the Tsu–Esaki model are given for 3D amorphous oxide and 2D layered insulators at a constant thickness of EOT = 0.76 nm. If no tunnel masses were known, the free-electron mass was used. The filled circles indicate the results of ab initio calculations and the dotted line connecting the circles is a guide to the eye. **c**, Currents at constant EOT for native oxides and fluorides. The leakage currents are given for native oxides and ionic fluorides at a constant thickness of EOT = 0.76 nm.

Both methods are in good agreement and demonstrate that while for ultrascaled EOT the leakage current through hBN is slightly lower than through $SiO_2$, it is orders of magnitude higher than through $HfO_2$ or $CaF_2$ at the same EOT. In particular, for pMOS devices with an EOT below 1 nm, hBN is unsuitable as a gate insulator due to its small dielectric constant, its relatively high valence band edge and moderate effective tunnel masses.

On the basis of the calculated leakage currents, we have also shown that there is currently a lack of insulators compatible with 2D materials that would sufficiently block currents to allow for continued scaling, while maintaining the low power consumption required in consumer electronic devices. The ideal gate insulator would offer large bandgaps, high tunnel masses, a moderate dielectric constant, a crystalline structure and a high-quality vdW interface with 2D materials, thereby enabling excellent gate control, small gate leakage currents, low defect densities, a high breakdown strength and an optimized semiconductor mobility. We believe that an intensive search for suitable gate insulators or gate insulator stacks formed by combinations of several insulators, together with the adoption of a concept for steep-slope transistors, is required to deliver the performance boost expected by next-generation ultrascaled CMOS logic.

## Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

## Code availability

For the Tsu–Esaki/WKB calculations, we used the Comphy code, which is publicly available from https://comphy.eu/ (ref. [39]). For the full-band transport simulations, the matrices were calculated with the CP2K package, which is publicly available from https://www.cp2k.org/ (ref. [44]). These matrices were loaded into the quantum transport solver OMEN, as described at https://www.cp2k.org/howto:cp2k_omen (ref. [45]). Both code packages can be downloaded from https://github.com/cp2k/cp2k.

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## Author contributions

T.K. and T.G. conceived the ideas and led the study; T.K., Y.Y.I. and T.G. prepared the manuscript draft; F.D. and M. Luisier prepared and performed the DFT+NEGF calculations in frequent discussions with T.K. and T.G.; C.S. implemented the Tsu–Esaki model within the Comphy framework under the guidance of M.W.; T.K. and M.I.V. performed the Tsu–Esaki calculations in frequent discussions with Y.Y.I. and T.G.; S.W. fabricated devices under the supervision of T.M. using crystals provided by K.W. and T.T.; M. Lanza fabricated devices and provided advice for data analysis; T.K. performed the electrical characterization of the devices; and all authors reviewed and revised the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

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