Curvature Based Feature Detection for Hierarchical Grid Refinement in TCAD Topography Simulations

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***Abstract*—We present a feature detection method for selective grid refinement in hierarchical grids used in process technology computer-aided design topography simulations based on the curvature of the wafer surface. The proposed method enables high-accuracy simulations whilst significantly reducing the run-time, as the grid is only refined in regions with high curvatures. We evaluate our method by simulating selective epitaxial growth of silicon-germanium fins in narrow oxide trenches. The performance and accuracy of the simulation is assessed by comparing the results to experimental data showing good agreement.**

***Index Terms*—TCAD, topography simulation, level-set method, curvature, hierarchical grid, non-planar epitaxial growth**

I. Introduction

Many non-planar semiconductor device geometries (e.g., FinFETs) are fabricated by employing strongly anisotropic processing techniques [1]. During selective epitaxial growth (SEG), wafer topographies emerge, which are characterized by crystal facets and thus a combination of high-curvature and essentially flat regions materialize [2]. Local high resolutions of the underlying grids are thus required to accurately resolve high-curvature features and material interfaces during a process simulation, while keeping the overall run-time as low as possible to maximize applicability.

The level-set method is widely used for simulating fabrication processes of semiconductor devices [3], particularly in technology computer-aided design (TCAD) workflows. The wafer surface is described with the zero level-set of a continuous function ϕ which is referred to as the level-set function. The propagation of the wafer surface, i.e., its topographical evolution, is governed by the level-set equation

$$\frac{\partial \phi(x,t)}{\partial t} + V(x)|\nabla \phi(x,t)| = 0\,, \tag{1}$$

which incorporates the velocity field V, allowing to model the growth or etch rates during a process step [3]. The level-set equation is typically solved on a regular grid with resolution Δx using a finite difference scheme [4], [5].

The previously hinted need for local high grid resolutions can be efficiently realized by using hierarchical grids. Hierarchical grids have a *base* grid covering the entire simulation domain, which is complemented by *sub*-grids with higher resolutions, covering areas of interest (e.g., sharp ridges) [6]–[8]. Fig. 1 shows an illustration of a level-set function with three features (i.e., corners) which are resolved with higher spatial accuracy by finer sub-grids. In order to optimize simulation run time, these sub-grids need to be optimally configured and placed.

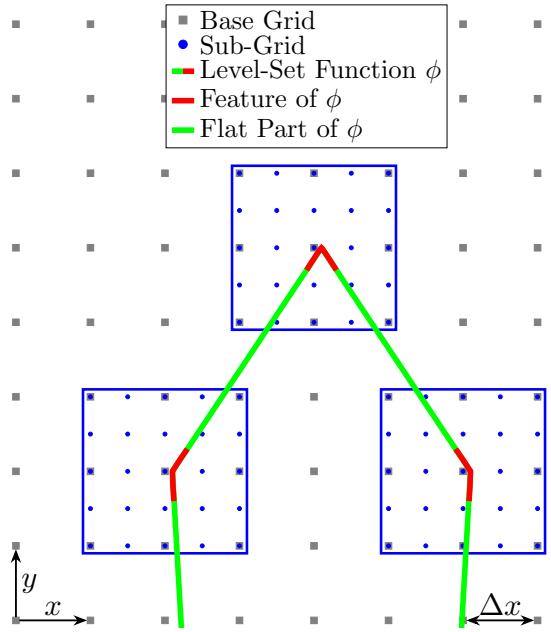

Fig. 1: Illustration of a level-set function ϕ (green/red line segments) with three features (i.e., corners; red line segments) on a hierarchical grid. The base grid has a resolution of Δx, the features of ϕ are covered by sub-grids with a two times higher resolution (blue boxes).

In this work, we introduce an efficient and automatic detection of level-set features for guiding the sub-grid generation mechanism of hierarchical grid-based process TCAD topography simulations. At the core of the feature detection is the calculation and evaluation of the wafer surface curvature, inspired by other curvature-based applications [9]–[11]. We assess our proposed method based on a representative and cutting-edge process simulation, i.e., selective epitaxy. To that end and to showcase integration into TCAD workflows, our feature detection method has been implemented into Silvaco's *Victory Process* simulator [12].

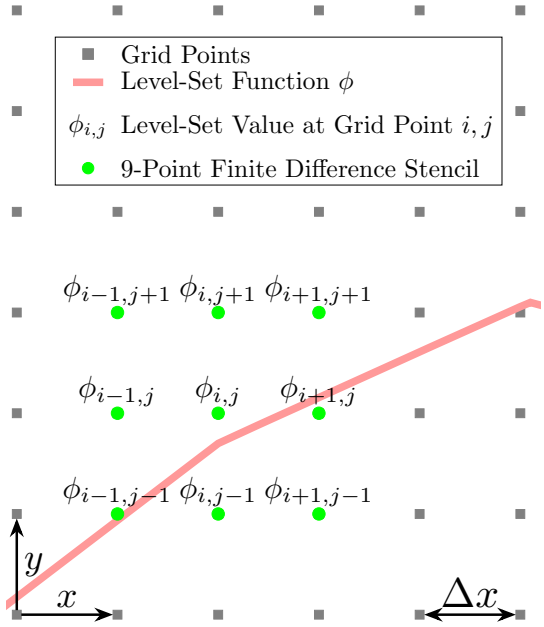

Fig. 2: Illustration of a level-set function and a 9-point stencil which is used to calculate the curvature of the surface at point $\phi_{i,j}$.

The thus augmented simulator is used to selectively grow silicon-germanium (SiGe) fins and to compare the results with recent experiments presented in [2]. Furthermore, we analyze the simulation performance and the accuracy of the results.

II. Method

The wafer topography during a fabrication step with pronounced anisotropy is typically characterized by regions of high and low curvature. In the level-set method the local curvature can be calculated directly from the level-set function ϕ

$$\kappa = \frac{\phi_y^2\phi_{xx} - 2\phi_x\phi_y\phi_{xy} + \phi_x^2\phi_{yy}}{|\nabla\phi|^3}, \tag{2}$$

where ϕ_i denotes the partial derivative of ϕ with respect to the coordinate $i \in \{x, y\}$. The partial derivatives are calculated using finite differences:

$$\phi_x \approx \frac{\phi_{i+1,j} - \phi_{i-1,j}}{2\Delta x},$$
$$\phi_{xx} \approx \frac{\phi_{i+1,j} - 2\phi_{i,j} + \phi_{i-1,j}}{\Delta x^2},$$
$$\phi_{xy} \approx \frac{\phi_{i+1,j+1} - \phi_{i-1,j+1} - \phi_{i+1,j-1} + \phi_{i-1,j-1}}{4\Delta x^2}.$$

The calculation of all required finite differences to determine the curvature κ requires a 9-point finite difference stencil around each point of the wafer surface (see Fig. 2).

The curvature is defined on each point of the wafer surface: The absolute value of the curvature $|\kappa|$ lies between 0 and $1/\Delta x$ since the maximal curvature a level-set function can describe is bound by the grid resolution [4]. Points with a curvature of $|\kappa| = 0$ describe a flat part of the wafer surface. In contrast, points with a larger value of $|\kappa|$ indicate a feature on the wafer surface. If the absolute curvature of a point exceeds $1/\Delta x$ it indicates that the resolution of the level-set function is not high enough to resolve this feature. Therefore, it is important that such grid points are flagged as features to improve the simulation quality.

Consequently, topography features are detected based on the curvature threshold parameter $0 < C < 1/\Delta x$, which is problem specific. If the curvature of a surface point is larger than C the point is flagged as a feature: The closer C is to 0 the more surface points will be detected as features. Furthermore, in this work, interfaces between stationary material regions are always considered features, which enables a well-resolved level-set description of SiGe material interfaces.

After the feature detection step the flagged surface points are grouped into rectangular *patches*. If patches overlap they are merged together until no more overlaps exist [13]. New sub-grids with, e.g., a four-times smaller Δx (facilitating locally increased resolutions) are then created according to these patches. The level-set values for the sub-grids are calculated with a hierarchical re-distancing step [14].

TABLE I: Simulation parameters employed for the SEG in trench arrays [2]. The number of deposition cycles P_i refers to the number of SEG cycles needed to achieve the topographies in Fig. 3.

Rates [nm/cycle]				Number of deposition cycles for profile P		
$R_{1\,0\,0}$	$R_{1\,1\,0}$	$R_{3\,1\,1}$	$R_{1\,1\,1}$	P_1	P_2	P_3
13	5	3.1	1.6	5	24	47

III. Results

The proposed feature detection method is evaluated by simulating the SEG process presented by Jang *et al.* [2]. There, in an initial dry etching step, $[\bar{1}\,1\,0]$-aligned SiO_2 trenches are formed. A cyclic SEG step follows, which leads to the formation of high-quality $\{3\,1\,1\}$ and $\{1\,1\,1\}$ crystal facets. Each individual cycle is taken as an artificial time step unit during the simulation. As previously indicated, this fabrication process has been simulated with Silvaco's *Victory Process* [12] augmented with the here proposed feature detection method: The method is employed during the SEG step, where we utilize a recently developed numerical stability-enabling level-set method for selective epitaxy [5].

The growth of the SiGe crystal is modeled with a crystal orientation-dependent velocity field V which is constructed from experimentally characterized growth rates [2], as given in Tab. I. The simulation results are in good agreement with the experiment (see Fig. 3).

Tab. II shows the utilized grid resolutions: The results shown in Fig. 3 are based on the *Multi-Grid* parameters, i.e., a base grid (Grid 1) complemented by one additional grid hierarchy level (Grid 2) offering a plethora of sub-grids with higher resolutions.

TABLE II: Grid parameters and run-times (Intel Xeon E5-2680v2) for the entire simulation.

Simulation	Grid 1 Res	Grid 2 Res	Run-Time
Coarse	0.002 µm	-	28 s
Fine	0.0005 µm	-	19 min 54 s
Multi-Grid	0.002 µm	0.0005 µm	13 min 38 s

Fig. 4 compares the results after the final simulation time step (47 SEG cycles) of the simulation using the parameters shown in Tab. II. Fig. 5 shows the error of the *Coarse* and *Multi-Grid* simulation results compared with the *Fine* simulation results: $|(x_1, x_2)| = \sqrt{x_1^2 + x_2^2}$ (L_2-norm). The error is measured from each point of the SiGe surface simulated with either *Coarse* or *Multi-Grid* parameters and its closest point (i.e., the point with the smallest L_2-norm) on the surface simulated with the *Fine* parameters (L_2-error).

The *Coarse* simulation results do not sufficiently match the results using the *Multi-Grid* parameters (Fig. 4), as evident from the mismatch of the peak positions of the SiGe crystal and the maximum of the L_2-error in Fig. 5. Additionally, the maximum L_2-error of *Multi-Grid* is smaller than the minimum L_2-error of *Coarse*, showing the anticipated increase in accuracy of the hierarchical approach.

As to be expected, there is a small L_2-error comparing the *Multi-Grid* results to the the *Fine* results, however, the simulation run with the *Fine* parameters has the disadvantage of significantly increased simulation run-times (see Tab. II). This is due to the higher resolution of the base grid, which unnecessarily increases the resolution of many irrelevant flat areas.The *Multi-Grid* result is based on the empirically chosen curvature threshold parameter $C = 0.9$ (and additionally considers the features at the interface of SiO_2 and SiGe, see Section II). To ensure the stability of the solution of (1) the maximal distance the zero level-set can propagate is bound by the Courant-Friedrichs-Lewy (CFL) condition [4]. The CFL condition is determined by the sub-grids with the highest resolution, so the feature detection and following re-distancing step (regridding) do not need to be executed in every time step of the simulation.

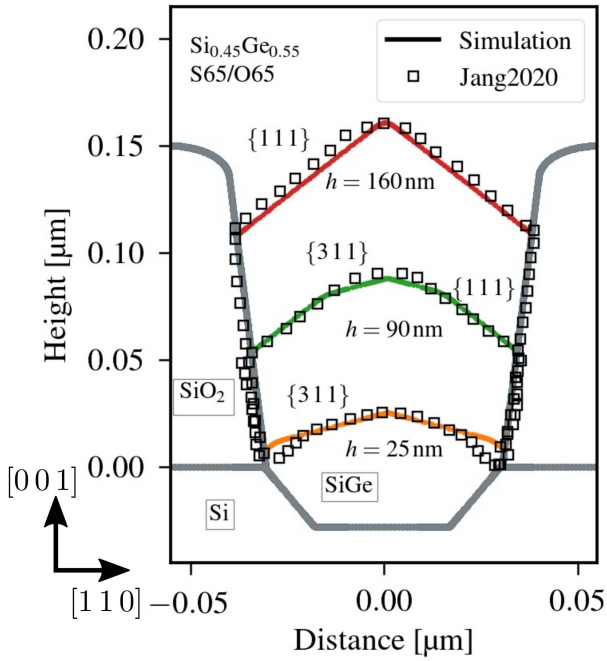

Fig. 3: Simulated surface of the SiGe crystal compared with the experimental results from [2] after 5 (orange), 24 (green), and 47 (red) SEG cycles. The simulation results show good agreement with the experimental data.

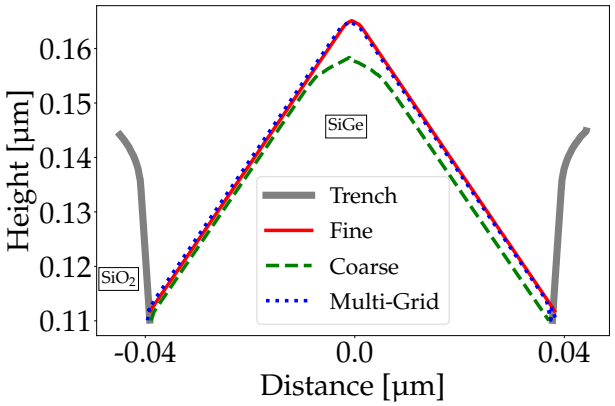

Fig. 4: Surface for the final simulation result of the SEG process after 47 SEG cycles using *Coarse*, *Fine*, and *Multi-Grid* resolutions. The error in the peak of the SiGe crystal using *Coarse* resolution is largest, since the grid resolution is not high enough to properly simulate the SEG process at this feature.

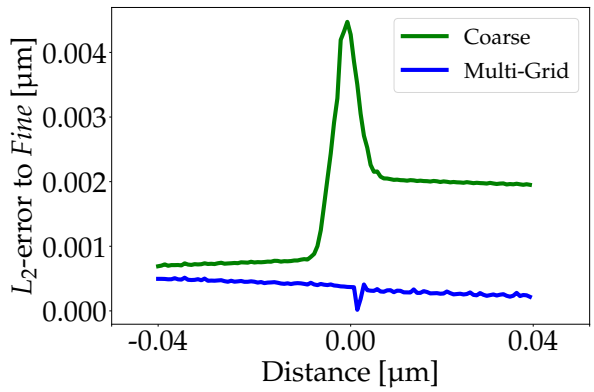

Fig. 5: Smallest L_2-error measured from the surface points of *Multi-Grid* and *Coarse* to the nearest surface point of *Fine*, in the final simulation result of the SEG process (see Fig. 4). The error of the simulation using the *Multi-Grid* parameters is negligible compared to the error when using the *Coarse* parameters.

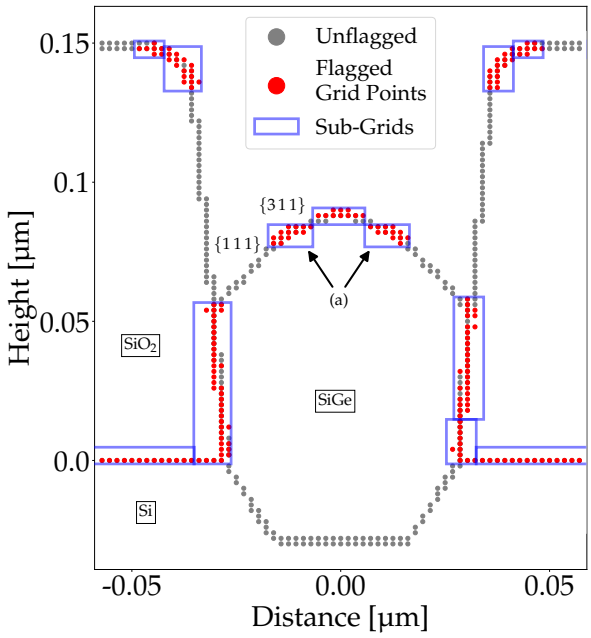

Fig. 6: Grid points near the level-set function for Grid 1 (i.e., base grid) of the *Multi-Grid* simulation after 24 SEG cycles. The flagged grid points (red) and generated sub-grids (blue boxes) for this time step are shown. (a) indicates sub-grids over fine features that develop during the SEG process.

The regridding step only has to be performed when the level-set values, within a sub-grid, required to calculate the finite difference scheme for the propagation of the zero level-set no longer lie within this sub-grid. Thus, to further improve the run-time of the simulation, we empirically determined that it is sufficient to perform the regridding every fourth time step. As discussed before (Fig. 3), *Multi-Grid* enables excellent agreement with the experimental data and a negligible L_2-error (Fig. 5) but with the advantage of a considerable reduced performance penalty as compared to the *Fine* case.

An example of the flagged grid points and thus generated sub-grids after 24 SEG cycles is shown in Fig. 6. This time point was chosen because here, the SEG process develops an additional geometrical feature between the $\{1\,1\,1\}$ and $\{3\,1\,1\}$ crystal facets, in addition to the peak of the crystal. Our feature detection method detects these fine features and sub-grids are placed accordingly, as indicated by (a) in Fig. 6.

IV. Summary

An efficient and automatic feature detection method for selective grid refinement in hierarchical grids of process TCAD topography simulations has been introduced. The method is based on a feature detection and successive grid refinement strategy which considers the curvature of the level-set function representing a wafer surface. The efficiency of this method has been demonstrated in a representative simulation of selectively grown epitaxial SiGe fins in oxide trenches. The feature detection, which has been used to optimally create the hierarchical grid, allows to use a low base grid resolution and only use sub-grids with higher resolution where crystal facets emerge during the SEG process and at material interfaces. By using our method the simulation run-time is considerably reduced compared to a simulation using a single high-resolution grid, while maintaining the accuracy of the simulation results.

Acknowledgment

The financial support by the Austrian Federal Ministry for Digital and Economic Affairs, the National Foundation for Research, Technology and Development, and the Christian Doppler Research Association is gratefully acknowledged.

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