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Performance Analysis of 4H-SiC Pseudo-D CMOS Inverter Circuits Employing Physical Charge Trapping Models

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Abstract. For the analysis of the characteristics and behavior of circuits prior to fabrication and to improve circuit performance, simulations using Spice tools are typically performed. Such tools rely on static compact models describing the behavior of the individual circuit components such as transistors. In reality, the behavior of the transistors changes over time due to aging, for instance, as a consequence of bias temperature instabilities (BTI). BTI is typically referred to as a drift of the threshold voltage of a transistor due to charge trapping at oxide and interface defects. To explain BTI, power-law-like mathematical expressions are often employed. However, using these simple formulas, the experimental data can only be replicated with limited accuracy. To evaluate the performance of logic inverter circuits made from 4H-SiC CMOS transistors with high precision, we use a physics-based defect model to describe the change of the device behavior from a defect-centric perspective. Our results indicate the limitations of using power-law-like formulas as they lead to an overly pessimistic estimation for circuit parameters.

Introduction

Transistors fabricated on 4H-SiC substrates exhibit superior properties, such as high blocking voltage capabilities, high thermal conductivity, etc., making them perfect candidates for high-power switching applications. In the recent past, lots of research has been conducted towards consistently improving the performance of SiC devices. Despite the numerous advantages over silicon devices, it has to be noted that the defect densities observed for various SiC technologies are considerably larger. Consequently, specific reliability issues, e.g., bias temperature instabilities (BTI) and gate leakage currents appear to be more prominent for SiC technologies [1], [2]. However, even though a more pronounced change in the device performance during operation can be observed than for Si transistors, not all reliability issues are a severe threat for circuits and applications. For instance, BTI, which is referred to as a drift of the threshold voltage of the transistor over time, can be mitigated in switching applications by using large gate overdrive voltages. It is evident that this is not optimal and leads to a slightly increased power consumption of the transistor during the switching cycles, which should be avoided.

The origin of BTI and the related drift of the threshold voltage lies in the charge trapping of defects located at the interface between the insulator and the SiC substrate [3]. Compared to Si technology, an approximately two orders of magnitude larger defect densitiy can be observed for SiC transistors. To improve the quality of the interface and oxide, post-oxidation annealing (POA) has been added to

the fabrication process. The impact of POA using different ambients has been studied recently. Using nitric oxide (NO) for POA, the electrical properties of the SiO_2/SiC could be significantly improved, enabling commercially available SiC MOS transistors [4]–[6]. However, there is still room for further improvement of the quality of the interface between the insulator and the SiC substrate to exploit the full potential of SiC technology.

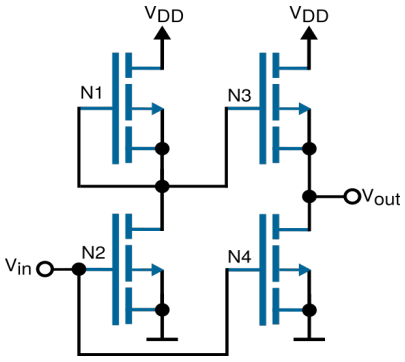

Fig. 1: The circuit diagram of the Pseudo-D CMOS inverter using 4H-SiC nMOS transistors is shown in [7]. The inverter consists of an input and an output stage. In our work, we analyze the inverter performance considering the degradation of the threshold voltage of the SiC transistors.

Based on the results from investigating reliability issues at the transistor level, one can evaluate their impact on the performance of circuits and applications. While computer simulations using physics-based TCAD software are primarily used to explain the characteristics of devices, circuit simulations are often carried out using Spice software. Spice simulations are vital for optimizing circuit performance and verifying designs operating stably under various operating conditions. In such simulations, compact models are typically used to mimic the behavior of the devices to evaluate the behavior of applications [8].

This work closely examines the pseudo-D CMOS inverter [7] shown in Fig. 1 using a commercially available 4H-SiC technology, i.e., C3M0065090J manufactured by Cree. For this, a combination of Spice simulations based on a compact model provided by Cree and our reliability tools, that are calibrated to explain BTI under DC and AC operating conditions for single transistors [9], are used. Afterward, the susceptibility of the signal propagation delay of the D-inverter circuit is evaluated.

Characterization of Reliability Issues of SiC Transistors

For the characterization of BTI, the measure-stress-measure (MSM) scheme is typically used [10], [11]. The MSM scheme consists of a series of stress and recovery phases where the stress and recovery times are continuously increased, as shown in Fig. 2. During the stress phase (red), the drain-source voltage is kept at 0V to prevent any hot-carrier degradation-related effects and ensure a homogenous carrier distribution at the interface along the channel. In the stress phase, where a high gate voltage is applied, many interface and oxide defects can become charged. Subsequently, recovery biases are used at the gate terminal (near the threshold voltage) and drain-source terminals (in the range of 0.1V), and the drain-source current is monitored. Even though constant biases are applied during the recovery phase, a drift of the drain-source current can be observed due to charge emission of defects that became charged during the prior stress phase. With increasing number of stress/recovery cycles, the observed drift becomes more and more prominent as longer stress and recovery times enable more defects to become charged. This is a consequence of the fact that discharging typically takes considerably longer than charging, meaning that even for an AC signal with a duty factor 50%, defects become charged with time. It has to be noted that this DC-MSM scheme is carried out using various gate stress biases and temperatures to evaluate the impact of charge trapping on the performance of the device as accurately as possible. For each measurement series, a fresh transistor has to be used as precise knowledge of the history of the drain and gate biases of the transistor are of utmost importance for the accuracy of the model parameters. Note that an initial IDVG characteristic is measured within a narrow gate bias range, and therefrom the time-zero V_{th} is extracted. The limited bias range is vital to avoid altering the charge state of the defects. This procedure allows accounting for device-to-device variability issues when the drift of V_{th} is extracted

from the MSM measurement. For discussion of the experimental data, the measured drift of the drain-source current is often represented as a change in the threshold voltage ΔV_{th}. This can be achieved by converting the current to an equivalent gate voltage using an initially measured IDVG characteristic [12], [13].
The most application-relevant gate bias patterns for SiC transistors are AC signals. To monitor the drift of the threshold voltage under AC bias conditions, a switching gate voltage is applied and interrupted at well-defined time points to measure and extract the current value of the device threshold voltage [14].

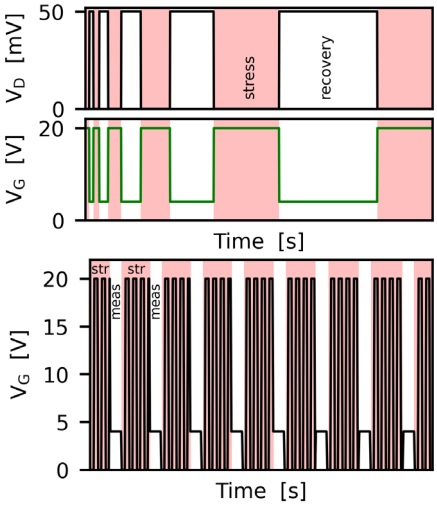

Fig. 2: Two typical gate voltage patterns are used to extract the behavior of SiC transistors under the most application-relevant operating conditions. (top) Characteristic for the DC-MSM scheme is a constant stress bias applied before the recovery phase is recorded [15]. *(bottom) For the selected AC measurement scheme, the AC signal is interrupted precisely at the end of the high-phase to consistently measure the drift of the threshold voltage V_{th}* [9], [14].

The experimental results for DC and AC-MSM measurements from a commercial transistors technology are shown in Fig. 3. As can be seen, a drift of the threshold voltage of more than 1V/0.6V for the DC/AC-MSM case can be observed. The solid lines are extracted from our simulations using our defect model that accurately replicates the experimental data and will be discussed in the next section in further detail.

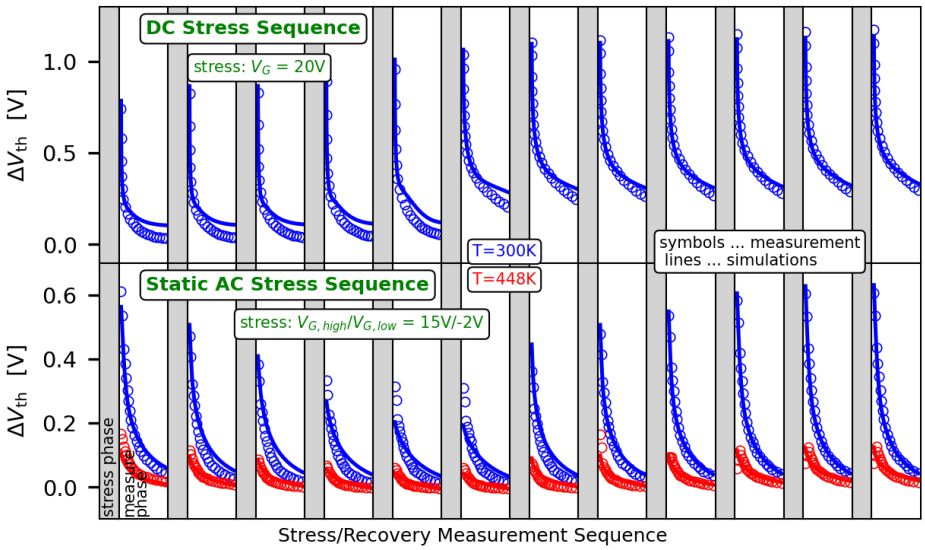

Fig. 3: The transient behavior of a SiC transistor obtained from applying the schemes of Fig. 2. (top) DC stress/recovery. (bottom) AC stress experiments. As can be seen for both cases, the drift characteristics of the V_{th} (symbols) of the devices can be accurately explained by our physical model (lines). The data has been measured at different biases and temperatures to calibrate the models for a large variety of operating conditions [9]. *It has to be noted that all trends can be consistently explained by our model using the same trap parameters, enabling fully accurate analysis of the impact of V_{th} degradation on the performance of circuits.*

Modeling of Bias Temperature Instabilities

To provide an explanation for the experimental data, simple power-law or exponential-like functions are often used [17]–[19] as they offer a fast and straightforward method to quantify the results with a reduced parameter set. However, such empirical formulations must be treated with care as they do not provide a physics-founded description of the underlying mechanisms. For instance, a serious limitation of power-law expressions is that the saturation of the drift of the threshold voltage with increasing stress time can not be explained, see Fig. 4. As a consequence, the extrapolations may not

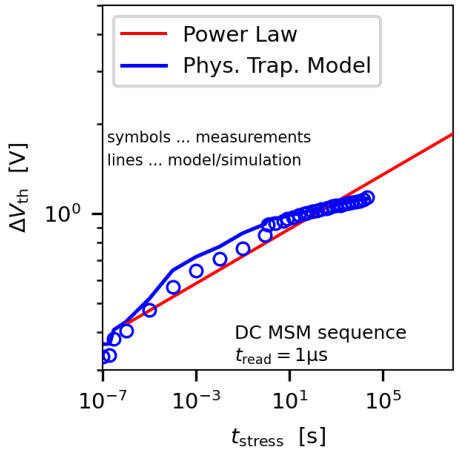

Fig. 4: Our physical charge trapping model [16] *and a power-law, i.e., $\Delta V_{th} = At^n$, is applied to explain the experimental data. As can be seen, the power-law function does not account for saturation of ΔV_{th}, which is one of the weaknesses of this approach. Ultimately, this leads to a considerable overestimation of the measured V_{th} degradation. In contrast, the physical defect model can be calibrated to replicate the measurement results. (The dashed line serves as guide for the eye).*

be accurate. As has been mentioned, a more accurate description of BTI can be achieved when the non-radiative multi phonon (NMP) model is considered [20]. In the recent past, it has been demonstrated that using this model, the drift of the threshold voltage can be explained properly employing various large-area and scaled transistor technologies [16], [21]. The two-state defect model, see Fig. 5, is available via our reliability simulator Comphy [22]. Quite recently, an effective

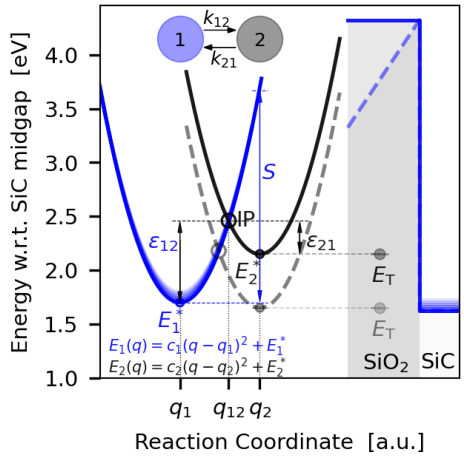

Fig. 5: The physical defect model which we employ to calculate the charge trapping dynamics of the defects calculates the charge state of a defect considering a two-state system. State 1 accounts for the carrier reservoir, i.e., the conduction band edge, and state 2 describes the defect. The transitions between the two states are calculated using potential energy sufaces. Note that this model has to be solved for a large ensemble of oxide defects to mimic the experimentally observed V_{th} degradation [15].

single defect decomposition algorithm has been built around Comphy [23], enabling the efficient computational extraction of a defect distribution to explain both the DC and AC data sets from Fig. 3. As the name suggests, the model consists of two states where state 1 refers to the situation where the charge carrier resides at the channel, i.e., the conduction band edge, and the defect is neutral. If the carrier dwells in state 2 the defect is considered to be charged. For a charge transfer to take place, the carrier has to overcome the energetic barrier determined by the intersection point of the two parabolas describing the energy of the states. In the case of $E_1 < E_2$, the barrier $\varepsilon_{12} > \varepsilon_{21}$ and thus the defect remains neutral. However, when a gate bi as is applied, the energetic position of E_2 becomes lowered with respect to E_1 and thus $\varepsilon_{12} < \varepsilon_{21}$. In this case, the defect can become charged. Next to the trap level of the defect, which is given by E_2, the trapping kinetics is also determined by the relaxation energy S and the curvature ratio of the parabolas $R = c_1/c_2$, which is typically considered as $R = 1$. The

detailed defect parameters of the interface and oxide traps used to explain the experimental data are extracted and discussed in [9]. The impact of charge trapping on the inverter circuit is analyzed next with the defect parameters and the calibrated Comphy simulation framework at hand.

Impact of Bias Temperature Instabilities on the Performance of Inverter Circuits

To quantify the impact of BTI on the behavior of a pseudo-D CMOS inverter circuit, the signal propagation delay between the input and the output voltage is analyzed, see Fig. 6. The open-source tool ngspice is used for the circuit simulations, and the propagation delay is extracted in a post-

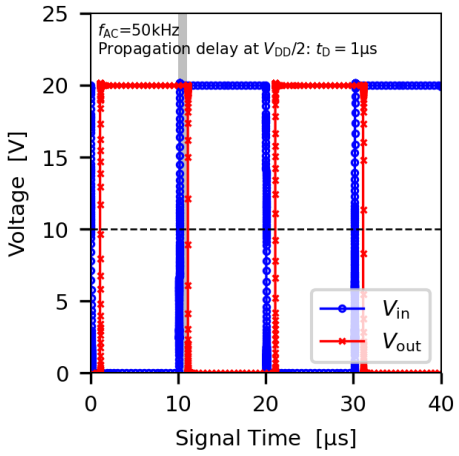

Fig. 6: The signal propagation delay of the inverter circuit is extracted as the time difference between the output and input voltage at $V_{DD}/2$. For the evaluation of this delay under application-relevant operating conditions, an AC signal frequency of 50kHz is considered.

processing step at $V_{DD}/2$. In order to consider the drift of the threshold voltage during circuit operation, the Spice simulations are combined with our reliability models. For the circuit simulations, a threshold voltage of $V_{th}+\Delta V_{th}$ is considered for each of the transistors, where ΔV_{th} is calculated employing Comphy for each transistor individually, depending on the applied bias history. Although this approach is not overly computational efficient, it accurately calculates the degradation of the circuit signal propagation delay due to BTI. Note that the compact transistor model used for the simulations is provided by the device manufacturer [24].
In Fig. 7, the results of our simulations are shown. It becomes evident that when physical defect

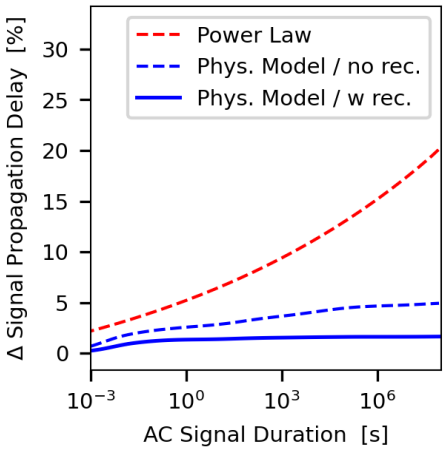

Fig. 7: The comparison of the simulated signal propagation delay shows a considerable deviation between simple models and physical defect models. The simple models predict an overly pessimistic signal propagation delay. Note that the low phases of the AC signal cause recovery of the devices, which has to be considered in the simulations. Otherwise, the signal propagation delay will be significantly overestimated by the simulations.

models are used, a considerably lower degradation of the signal propagation delay can be observed. Furthermore, a severe limitation of frequently applied approaches is that device recovery during the low bias phase under AC operating conditions is omitted [25]. This leads to overly pessimistic estimates for the signal propagation delay of the investigated circuit. We also evaluate the degradation of each transistor individually in Fig. 8. One can see that N2 and N4 show a similar impact on the signal propagation delay while the circuit is less sensitive to a V_{th} drift of N1 and N3.

A final important aspect we observed in our simulations is that an overestimation of ΔV_{th} may lead to a misbalance of the impedances of the series connection of N3 and N4. In summary, the shown lack in prediction accuracy, which simple empirical models can

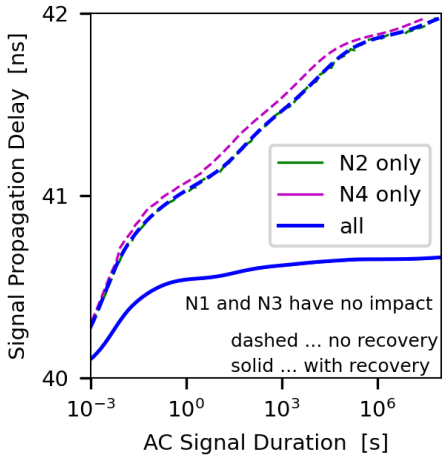

Fig. 8: An analysis of the impact of the transistors N1 to N4 on the signal propagation delay of the inverter circuit is shown. While N1 and N3 do not impact the signal propagation delay, a degradation of N2 and N4 affects the signal propagation delay similarly.

introduce, is a clear indicator of the need for precise simulation models to avoid potential circuitry overhead.

Conclusions

Circuit simulations using Spice software are vital for optimizing the performance of circuits and for verifying that designs can operate in a stable manner under various operating conditions. In our work, we analyze a pseudo-D CMOS inverter circuit made employing 4H-SiC transistors. We combine circuit simulations with physics-based defect simulations to account for the impact of charge trapping on the performance of SiC transistors and examine the signal propagation delay of the inverter. Our results indicate that the performance degradation of the transistors leads to an increase in circuit delay. Also, one can see that empirical models often lead to a significant overestimation of the performance loss of the inverter circuit. Finally, it has to be noted that considering the device recovery during low phases of AC input signals is vital as otherwise too pessimistic values for the signal propagation delay are obtained from theoretical investigations.

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