DISSERTATION

Investigation of the Impact of Oxide and Interface Defects on the Performance of 4H-SiC MOSFETs

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Abstract

The reliability issues caused by oxide and interface defects of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) play a major role in the robustness of device functionality. 4H silicon carbide (4H-SiC) MOSFETs are a serious competitor to silicon (Si) power devices because of their ability to operate at higher temperatures, higher power densities, higher frequencies, reduced dimensions, and higher voltages than Si-based MOSFETs. Even with well-known manufacturing processes, much research has focused on the reliability concerns associated with the SiC/SiO_2 interface and oxide quality, attributed to the higher defect density that can be observed when data is compared to that of the SiO_2/Si interface. A new direction for future generations of 4H-SiC power MOSFETs is related to trench technologies, which offer increased channel mobility, resulting in reduced ON resistance owing to their unique interface properties. The differences between planar and trench 4H-SiC MOSFETs are evident in the hysteresis width observed in the $I_d - V_{gs}$ and $C - V$ curves, as well as in the Bias Temperature Instability (BTI) and Gate Switching Instability (GSI), which arise from the different kinds of defects and their associated charge trapping kinetics affected by the applied voltage bias, ambient temperature, sweep duration, and frequency.

Despite the evident advancements in recent years regarding interface enhancement via post-oxidation annealing in various gases, as well as the improvement of channel carrier mobility, threshold voltage stability, and reduction of hysteresis width, the precise origin and electrical properties of these traps continue to be a contentious issue, particularly concerning the different properties of planar and trench MOSFETs interfaces and the corresponding distinct gas recipes for interface enhancement. The various trap types at the SiC/SiO_2 interface have been shown to consist of acceptor-like or donor-like types, which can be categorized as "slow" border traps which located deep in the insulator or "fast" interface traps in relation to their charge-trapping kinetics, exhibiting complex cumulative instability effects. Thus, the fundamental charge transfer reactions for the "slow" traps can be characterized by the Non-Radiative Multi-Phonon (NMP) model. To understand the "fast" traps behavior, a physical-based modeling approach based on Shockley-Read-Hall (SRH) theory was used in this research. By using TCAD simulations and comparing them with the measurement results, a possible trap candidate for anomalously elevated hysteresis width at higher temperatures was investigated. It was postulated that the increase in the hysteresis width at elevated temperatures may be attributed to amphoteric P_b or P_{bC} trap centers with varying NMP parameters.

Finally, the hysteresis width characteristics across a broad temperature range were examined in both the $I_d - V_{gs}$ and $C - V$ curves, along with the BTI and subthreshold

voltage slopes for the lateral MOSFETs. The hysteresis width of the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves across multiple cycles and $C - V$ curves for the trench devices were simulated. The results presented in this study will contribute to improving simulation frameworks to explain the intricate behavior of charge trapping phenomena under various operating conditions.

Kurzfassung

Die Zuverlässigkeit von Metalloxid-Halbleiter-Feldeffekttransistoren (MOSFETs) stellt einen zentralen Aspekt für die Robustheit und Langzeitsatbilität in Applikationen dar. Insbesondere 4H-Siliziumkarbid (4H-SiC)-MOSFETs ersetzen zunehmend konventionelle Silizium-(Si)-Leistungshalbleiter, da sie in der Lage sind, unter höheren Temperaturen, mit höheren Leistungsdichten, höheren Schaltfrequenzen, kleineren Abmessungen sowie bei erhöhten Betriebsspannungen gegenüber Si-basierten MOSFETs zu arbeiten.

Trotz etablierter Fertigungsprozesse konzentriert sich ein erheblicher Teil der aktuellen Forschung weiterhin auf die Zuverlässigkeit dieser Bauelemente, insbesondere im Hinblick auf die SiC/SiO_2-Grenzfläche und die Qualität der Gate-Oxide. Die Ursache hierfür liegt in der signifikant höheren Defektdichte im Vergleich zur etablierten Si/SiO_2-Grenzfläche , welche aus elektrischen Messungen an SiC Transistoren hervorgeht. Konventionelle planare MOSFET-Strukturen weisen diesbezüg-lich Nachteile auf und bleiben hinsichtlich ihrer Leistungsfähigkeit hinter den neuesten kommerziell verfügbaren 4H-SiC-Leistungs-MOSFETs zurück.

Ein innovativer Ansatz für zukünftige Generationen von 4H-SiC-MOSFETs stellt die Implementierung von Grabenstrukturen (Trench-Technologien) dar, welche durch eine erhöhte Kanalflächendichte eine Reduktion des Einschaltwiderstands ermöglichen. Diese Vorteile ergeben sich maßgeblich aus den besonderen Eigenschaften der Grenzfläche.

Die Unterschiede zwischen planaren und trench-basierten 4H-SiC-MOSFETs manifestieren sich deutlich in der beobachteten Hysteresebreite sowohl in den I_d-V_{gs}- als auch den C-V-Kennlinien sowie in der Ausprägung der Bias Temperature Instability (BTI) und der Gate Switching Instability (GSI). Diese Phänomene sind das Resultat unterschiedlicher Systeme und Dynamiken des Ladungsfangs an Defekten im Transistor, die durch die angelegte Vorspannung, die Umgebungstemperatur, die Schwingungsdauer und die Anregungsfrequenz beeinflusst werden.

Auch wenn in den letzten Jahren erhebliche Fortschritte erzielt wurden – insbesondere durch Nachoxidationsprozesse unter unterschiedlichen Gasatmosphären, die Grenzflächeneigenschaften verbessern, die Kanalträgermobilität erhöhen, die Schwellenspannung stabilisieren und die Hysteresebreite reduzieren – sind die genauen physikalischen Eigenschaften der beteiligten Defekte weiterhin Gegenstand intensiver Forschungsarbeiten. Dies gilt insbesondere im Kontext der strukturellen und prozesstechnologischen Unterschiede zwischen planaren und trench-basierten Bauelementarchitekturen sowie der Verwendung unterschiedlicher Gasrezepte zur Grenzfläch-enpassivierung.

Die Defekte, welche sich an der SiC/SiO_2-Grenzfläche befinden, lassen sich in akzeptor- und donatorartige Zustände unterteilen, die entsprechend ihrer Ladungsdy-

namik als "schnell" bzw. "langsam" klassifiziert werden. Diese Zustände können komplexe, kumulative Instabilitätseffekte hervorrufen. Die fundamentalen Ladungstransferprozesse bei "langsamen" Trap-Centers können dabei durch das nicht-strahlende Multiphononenmodell (Non-Radiative Multi-Phonon, NMP) beschrieben werden. Zur Modellierung des Verhaltens der "schnellen" Trap wurde im Rahmen dieser Arbeit ein physikalisch fundierter Modellierungsansatz auf Basis der Shockley-Read-Hall-(SRH) Theorie hera-ngezogen.

Mittels Computers Simulationen in Kombination mit experimentellen Messergebnissen wurde ein möglicher Kandidat für eine Defekklasse identifiziert, die für die, bei erhöhten Temperaturen beobachtete, anomale Verbreiterung der Hysteresekennlinien verantwortlich sein könnten. Es ist davon auszugehen, dass nicht ausschließlich mobile Ionen, sondern insbesondere amphotere P_{b}- bzw. P_{bC}-Zentren mit variierenden NMP-Parametern diese Effekte verursachen könnten.

Abschließend wurden die Hysteresebreiten in einem weiten Temperaturbereich sowohl für die $I_{\mathrm{d}} - V_{\mathrm{gs}}$ als auch die $C - V$ Kennlinien systematisch untersucht. Dazu wurden BTI Phänomene und die Subthreshold-Spannungsneigung für laterale MOSFET-Strukturen analysiert. Ergänzend zu der Untersuchung wurden die Hysteresebreiten der $I_{\mathrm{d}} - V_{\mathrm{gs}}$ Kurven und die Kennlinienverläufe der $C - V$-Messungen bei Trechn-Bauelementen simulativ erfasst. Die Auswertung offenbarte ein charakteristisches Trap-System, das sich durch spezifische Parameter beschreiben lässt, und welches die experimentell ermitelten Messergenisse gut widerspiegelt. Die gewonnenen Ergebnisse unterstützen zukünftige Arbeiten dabei Simulationsmodelle noch besser zu kalibrieren und so das Verhalten der SiC Transistoren noch besser beschreiben zu können.

List of Abbreviations

4H-SiC	4H-Silicon Carbide
BTI	Bias Temperature Instability
CCDLTS	Constant-Capacitance Deep-Level Transient Spectroscopy
CET	Capture Emission Time
DFT	Density Functional Theory
EELS	Electron Energy Loss Spectroscopy
eMSM	extended Measure Stress Measure
GSI	Gate Switching Instability
GSI	Gate Switching Instability
HCD	Hot Carrier Degradation
HTGS	High-Temperature Gate-bias Stress
IGBT	Insulated Gate Bipolar Transistor
MOS	Metal Oxide Semiconductor
MOSCAP	Metal Oxide Semiconductor Capacitor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MSM	Measure Stress Measure
NBTI	Negative Bias Temperature Instability
NMP	Non-Radiative Multi-Phonon
PBTI	Positive Bias Temperature Instability
POA	Post Oxidation Annealing
RTN	Random Telegraph Noise
SiC	Silicon Carbide
SIMS	Secondary Ion Mass Spectroscopy
SiPM	Silicon Photomultiplier
SRH	Shockley-Read-Hall
STEM	Scanning Transmission Electron Microscopy
TCAD	Technology Computer-Aided Design
TDDB	Time-Dependent Dielectric Breakdown
TDDS	Time-Dependent Defect Spectroscopy

1. Introduction

In power electronics, an electrical switch is typically implemented using a metal-oxide semiconductor field-effect transistor (MOSFET) or an Insulated Gate Bipolar Transistor (IGBT). With considerable enhancements in the conversion efficiency realized in devices utilizing silicon substrates, inherent limitations in minimizing static and dynamic switching losses owing to the material characteristics of silicon must be resolved. Wide-bandgap semiconductors, such as silicon carbide (4H-SiC) and gallium nitride (GaN), provide enhanced features for power electronics to enhance the conversion efficiency, have been included as substrate materials in commercially accessible devices, and are serious contenders for replacing Si-based power switches in the near future [1], [2]. Commercial planar and trench 4H-SiC MOSFETs are promising candidates for use in power electronics. However, thermally grown silicon dioxide (SiO_2) on SiC surfaces remains a major research topic owing to the high defect density at the SiO_2/SiC interface compared with that at the SiO_2/Si interface. This became more pronounced because the devices used different 4H-SiC faces, which influenced the reliability of the electrically active border and interface traps on the reliability of circuit operation. Investigating these defects using $I_\mathrm{d} - V_\mathrm{gs}$ with $C - V$ curve toughener and accurate modeling of the trap kinetics allows us to better understand the origin of the hysteresis and other instability phenomena and reduce the density of interface states using special technology steps such as post-oxidation annealing.

1.1. Silicon Carbide Material Properties

In the late 1980s, it became evident that silicon power-switching devices exceeded their theoretical limits, which could be substantially extended by manufacturing power devices using materials with higher breakdown electric fields such as silicon carbide (4H-SiC) or semiconducting diamond [3]. For vertically oriented devices, the theoretical minimum value of the specific resistance (in $\Omega\,\mathrm{cm}^2$) is

$$R_{SP} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_N \varepsilon_S E_C^3} = \frac{3.375 V_B^2}{\mu_N \varepsilon_S E_C^3} \tag{1.1}$$

where μ_N is the electron mobility perpendicular to the surface, ε_S is the permittivity of the semiconductor, E_C is the critical field for the avalanche breakdown perpendicular to the surface, and V_B is the designed blocking voltage in the drift region. where $(\mu_N \varepsilon_S E_C)$ is the Baliga figure of merit (BFOM) [4].

The critical field in SiC is almost an order of magnitude higher than that in Si, as shown in Table 1.1.

Table 1.1: Semiconductor material parameters. [5], [6]

Material	4H-SiC	GaN	β-Ga_2O_3	Diamond	Si
E_g (eV)	3.26	3.4	4.7-4.9	5.5	1.1
ε_S	9.7	9.0	10	5.5	13.1
E_C ($MV\,cm^{-1}$)	3.0	3.3	8	10	0.3
μ_N ($cm^2\,V^{-1}\,s^{-1}$)	900	900	300	1900	1438
Relative BFOM	517	854	3371	22937	1
λ ($W\,cm^{-1}\,K^{-1}$)	4.9	1.3	0.24	22	1.5
v_g ($10^7 cm\,s^{-1}$)	2.0	2.5	2	1 (holes)	1.0

In addition, the thermal conductivity λ of 4H-SiC and saturation carrier velocity v_g are higher than those of Si.

1.2. 4H-SiC/SiO_2 Interface Poperies. Crystal Faces

The first planar and lateral 4H-SiC MOSCAPs and MOSFETs had (0001)-Si faces. Nevertheless, alternative face options are available, such as the nonpolar $(11\bar{2}0)$ a-face (which is mostly used in trench devices), $(1\bar{1}00)$ m-face, and polar $(000\bar{1})$ C-face (see Fig. 1.1). The $(03\bar{3}8)$ in 4H-SiC is the face was tilted by 54.7° toward $<013\bar{3}0>$ from the (0001) face [7]. The atomic structure of a surface differs from face to face. Si atoms determine the Si-face of SiC, whereas C atoms terminate the C-face; the non-polar faces have equal amounts of Si and C atoms. The various surface structures exhibit unique characteristics. For example, the a-face has a higher channel mobility than the Si-face and alternative faces even after post-oxidation annealing. This corresponds to the different defect densities at the 4H-SiC/SiO_2 interface. Alternatively, there are different oxidation rates at 1150 °C. In addition, the a-face and C-face have the highest oxidation rates compared to the Si-face, which has the lowest rate.

A specialized POA is required to enhance the interface quality owing to the different defect densities across different faces. For Si-face devices, wet oxidation and/or H_2 annealing may enhance channel mobility.

The a-face channel mobility was improved using the hydrogen POA process or wet annealing. NO annealing of the $(03\bar{3}\bar{8})$ face also enhanced the channel mobility. The preferred POA is the nitrogen NO base method for creating a-face and m-face devices. Dry oxidation and/or NO annealing are employed for the Si-face and non-polar faces; however, they are less effective on the C-face in terms of reducing the interface trap density and enhancing mobility. In conclusion, devices with nonpolar faces exhibit a higher threshold voltage than those with Si faces, which is particularly advantageous for power-device applications [5], [8].

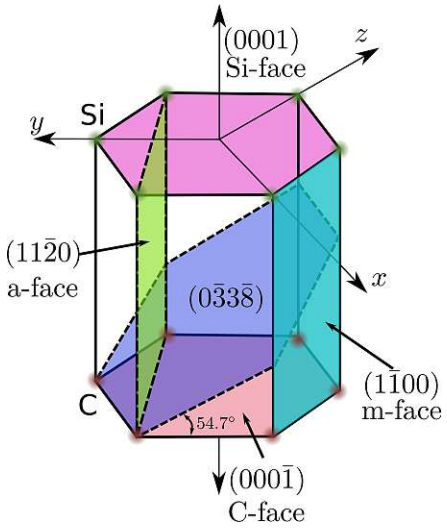


Figure 1.1.: Crystal faces in 4H-SiC. The Si-face ends with Si atoms (large green balls), whereas the C-face ends with C atoms (small black balls). Non-polar faces, such as the a-face and m-face, possess an equal number of silicon and carbon atoms. Adapted from [5].

1.3. 4H-SiC MOSFET and MOSCAP Structures

Depending on the design, two primary crystal orientations where the oxide is grounded are used: the Si-face for the lateral and DMOSFETs and the a-face for the asymmetric trench 4H-SiC nMOSFET, as illustrated in Fig. 1.2. In our investigation, a lateral 4H-SiC nMOSFETs with an n^+ poly gate is used. An oxide thickness of 50 nm and a gate length of 7.5 µm were assumed, see Fig. 1.2, a. This oxide layer was formed on a Si-face substrate via chemical vapor deposition. Next, a commercial discrete asymmetric trench 4H-SiC nMOSFET, and assumed that the intended oxide thickness was 60 nm were used. A trench was fabricated using plasma-etched surfaces. The n-channel a-face MOSFETs received SiO_2 deposited via chemical vapor deposition with subsequent post-oxidation annealing in NO ambient, see Fig. 1.2, c [1], [2], [9], [10]. In this study, only test lateral MOSFETs were examined because the trap system is identical to that of DMOSFETs (Fig. 1.2, b), which have the same crystal face as the lateral devices (Fig. 1.2, a).

It is assumed that the fast interface traps are located directly at the SiC/SiO_2 interface, whereas the slow border traps are positioned at a depth of 1 nm from the interface. Only traps placed directly above the channel were involved in the trapping kinetics. This behavior depends on its parameters, which can either capture or emit electrons or holes, leading to distortions in the measured curves (see Fig. 1.2).

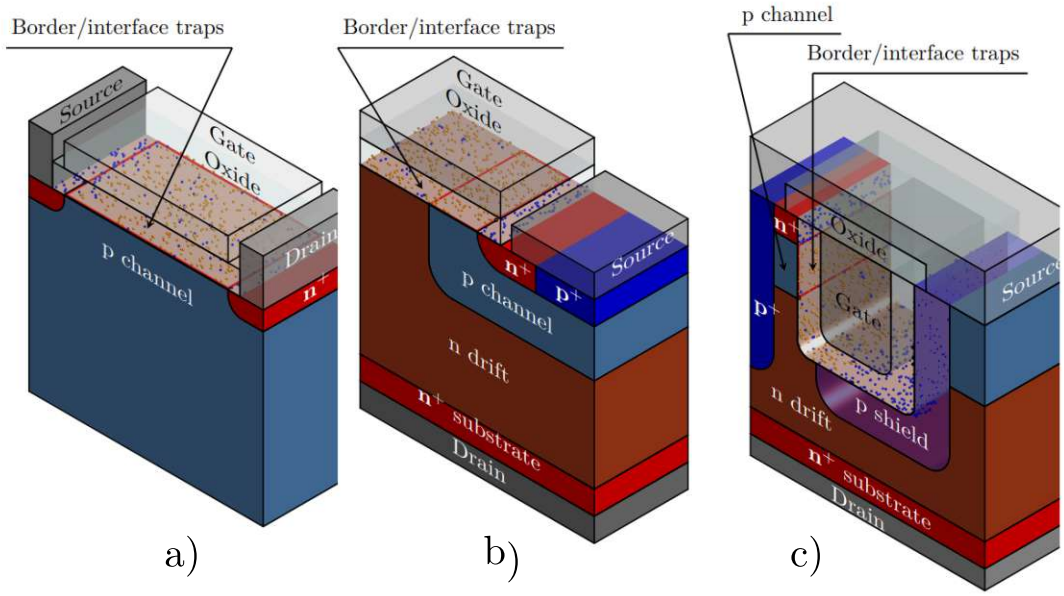


Figure 1.2.: a) Lateral 4H-SiC transistor. The possible defects leading to the distortion of the $C-V$ and $I_{\mathrm{d}}-V_{\mathrm{gs}}$ curves are shown. b)Planar DMOSFET c) Asymmetric trench 4H-SiC MOSFET (the very light grey marks the oxide).

2. Overview of Reliability Concerns

Time-dependent threshold voltage instability, also known as Bias Temperature Instability (BTI), occurs under a static gate bias. A positive gate bias induces a positive threshold voltage shift, commonly referred to as Positive Bias Temperature Instability (PBTI), whereas a negative gate bias results in a negative threshold voltage shift, known as Negative Bias Temperature Instability (NBTI) [11], [12], [13]. The permanent BTI is almost unrecoverable on a timescale of hours. Regardless of how the threshold voltage drifts, static BTI can be treated as low risk in circuit operation and can be managed by interface passivation and correctly selecting the gate voltage. However, because the gate stress applied to the SiC MOSFET is usually dynamic rather than static, the threshold voltage instability under dynamic gate stress, which is referred to as the dynamic BTI, is more important [14]. Similar to the case of a static BTI, the threshold voltage in a dynamic BTI drifts positively under positive gate bias and negatively under negative gate bias. However, unlike the static BTI, the dynamic threshold voltage drift, which is mostly induced by the interface traps, is believed to recover within one device switching period. Dynamic BTI, also known as threshold hysteresis, is often regarded harmless [15], [16]. As silicon carbide SiC epitaxy technology advances [17], they experience fewer crystalline defects, resulting in longer carrier lifetimes and, for example, a low R_{on}. However, the main degradation effects arise from the interfaces between SiC and the oxides because of their amorphous nature. This leads to dangling bonds and defects in the oxides. Hence, we can observe that in MOSFETs, effects such as channel mobility degradation, $1/f$ noise, random telegraph noise (RTN) [18], hot carrier degradation (HCD) [19], positive- and negative-bias temperature instability (PBTI and NBTI), and hysteresis [20].

It is shown that the different behaviors of MOSFETs during positive and negative gate voltage stress and temperature variations originate from the different trap parameters. Understanding and predicting the charging and discharging kinetics of oxide and interface defects is important for improving the reliability of 4H-SiC MOSFET reliability or controlling BTI to investigate state-of-the-art devices based on trap kinetics. Eventually, significant progress was made using the nonradiative multiphon NMP model with modifications and how the trap parameters influence the capture emission regime, resulting in the occupation of these traps and reliability issues such as BTI and hysteresis [18], [21].

The first review paper, which presented a synthesis of theoretical and experimental results, was presented by Wang *et al.* in 2006 [22]. The asymmetry in the measurement results, which has been observed by various scientists, was described by the different types of traps, owing to the amphoteric nature of P_{b} centers and hydrogen bridges (Si–H–Si), which have been considered the main culprit for BTI [23], [24], [25], [26].

When the 4H-SiC MOSFET is stressed by applying high gate voltages at elevated temperatures, we can observe the threshold voltage shift ΔVth which is called bias temperature instability. During the stress time at room temperature, the dynamic nature of V_{th} did not degrade the device because the effects were recoverable and repeatable. V_{th} drift is non-destructive, non-permanent, and reversible owing to a transient charge-trapping phenomenon [16]. However, in a pseudo-D CMOS inverter circuit with 4H-SiC MOSFETs, the impact of charge trapping leads to performance degradation and increases circuit delay [27]. For example, if V_{th} shifts in the negative direction, it might result in a substantial increase in the device leakage current, even when the device is supposed to be in an off or blocking state, and the positive V_{th} shift tends to increase the on-state resistance and degrade performance [16], [28], [29].

The progress made in enhancing the properties of the 4H silicon carbide (4H-SiC) epitaxial layer has provided a significant boost for its application in high-power electronics, owing to its unique attributes compared to silicon (Si). The ability to grow native oxides on the surface of a 4H-SiC substrate enables the creation of MOSFETs without requiring substantial modifications to the manufacturing process employed for silicon Si MOSFETs [30]. The wider bandgap of 4H-SiC results in an increased number of active traps and defects caused by imperfect manufacturing processes and contamination, as well as the different band alignment compared to Si. Consequently, the initial investigations focused mostly on studying the mechanisms occurring at the interface between SiC and SiO_2, specifically in different crystal structures and surface orientations, and their subsequent enhancements. Early studies, such as the one conducted by Afanas′ev *et al.* [8], [31], [32], [33], [34], [35], [36], [37], [38], [39] Lelis *et al.* [16], [28], [29], [40], [41], [42], [43], [44], [45], [46], [47], [48], Aichinger *et al.* [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], [75], [76], Kimoto *et al.* [7], [17], [36], [38], [39], [77], [78], [79], [80], [81], [82], [83], [84], [85], [86], [87], [88] and another authors have examined the impact of border, oxide, and interface traps in MOScap and MOSFETs structures. These studies focused on the effects of these traps on voltage shifting and hysteresis using techniques such as $I_{\text{d}} - V_{\text{gs}}$ and $C - V$ measurements. Subsequently, initial techniques for passivation in various environments were suggested, including annealing and stress testing.

2.1. Hysteresis in the $C - V$ Characteristics of MOSCAPs and MOSFETs Devices

Capacitance - voltage ($C - V$) curves are one of the most common methods used to investigate the 4H-SiC/SiO_2 interface properties, owing to the visibility of trap states during the depletion and accumulation regimes in the shifted or stretched-out $C - V$ curves. $C - V$ measurements can be performed on both MOSCAP and MOSFET structures. Fig. 2.1 illustrates the ideal and real $C - V$ curves during both up and down gate voltage sweeps. In the ideal case, the high-frequency MOSCAP $C - V$ (HF $C - V$) follows the lower curve in Fig. 2.1. In contrast, at a low frequency or

quasi-static (QS), even MOSCAPs $C-V$ would follow the upper curve. When an up-gate voltage is applied, the Fermi level moves, leading to a change in the occupation of the interface or borer traps. The "stretch out" effect (or ΔV_{th} and ΔV_{fb} shifts) at high-frequency $C-V$ curves corresponds to fast interface traps, while the hysteresis width (calculated as the difference between down and up voltage shifts for depletion to accumulation and to inversion regions) corresponds to slow border traps. These shifts depend on the number of trap states and their energy levels. The fixed oxide traps contributed to the parallel shift of $C-V$ curves, without any hysteresis effect.

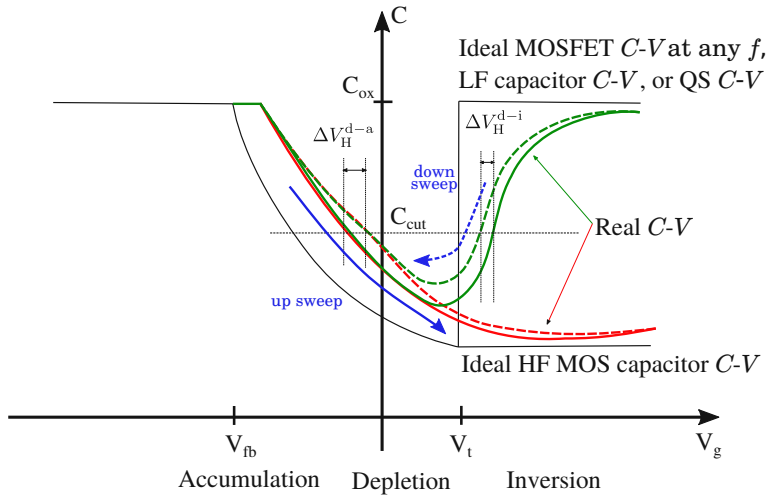


Figure 2.1.: Ideal $C-V$ curves (black line) and shifted $C-V$ curves (green and red lines). The solid colored lines represent the up-gate voltage sweep, and the dashed line represents the down-gate voltage sweep. Hysteresis widths $\Delta V_{\mathrm{H}}^{\mathrm{d-a}}$ and $\Delta V_{\mathrm{H}}^{\mathrm{d-i}}$ are the differences between the up and down curves at the corresponding capacitance C_{cut}. It was assumed that the flatland voltage ΔV_{fb} and threshold voltage ΔV_{th} shifts, together with the hysteresis ΔV_{H}, were due to charge trap kinetics at the 4H-SiC/SiO_2 interface and in the oxide.

2.2. Hysteresis in the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ Characteristics of MOSFETs Devices

The fast and ultrafast $I_{\mathrm{d}}-V_{\mathrm{gs}}$ up- and down- (or back-and-forth) characteristics may have a hysteresis effect (see Fig. 2.2). As in $C-V$ curves, this was due to the oxide-trap charging effect [12], [40]. ΔV_{th} and ΔV_{H} depend on the trap type and measurement conditions, such as the sweep rate, sweep gate voltage range, and temperature. If the up-gate voltage sweeps in the positive direction, we have a positive V_{th} or positive-bias temperature instability (PBTI) in the nMOSFET. Conversely, if has a more negative starting gate voltage, we have a negative bias temperature instability or NBTI when V_{th} shifts toward lower gate voltages. The absolute hysteresis width was calculated as the difference between the downward and upward absolute voltage shifts of the reference drain currents.

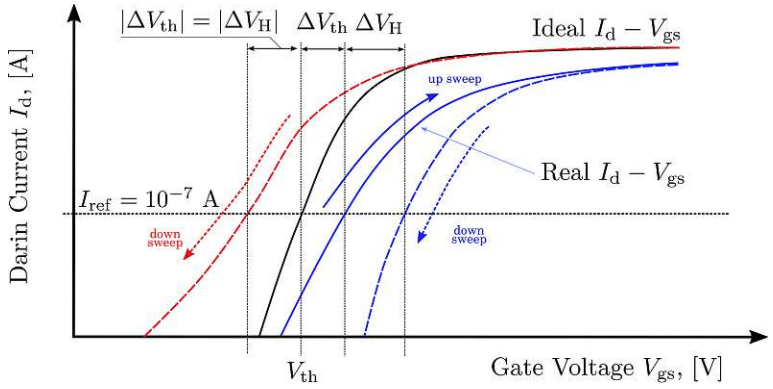


Figure 2.2.: Ideal $I_d - V_{gs}$ curves (black line) and shifted $I_d - V_{gs}$ curves (blue and red lines). The absolute hysteresis width $|\Delta V_H|$ was calculated as the difference between the down- (dashed line) and up- (solid line) absolute voltage shifts $|\Delta V_{th}|$ at the reference drain current ($I_{ref} = 10^{-7}$A). For NBTI, ΔV_{th} is negligibly small (not plotted) and $|\Delta V_{th}| \approx |\Delta V_H|$.

For the PBTI, the hysteresis is due to acceptor-like traps located close to the conduction band. For NBTI, the charge trapping kinetics are more complicated, and it is assumed that this is due to neutral traps with energy levels in the middle of the 4H-SiC bandgap, which can capture or emit electrons or holes. The final hysteresis width depends on the net charges in the occupied acceptor- or donor-like defects under PBTI and NBTI conditions [89]. The subthreshold slope $SS = \partial V_{gs}/\partial \log(I_d)$ is another critical parameter for switching between the ON and OFF states within a small gate bias range.

2.3. Hysteresis at Fast Bipolar Switching

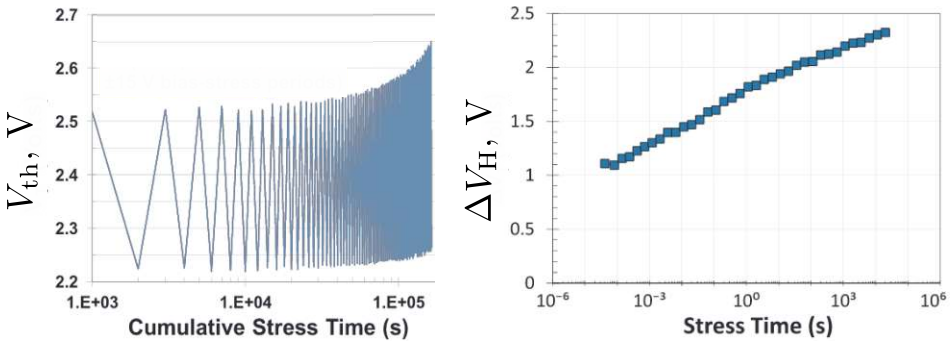


Figure 2.3.: Right: The constant back-and-forth bias-temperature stress under positive gate bias (+15 V), followed by 1000 s under negative gate bias (–15 V), repeated over and over, at 150 °C. V_{th} slowly increases and drifts in the positive direction because of the activation of additional near-interface oxide traps. V_{th} was calculated by determining the change in voltage for a constant current. Left: Example of increasing the hysteresis width at stress time owing to a back-and-forth gate bias stress sequence. From *Lelis A. J., et al. "SiC MOSFET threshold-stability issues." Materials Science in Semiconductor Processing (2018), 78 , pp.32-37* [90].

The hysteresis width at back-and-forth, or bi-polar stress, increases in comparison with the stress at one polarity (see Fig. 2.3, left [90]). It also increases for two different V_{high} and V_{low} combinations of the AC signal (as in gate switching instability (GSI)) [91]. The magnitude of this V_{th} instability also increased with increasing applied gate bias stress (see Fig. 2.3, right). Because the devices have different faces, ΔV_{th} may behave differently over time. For example, ΔV_{th} shifts more with an increasing magnitude of the positive gate bias stress, whereas ΔV_{th} quickly saturates with an increasing magnitude of the applied gate bias during negative bias stress. This process is generally reproducible [90].

2.4. Correlation Between Bias Temperature Instability and Hysteresis

BTI is an important degradation effect in 4H-SiC devices. This phenomenon manifests as the capture of charges at both pre-existing and newly formed defects within the oxide layer or the interface of MOS devices when subjected to elevated bias voltage and temperature conditions [92]. At BTI, the device threshold voltage $|\Delta V_{th}|$ (or $|\Delta V_{fb}|$ in $C-V$) increases, whereas the gate leakage is enhanced, resulting in an increase in circuit power consumption [16]. The positive shift in ΔV_{th} is expected to increase the on-state resistance and degrade performance. [16], [28], [29].

The hysteresis phenomenon is attributed to the same charge-trapping mechanism observed in BTI. This is because not all charges are emitted during the reverse- or down-gate voltage sweeps. Similar to the BTI, the hysteresis width is influenced by measurement parameters such as the sweep rate, temperature, and sweep range.

The hysteresis width and threshold voltage/flat band shifts were fully correlated, even under different conditions, as shown in Fig. 2.4 [93], [94].

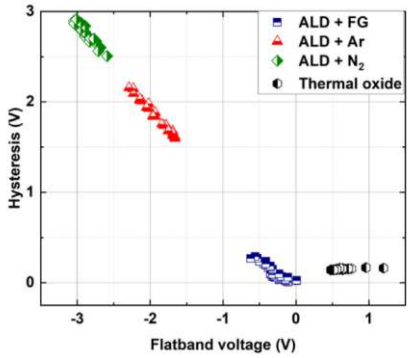


Figure 2.4.: Example of the correlation between ΔV_H and ΔV_{fb} plotted for 50 MOSCAPs per different sample and different POA. Based on *Renz A. B., et al. "The improvement of atomic layer deposited SiO_2/4H-SiC interfaces via a high temperature forming gas anneal." Materials Science in Semiconductor Processing (2021), 122, p.105527* [93].

However, it should be noted that the observed hysteresis differs from the classical BTI and should not be classified as a degradation. This phenomenon is both reversible and reproducible, and does not increase after the end of life [91], [95].

2.5. State of the Art and Thesis Outline

Utilizing the NMP theory for oxide and interface defects, along with the SRH theory for interface defects in lateral and trench 4H-SiC MOSFETs, combined with device simulation in modern TCAD frameworks, charge trapping has been recognized as the principal mechanism responsible for hysteresis width and BTI.

Existing models assume that the fluctuation of current-voltage characteristics is predominantly influenced by interface traps. However, the hysteresis width was not accurately simulated over a wide temperature range. Simultaneously, they depict the experimental curves and BTI for ambient and higher temperatures, specifically within the region 300–500 K. In this study, we extended the temperature range from 100 K to 600 K to compare the measured hysteresis widths in the $I_d - V_{gs}$ curves with those of the simulations. At the same time, a comprehensive study of the hysteresis width in the $C - V$ curves of lateral MOSFETs has not yet been conducted.

In this study, the hysteresis width, BTI, and subthreshold voltage slope of the $I_d - V_{gs}$ characteristics of lateral 4H-SiC MOSFETs across a temperature range of 150–300 K and the hysteresis width from 100 K to 600 K, incorporating an additional amphoteric P_b or P_{bC} trap type, were investigated. The hysteresis width and stretch-out effect of $C - V$ were simulated across a broad frequency range from 1 kHz to 1024 kHz and at elevated temperatures of 300 K, 373 K, and 448 K, incorporating an acceptor-like trap type at the mid-gap. To fit the $I_d - V_{gs}$ curves of the 4H-SiC MOSFETs across multiple cycles at room temperature, a unique trap system featuring donor-like traps was positioned slightly below the mid-gap. This system was further adapted to simulate the $C - V$ curves by including a high concentration of donor-like traps exponentially distributed from the valence band. The trap concentrations are lower than those in the conduction band, resulting in a higher channel mobility for trench devices; however, the hysteresis width is wider because of the larger concentrations of border traps positioned below the mid-gap compared with lateral devices.

Chapter 1 presents an overview of the advantages of using SiC as a substrate material in power MOSFETs, by detailing its material features. The latest SiC MOSFET structures are briefly explored, followed by an introduction of various SiC/SiO_2 interface properties resulting from different crystal orientations.

Chapter 2 presents an overview of reliability concerns. Specifically, the hysteresis width, BTI, and GSI in the $I_d - V_{gs}$ curves and their interrelations, as well as the hysteresis width and stretch-out effect of the $C - V$ curves.

Chapter 3 contains an overview of the measurement techniques used to investigate SiC/SiO_2 interface properties.

Chapter 4 defines the many reliability concerns observed in MOSCAP across planar, lateral, and trench MOSFETs, considering different facets, substrate types, measurement settings, oxide thicknesses, and POAs. Preliminary hypotheses regarding the trap type, density of states, and anomalous hysteresis width at high temperatures were reviewed.

Chapter 5 provides an overview of trap kinetics modeling approaches addressing reliability concerns related to pure SiC/SiO_2 interface quality is described in depth.

The two-state NMP model, which is extensively utilized for characterizing charge transfer reactions at defects, was employed and compared with alternative models. The specific impact of the hysteresis width on each NMP parameter was examined.

Finally, Chapter 6 describes the findings of the investigations conducted in this study. First, the hysteresis width, BTI, and subthreshold slope of the lateral MOSFETs within the temperature range of 150–300 K were reported using the NMP model for slow traps and the SRH models for fast traps. Second, the simulation of the hysteresis width of lateral MOSFETs across the temperature range of 100 K to 600 K was expanded and effectively modeled using the addition trap type. Third, the hysteresis width and stretch-out effect on the capacitance-voltage characteristics of the lateral MOSFETs were analyzed across different frequencies and temperatures. The incorporation of slower acceptor-like border traps along the SiO_2/SiC interface located at the midpoint of the 4H-SiC bandgap was implemented. In addition, the hysteresis in $I_d - V_{gs}$ of the trench MOSFETs across numerous cycles and in the $C - V$ curve was examined by investigating a unique trap system resulting from varying crystal faces.

Finally, the conclusions and outlook are presented. The potential uses and extensions of the proposed modeling method are described.

3. Measurement Techniques for Investigating SiC/SiO_2 interface Properties

Various measurement techniques and instruments have been developed to investigate the reliability of 4H-SIC MOSFETs. Many measurement parameters, including timing (measurement speed and delay), biasing range and polarity, and temperature, strongly influence the observed V_{th} shift. This indicated that the approach used in the measurements played a significant role in our investigation. These measurements can yield contradictory results when the initial state of the trap system is unknown. 4H-SiC, a wide-bandgap semiconductor, is well-suited for power applications that require operation at elevated temperatures, and the process of turning latent defects into active traps is accelerated. V_{th} in 4H-SiC MOSFETs at positive gate bias stress shifts positively, whereas it shifts negatively at negative gate bias stress. It follows that in most cases, these shifts are reversible and impermanent.

Because we have interface traps, fixed charges, oxide traps, near interface traps, or mobile ions of traps, separating the types of charges is difficult using conventional analysis techniques, such as $C-V$ and $I_{\mathrm{d}}-V_{\mathrm{gs}}$. For example, all types of charges will shift the flatband and threshold voltages, but the oxide and interface traps will also stretch the $C-V$ curve and subthreshold slope characteristics of the MOSFET $I_{\mathrm{d}}-V_{\mathrm{gs}}$. To directly analyze the number of switching oxide traps, the stretch out of the subthreshold $I_{\mathrm{d}}-V_{\mathrm{gs}}$ characteristics of the MOSFET during the up- and down-stress threshold voltage instability was measured [96]. To investigate the significant threshold voltage shift and increasing hysteresis width due to fast sweeping down, fast switching (typically faster than 15 µs) was used. In this section, we discuss and compare the most widely used schemes.

3.1. Fast and Ultra-fast $I_{\mathrm{d}}-V_{\mathrm{gs}}$ Measurement Techniques

Initially, adapted fast $I_{\mathrm{d}}-V_{\mathrm{gs}}$ measurement techniques for investigating SiC MOSFET were used by M. Gurfinkel, A.J. Lelis *et al.* [12], [89], [97], [98]. In the measurement scheme, the drain current was measured using an oscilloscope and generator, as shown in Fig. 3.1. The hysteresis width of $I_{\mathrm{d}}-V_{\mathrm{gs}}$ can be measured as the difference between the down- and up-gate-voltage sweeps. The fast $I_{\mathrm{d}}-V_{\mathrm{gs}}$ measured curves depend on the V_{gs} speed ramp and the bipolar DC stress.

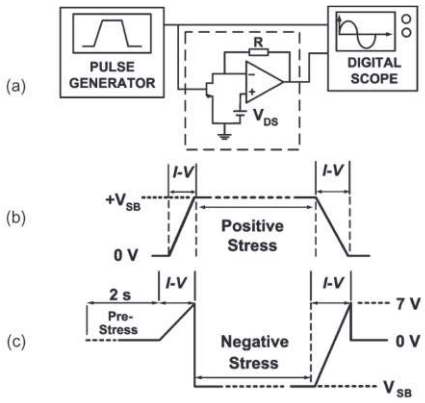


Figure 3.1.: . (a) Schematic of the fast $I-V$ measurement setup. (b) Positive-bias stress pattern. (c) Negative-bias stress pattern. Based on *Gurfinkel et al. "Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I – V Techniques." IEEE Trans. Electron Devices (2008), p 2005* [98].

3.2. Hysteresis Measurements at $I_d - V_{gs}$

Using this device characterization method, the gate voltage was swept up and down during the recording of I_d. Typically, one sweep cycle is used with long precondition pulses to avoid a cumulative effect and significant distortion, as shown on the left in Fig. 3.2. However, to understand the long-term trap behavior, several sweep cycles were applied (see Fig. 3.2, right). The one cycle $I_d - V_{gs}$ curves were measured at a fixed drain voltage of $V_{ds} = 0.1\,V$ while V_{gs} is swept up and down within the range of 0 to 20 V at a sweep rate of 3.2 V/s, see Fig. 3.2, left. A constant step width of 0.8 V was used for the gate bias.

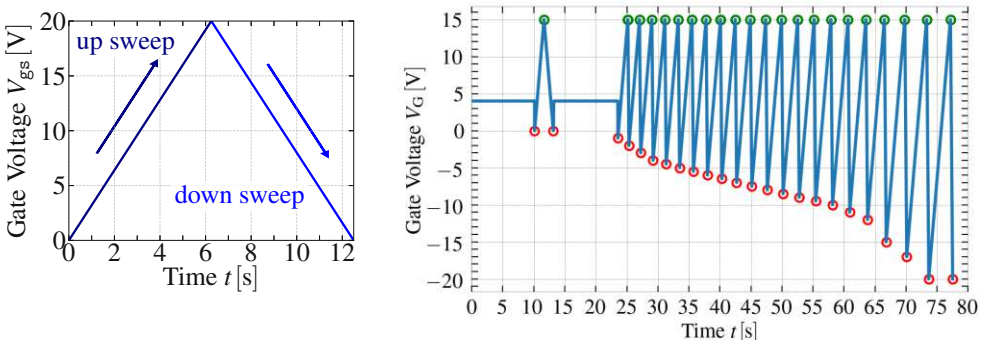


Figure 3.2.: Left: A method for sweeping the gate voltage during $I_d - V_{gs}$ measurements of planar 4H-SiC MOSFETs. The up sweep curve (dark blue) starts at 0 V. Right: An extended gate voltage up and down sweep of 21 cycles with an initial pre-stress signal was used for trench 4H-SiC MOSFET $I_d - V_{gs}$ measurements. The final gate voltage was −20 V and the starting voltage became more negative in each cycle. The sweep rates were the same for each cycle [99].

Two hysteresis widths, ΔV_{H1} and ΔV_{H2}, are defined as the difference between up and down ΔV_{th} values corresponding to the two reference drain currents ($I_d^{ref1} = 10^{-7}$A and $I_d^{ref2} = 10^{-9}$A, see Fig. 6.1). The hysteresis width was extracted for operating temperatures between 100 and 600 K [99].

At multiple cycles, the gate voltage V_{gs} sweep started at a positive gate bias stress of 4 V during 10 s (see Fig. 3.2, right). We then applied a zero pulse with a sweep rate of 1 V s^{-1} for up- and down-gate voltages within the range of 0–15 V. After the second stress period, we applied the next 21 pulses with a sweep rate of 1 V s^{-1} for up and 10 V s^{-1} for down gate voltages, and every period changed the starting negative gate voltage to the same final positive gate voltage.

3.3. "Up-and-Down" $C-V$ Measurement and Impedance Analysis

$C-V$ measurements are widely used to investigate the defect properties of MOS capacitance. An alternating current (AC) voltage of small amplitude, typically approximately 50 mV at a frequency of 100 kHz, was superimposed on a gradually varying direct current (DC) bias. Significant information can be derived from the $C-V$ characteristics, including the flat-band voltage (V_{fb}), threshold voltage (V_{th}), bulk doping, and surface potential (ϕ_s). This information can be obtained either by measuring the displacement current during a gate voltage sweep (ramp-up method) or by superimposing a small AC signal onto the DC gate bias and measuring the AC current (impedance method), as shown in Fig. 3.3. Both MOSCAP and MOSFET devices can be used for $C-V$ measurements.

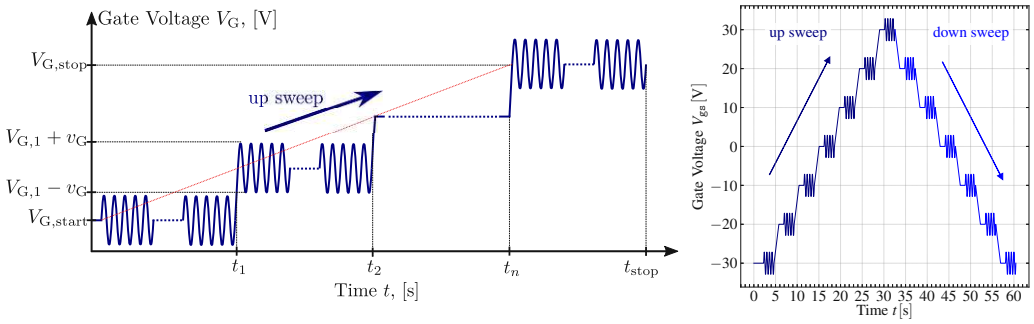


Figure 3.3.: Left: Depiction of V_G waveform applied to the gate for C_{gb}. An up V_G sweep signal was applied to the gate to establish the MOS capacitor, followed by a high-frequency (10 kHz to 10 MHz) and low-amplitude v_g (50 mV). The AC signals were superimposed onto each V_G level, after which the AC current (i_B) through the capacitor was measured to calculate capacitance. The same procedure was repeated during the downward V_G sweep (not plotted). The dashed red line represents sweep rate $V_{G,n}/t_n$. Right: Schematic of the gate voltage applied during impedance measurement. Both the small-signal and the gate voltage sweep are used in the transient analysis to investigate traps dynamics [100].

When MOSFETs are used, the source and drain contacts are typically grounded or

linked to the bulk. The main difference between MOSCAP and MOSFET devices is that in MOSFETs, the minority carriers necessary for inversion can be rapidly provided by the source and drain regions. This facilitates faster gate bias sweeps, in contrast to MOSCAP systems. The drawbacks of MOSFETs include supplementary parasitics resulting from the overlap between the source and drain areas with the gate, or other geometrical issues. MOSCAP structures have the added benefit of being predominantly one-dimensional, facilitating the use of easily understood and precise models for characterization. In up- and down- (or "back-and-forth" [101]) impedance measurements, full information regarding slow and fast traps can be investigated [102].

The small-signal method was employed for the measurement of the $C-V$ and con-ductance-voltage ($G-V$) curves. Equivalent circuit capacitance and conductance were configured in parallel. A sinusoidal small signal for each bias step, along with the gate voltage up and down sweeps, was employed to examine the trapping dynamics, as illustrated in Fig. 3.3, right [103], [104]. Gate voltage V_{gs} varied between $-30\,\mathrm{V}$ and $30\,\mathrm{V}$ at a rate of $2.0\,\mathrm{V\,s^{-1}}$, as illustrated in Fig. 3.3. The measured small-signal amplitude was $50\,\mathrm{mV}$, with a frequency range extending from $4\,\mathrm{kHz}$ to $1024\,\mathrm{kHz}$. The time interval for each gate bias was $0.13\,\mathrm{s}$ and the delay between the upward and downward sweeps was $12\,\mathrm{ms}$. The hysteresis width was determined for operating temperatures $300\,\mathrm{K}$, $373\,\mathrm{K}$, and $448\,\mathrm{K}$ [100].

Impedance Extraction

Detecting fast states necessitates very high-frequency measurements, which complicates the identification of defects owing to the series resistance and inductance [78].

The small signal impedance Z is given by the division of the complex values of the AC gate voltage v_g and bulk current i_B: [102]

$$Z = \frac{v_G}{i_B} \tag{3.1}$$

$$|Z| = \frac{|v_G|}{|i_B|} \tag{3.2}$$

$$\arg(Z) = \arg(v_G) - \arg(i_B) \tag{3.3}$$

Commercial impedance analyzers or $C-V$ meters often give the impedance as values of an effective parallel or series $R-C$ circuit:

$$Z = R_s + \frac{1}{jwC_s} \tag{3.4}$$

$$1/Z = 1/R_p + jwC_p \tag{3.5}$$

When the equivalent circuits accurately represent the setting, it is advisable to identify the complex impedance and thereafter compute the required $C-V$ curves by utilizing the most appropriate equivalent circuit for a specific combination of the experimental setup, operating conditions, and device [102].

3.4. Measure-Stress-Measure Technique

The measureure-stress-measure technique or MSM is used for V_{th} shift measurement and is typically not used for hysteresis extraction. This method consists of a three face: first, where the fresh device is measured; second, the voltage stress is applied; and third, the final measurements after stress. The stress and measurement phases can be repeated several times, often under severe conditions. In the extended MSM (eMSM) scheme during the measurement phase, additional important device characteristics are controlled, such as V_{th}, mobility, and channel conductivity, as shown in Fig. 3.4 [57], [102], [105], [106]. The measurements can also be performed at various temperatures.

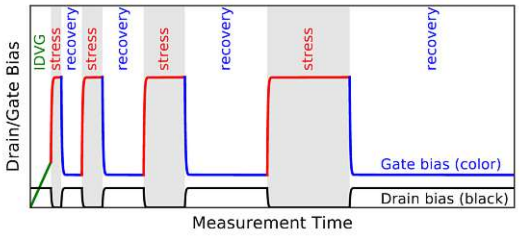


Figure 3.4.: Typical for an eMSM sequence are the repeatedly applied phases of stress and recovery bias. After each cycle, the stress and recovery times were increased. It should be noted that the initial $I_d - V_{gs}$ affects the charge state of the number of traps. From *Waltl M. "Defect Spectroscopy in SiC Devices." IRPS (2020)* [105].

3.5. The Fast I_d Measurement Technique

Using the fast I_d method, I_d was measured at V_{mes} as quickly as possible with no stress-off time, as shown in Fig. 3.5, right. The V_{th} shifts were extracted from the parallel $I_d - V_{gs}$. ΔV_{th} can be simply computed from the I_d shifts in the linear area with the initial transfer conductance g_m, which represents the slope of $I_d - V_{gs}$, as shown in Fig. 3.5, left.

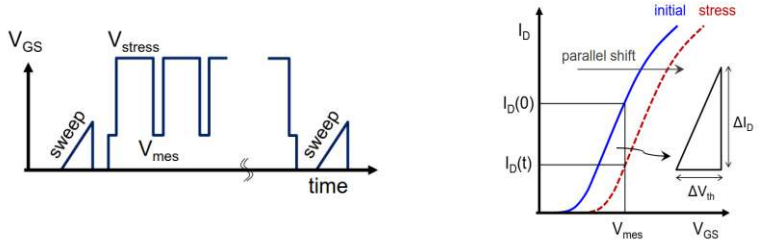


Figure 3.5.: Left: Schematic V_{gs} patterns of the fast I_d method in the PBTI tests. Right: Schematic of $I_d - V_{gs}$ before and after PBTS and the calculation of the V_{th} shift in the fast I_d method. From *Okunishi T.*, et al. *"Reliability study on positive bias temperature instability in SiC MOSFETs by fast drain current measurement." Jpn. J. Appl. Phys., (2017) p. 04CR01-2* [107].

$$\Delta V_{\mathrm{th}} = \frac{I_D\,(0) - I_D\,(t)}{g_m} \tag{3.6}$$

The fast I_{d} method is more precise than the standard method because of its ability to reduce measurement time. Nevertheless, this method is not infallible, as it allows for a measurement delay of several milliseconds [107]. The fast I_{d} method was used to investigate PBTI at different temperatures [107].

3.6. Bipolar AC Gate Bias Stress Test

This measurement technique was used to measure the threshold voltage shift and hysteresis width at various temperatures during a bipolar AC signal in the range of 50 kHz [91], [108]. As described in [108] the measurement delay should be shorter than the period time; for measuring V_{th} the AC signal must be interrupted at several points, and the shortest possible measurement delay with our setup is $t_{\mathrm{d}} = 1\,\mu\mathrm{s}$, see Fig. 3.6.

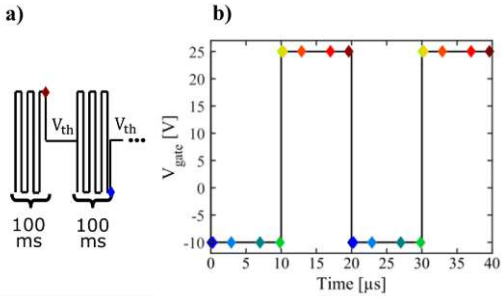


Figure 3.6.: a) The AC stress was interrupted at different points for the threshold voltage measured from 1 µs to 10 ms recovery times. (b) Example of a 50 kHz bipolar AC signal with different points of interruption, as described in (a). From *Puschkarsky K.*, et al. *"Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability." TED, (2019) p. 4609* [91].

3.7. Charge-Pumping Technique

The standard charge-pumping method uses a constant pulse amplitude while sweeping the base level. The maximum charge pumping current I_{cp} was measured, and V_{th} and V_{fb} were estimated by the positions of the rising and falling edges of the signal, respectively. The typical pulse frequency was 500 kHz, where the measured I_{cp} was primarily due to the fast interface traps, as shown in Fig. 3.7. This method was employed to investigate the kinetics of the interface traps and their impact on the ΔV_{th} shift during BTS. At a gate bias of 150 °C, an increase in the charge-pumping current

over time indicates the formation of acceptor-like interface traps (or near-interface oxide traps) responsible for the positive drift under these conditions [44].

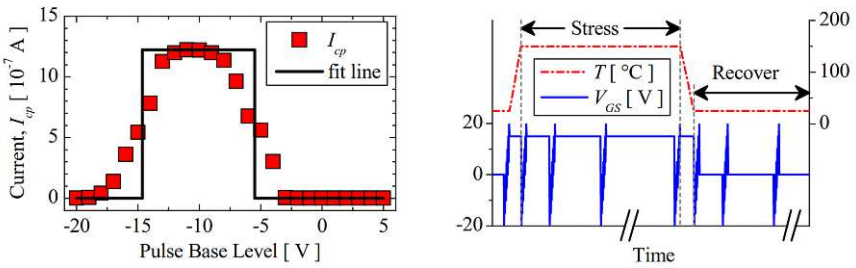


Figure 3.7.: Left: Charge pumping current I_{cp} versus the pulse base level (red squares), along with a fit line used to determine the number of charge pumping states N_{cp}, V_{th}, and V_{fb} (solid black line). Right: Schematic of the stress-and-measure sequence showing profiles of temperature (dashed red line) and gate bias (solid blue line) as a function of time. From *Habersat D.B.,* et al. *"Evaluation of PBTS and NBTS in SiC MOS Using In Situ Charge Pumping Measurements." MSF, (2013) p. 546* [44].

3.8. The Pump-Probe Measurement

The pump-probe measurement investigates the correlation between the threshold voltage shift recovery and the number of emitted photons.

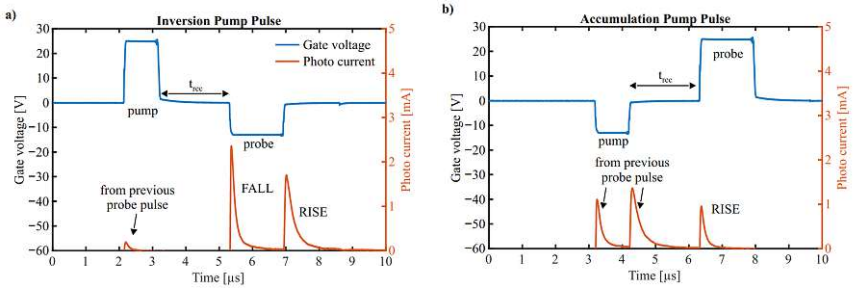


Figure 3.8.: Measured photocurrent in response to a pump-probe pulse scheme at the gate for inversion (a) and accumulation (b) pump pulses, respectively. A pump pulse provokes charge trapping at defects, whereas the probe pulse provides opposite charge carriers, leading to trap-assisted recombination and emission of photons. From *Feil M.W.,* et al. *"Optical Emission Correlated to Bias Temperature Instability in SiC MOSFETs." IRPS, (2022) p. 3B.1-4.* [109].

Using a silicon photomultiplier (SiPM) in the bipolar AC gate bias stress test, photon emission was measured at both the rising and falling edges of the gate signal, represented by the SiPM current. The field effect at the semiconductor-insulator interface induces out-of-equilibrium occupancy of defects by applying a 1 µs pump pulse to the gate. The pump pulse can be positive (inversion) or negative (accumulation). The pump pulse is succeeded by a recovery phase of duration t_{rec}, during which the out-of-equilibrium state may return to equilibrium at a gate voltage of 0 V, as shown in Fig. 3.8 [109], [110].

3.9. Gate-Switching-Stress Test

A recent study (Puschkarsky *et al.*, Feil*et al.* [55], [56], [59], [111], [112]) explained gate switching instability (GSI), a phenomenon in which bipolar alternating gate voltages induce an increased threshold voltage drift compared with static gate voltage measurements (DC-BTI/DC-HTGS) [14], [15], [76], [113]. In certain applications, 4H-SiC MOSFETs require continuous gate-voltage switching at frequencies of hundreds of kilohertz. In this operational mode, the positive gate bias significantly exceeded the threshold voltage during the high phase ($V_{GH} \gg V_{th}$), whereas the negative gate bias substantially fell below the flat-band voltage in the low phase ($V_{GL} \ll V_{fb}$). For this, an alternating current high-temperature gate-bias stress (AC-HTGS) test or gate switching stress (GSS) test, which covers all gate oxide drift phenomena, was created, as shown in Fig. 3.9 [55].

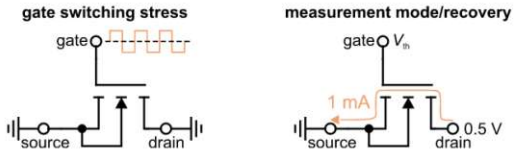


Figure 3.9.: Schematic illustration of GSS and the measurement of V_{th} via a feedback loop. During stress, the MOSFET is switched in bipolar mode while keeping both the drain and source terminals grounded. When measuring the V_{th}, a feedback loop forces a constant drain–source current (I_{DS}) by regulating the gate voltage. From *Feil M.W.,* et al. *"Gate Switching Instability in Silicon Carbide MOSFETs—Part I: Experimental." TED, (2024) p. 4211.* [114].

Both BTI and GSI occur and superimpose on the total ΔV_{th}:

$$\Delta V_{th} = \Delta V_{th}^{BTI}(t_{stress}) + \Delta V_{th}^{GSI}(n)\,;\; n = t_{stress} \cdot f_{SW} \tag{3.7}$$

where n is the switching cycle, t_{stress} is the fixed stress time. The GSI component depends on the cumulative number of switching cycles n, whereas the frequency-independent BTI component still depends on t_{stress} [114].

3.10. Summary

This chapter presents typical techniques for MOSFET parameter extraction, emphasizing the characterization of the hysteresis width, bias temperature instability, and gate-switching instability in large-area transistors. In this research, two main measurement techniques have been employed: "up-and-down" $C-V$ measurement and impedance analysis and hysteresis measurements at $I_d - V_{gs}$.

4. Instability of 4H-SiC MOSCAPs and MOSFETs

In this chapter, a review of previous investigations on the measured instability of MOS capacitors (MOSCAPs) and MOSFETs found in the literature is presented. Since 1996, investigations on SiC/SiO_2 interfaces have grown rapidly. The $C-V$ analysis of MOSCAPs was used to identify the trap density of states (DOS) responsible for the "stretch-out" effect, shift in V_{fb}, and hysteresis phenomenon. The different interface properties were dependent on the SiC polytypes and crystal faces upon which the oxide was deposited. The technique of growth and post-oxidation annealing, along with channel properties such as the concentration and conduction type, contribute to the variation in the trap DOS. In addition to electrical measurements, optical measurements, such as photoemission of electrons and spectral analysis, were used to examine the trap system. With the possibility of manufacturing the first SiC MOSFETs, the instability of the transient $I_d - V_{gs}$ characteristics, such as V_{th} shift and hysteresis width, was investigated. The effective operation of both n-channel and p-channel MOSFETs is significantly influenced by Bias Temperature Instabilities (BTI), which represent a critical reliability issue. By applying bipolar stress, both positive and negative BTI values were obtained. With increasing switching frequency of the AC signal, extra Gate Switching Instability (GSI) plays a significant role. The instability in the measured data from identical devices using different methods should be consistent for the same trap types and DOS. Differences may arise in the sensitivity of the measurement techniques. This indicates that all phenomena, such as BTI, HCD, hysteresis, and GSI, should be correlated, because the device under testing exhibits identical traps. Simultaneously, measurement parameters such as temperature, sweep rate, sweep range, high- and low-voltage levels, frequency, delay time, and preconditions significantly influence the measured data, and these effects must be clearly identified and considered. In addition, a transition layer at the border of SiC/SiO_2 was detected to investigate the spatial trap distribution and impurities in the oxide.

4.1. Hysteresis at MOSCAPs

MOSCAPs are essential in research and development as they provide a direct, dependable, and easy to use method to investigate the electrical characteristics of the SiC/SiO_2 interface, which is crucial for the performance and scaling of MOS devices. These fundamental structures usually include metal, oxide, and semiconductor layers. Their simplicity removes multiple complex variables and additional distortions, which makes them optimal for investigating the intrinsic characteristics of the interface.

The fundamental contribution of the SiC/SiO_2 interface investigations was made by Afanasév V.V. *et al.* [32], Kimoto T. *et al.* [83], Lelis A. *et al.* [101] and numerous other researchers and groups. In 2011 D. Habersat *et al.* and A. Lelis *et al.* improved the observation of SiC/SiO_2 oxide charge traps. Measurements utilizing the "back-and-forth" $C-V$ technique exhibit more overall instability than $I_d - V_{gs}$ and may correlate with measurements conducted using fast $I_d - V_{gs}$. $C-V$ measurements are sensitive to traps situated within the midgap, thereby enabling this method to be more precise for evaluating the actual density of the trap states. “One-way negative bias-stress” $C-V$ measurements indicate considerable instability when compared to one-way bias stress $I_d - V_{gs}$ measurements. The net bias – stress shift or hysteresis is the difference between the up and down gate voltage sweeps at the reference flat-band capacitance for V_{fb} $(C-V)$ or current for V_t $(I_d - V_{gs})$ [101]. Multiple studies have been conducted on samples with different properties.

4.1.1. Temperature Dependence of the Hysteresis Width at Various Faces

As mentioned before, there has various faces in 4H-SiC that have different properties. The hysteresis widths at different temperatures are shown in Fig. 4.1. Based on Yano H. *et al.*, the hysteresis for (0001) and $(03\bar{3}8)$ was minimal (< 0.1 V), whereas 0.4 V was observed for $(11\bar{2}0)$. At a low temperature of 100 K, both the flatband voltage shift ΔV_{fb} and hysteresis ΔV_H increase because of the interface states at shallow energy levels [7]. The shallow interface states located near the conduction band induce a positive flatband voltage shift owing to the electrons being trapped in these states, which remain for a long time and act as negative fixed charges. Some trapped electrons were slowly emitted throughout the voltage sweep in the capacitance-voltage measurements, even at low temperatures, resulting in hysteresis.

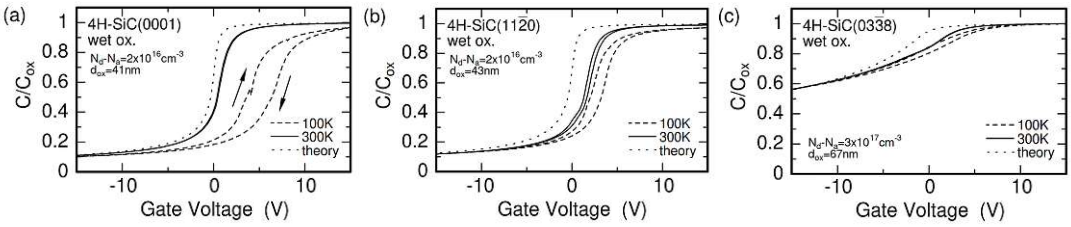


Figure 4.1.: High-frequency $C-V$ characteristics of n-type 4H-SiC MOS capacitors on (a) (0001), (b) $(11\bar{2}0)$, and (c) $(03\bar{3}8)$ faces. Solid and broken curves are obtained at 300 and 100 K, respectively. The dotted curves indicate theoretical calculations. Injection-type hysteresis was observed. Note that the gentle slopes of the $C-V$ curves for $(03\bar{3}8)$ are due to a higher net donor concentration and thicker oxide than for (0001) and $(11\bar{2}0)$. From *Yano H.,* et al. *"SiO_2/SiC Interface Properties on Various Surface Orientations." Mat. Res. Soc. Symp. Proc., (2003) p. K4.5.3* [7].

At room temperature, the emission time decreased, whereas the flatband voltage and hysteresis remained constant, indicating that defects were located close to the conduction band. The two additional faces demonstrated an increased flatband voltage shift of approximately 4.9 V and 4.4 V for $(11\bar{2}0)$ and $(03\bar{3}8)$, respectively. The increase

in the hysteresis was also dependent on the surface orientation. At 100 K, the hysteresis for (0001) increased to 2.4 V, whereas it remained negligible at 300 K. The hysteresis measured at 100 K for the $(11\bar{2}0)$ and $(03\bar{3}8)$ orientations was recorded as 0.9 V and 0.4 V, respectively, at 100 K [7], [36], [77].

With almost little hysteresis and a minor stretch out, the $C-V$ curve for the (0001) face at 300 K indicates a low interface state density. In contrast, a significant increase in the stretch out near the accumulation region was also evident in the $C-V$ curves measured at 77 K. With a maximum positive accumulation bias of 10 to 40 V in 5 V, the hysteresis increased; however, this was not observed at 300 K. The 4H-SiC bandgap is reduced from 3.3 eV to 3.2 eV from 80 to 300 K. A significant number of N_{it} shifts energetically above the conduction band as the bandgap shrinks, making it impossible for electrons to occupy at 300 K [34], [35], [115], [116], [117]. However, at low temperatures, the carrier concentration is reduced because of incomplete deep dopant ionization, and the semiconductor changes from a doped to intrinsic material [118] which leads to a reduction in the voltage shift [119].

Particularly for (0001) close to the conduction band edge, ΔV_{fb} and hysteresis ΔV_H are correlated with an increase in the interface state density (see Fig. 4.1). The trap parameters are provided in Table A.1 and explained in the relevant section.

A preliminary schematic of the capture and emission processes of electrons and their influence on the hysteresis width in the $C-V$ measurements is shown in Fig. 4.2.

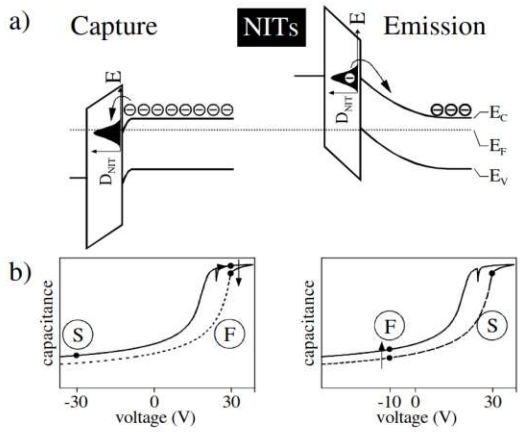


Figure 4.2.: a) Band diagrams and b) $C-V$ characteristics demonstrating the experimental situation for the capture and emission process of electrons. From *Pensl G.,* et al. *"Traps at the SiC/SiO_2-Interface." Mat. Res. Soc. Symp. Proc., (2001) p. H3.2.8* [36].

A sketch of the $C-V$ diagram with the corresponding band diagram for the starting (S) and final (F) is presented in Fig. 4.2 (a) and (b), respectively. To determine τ_c the voltage sweeps from the depletion (S) (which depends on the threshold voltage of the device) to the accumulation (F), and the number of charged electrons in N_{it} is measured. To determine τ_e the voltage sweeps from accumulation (S) to depletion (F) and the emission of electrons from N_{it} are monitored. These measurements resulted in two time constants for emission and capture (τ_e^1= 59 s, τ_e^2= 7.3 s, and τ_c^1= 63 s, τ_c^2= 6.8 s), which means that two different distributions of N_{it} contributed to D_{it} [36].

4.1.2. Anomalous Hysteresis Width at High Temperatures

In 2012 Chanthaphan A. *et al.* [120] investigated the unusual intrinsic positive mobile ion effects of the 4H-SiC (0001) Si-face MOSCAPs. These phenomena have been observed mostly in MOSFET structures, leading to V_{th} shift and decrease in the hysteresis width at elevated temperatures [48], [121]. However, at some point, the hysteresis width increases, especially at very high temperatures [122], particularly at the Si face. The electron injection and ion drift effects were hypothesized to explain the clockwise (positive) and counterclockwise (negative) behaviors, respectively. Fig. 4.3 shows this bidirectional $C-V$ curves measured at room temperature (black open squares) and 200 °C (red open triangles). When the measurement temperature was increased to 200 °C, the orientation of the $C-V$ hysteresis reversed counterclockwise.

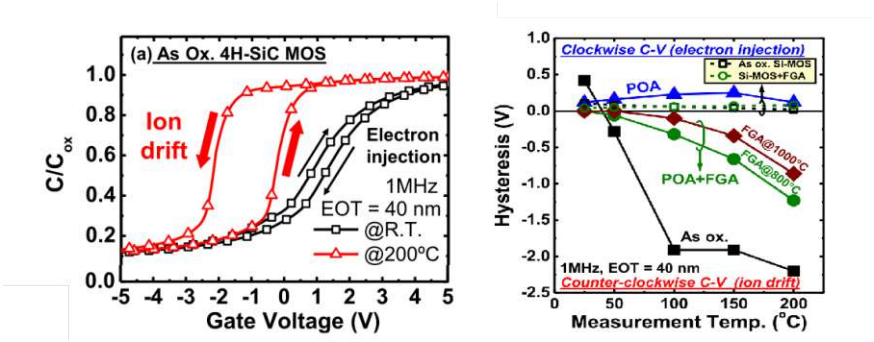


Figure 4.3.: Left: Bidirectional C-V curves obtained from a SiC-MOS capacitor with an as-oxidized thermal oxide. $C-V$ measurements were performed at room temperature (black open squares) and 200 °C (red open triangles). The measurement frequency was 1 MHz for all the cases. Right: The temperature-dependent $C-V$ hysteresis of the SiC-MOS capacitors (solid lines with filled symbols) depends on different POA and high-temperature forming gas annealing (FGA) conditions in comparison with the as-oxidized SiC capacitor (As ox.). From *Chanthaphan A.*, et al. *"Investigation of unusual mobile ion effects in thermally grown SiO_2 on 4H-SiC(0001) at high temperatures." Appl. Phys. Lett., (2012) p. 252103-3* [123].

Upon cooling to the normal temperature, the bidirectional $C-V$ curve obtained for the exact capacitor reverted entirely to a clockwise orientation, indicating that the influence of mobile ions is significant only at elevated temperatures [120], [123].

The SiC MOSCAPs that received PBTS before wet etching exhibited a marked negative V_{fb} shift and counterclockwise $C-V$ hysteresis, comparable to that of the as-fabricated capacitor at 200 °C. In contrast, no hysteresis at NBTI was observed at 200 °C. This effect depends on the defect passivation and is comparable to the effect of hydrogen treatment. Forming gas annealing (FGA) induces positive mobile ions in oxides [124], [125].

4.1.3. Hysteresis Phenomena in n-Type and p-Type MOSCAPs

E. Danielsson *et al.* [126] in 1998 employed MOS structures with TiN as a metal on n- and p- 4H-SiC in comparison with Al using $C-V$ measurements. They observed that the hysteresis and interface states were comparable for the two gate types. Leakage on the n-type substrate was lower than that on the p-type substrate. The high flatband voltage V_{fb} of the p-type samples was due to the high density of the interface states. In the flatband region, these states were uncharged for the n-type samples and positively charged for the p-type samples, leading to a larger voltage shift in the p-type samples, as shown in Fig. 4.4. This result is not correlated with Fig. 4.8, where D_{it} is higher for the n-substrate, but may depend on the measurement conditions.

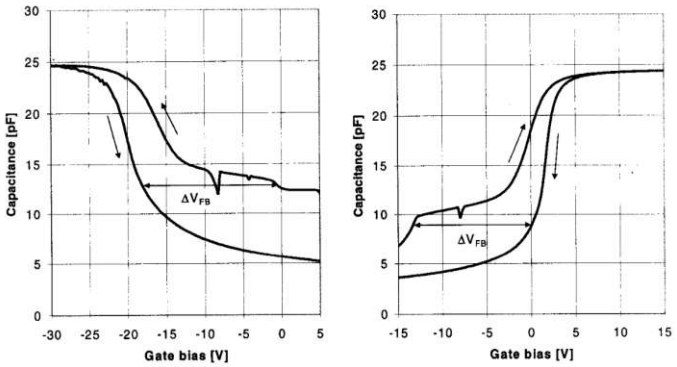


Figure 4.4.: Typical results from p-type and n-type $C-V$ measurements after FGA (400 °C). The arrows indicate the up- and down-gate voltage sweeps. ΔV_{fb} is due to charge capture at the interface. From *Danielsson E.,* et al. *"Thermal Stability of Sputtered TiN as Metal Gate on 4H-SiC." MSF., (1998) p. 807* [126].

The kinetics of charge trapping are influenced by deep dopants in the n- or p-type substrates of the 4H-SiC/SiO_2 structures. BTI may fluctuate because of these varying properties. The measured effective activation energies in 4H-SiC metal-oxide-semiconductor capacitors were 0.23 ± 0.2eV (for negative threshold voltage shifts) for p-type capacitors and 0.12 ± 0.20eV (for positive threshold voltage shifts) for n-type capacitors. At room temperature, less than 50% of the p-substrate and more than 90% of the n-substrate were ionized; at lower temperatures, this value was even lower [119]. This factor may also affect the BTI and hysteresis width at extremely low temperatures.

In addition, asymmetric degradation occurs under gate-switching stress in both p- and n-type SiC owing to the reconfiguration of oxygen vacancies in the SiO_2 layer following hole capture, as illustrated in Fig. 4.5, left [127]. The midgap voltage (V_{mg}) shows a positive shift under positive gate bias stress at elevated temperatures for n-substrate capacitors with 67.5 nm nitrided oxides, which is attributed to total electron trapping by deep donors. Conversely, it exhibits a negative shift under a negative gate bias for p-substrate capacitors with 55 nm nitrided oxides, resulting from total hole trapping by deep acceptors. The effective activation energy for the BTI, measured within the temperature range of 25–250 °C, is 0.12 eV for n-substrate capacitors (positive shifts) and 0.23 eV for p-substrate capacitors (negative shifts), as illustrated

in Fig. 4.5, right [119]. The primary defect candidates for charge trapping include near-interfacial oxygen vacancies, deep interface traps, and/or nitrogen-related defects inside near-interfacial SiO_2 [119].

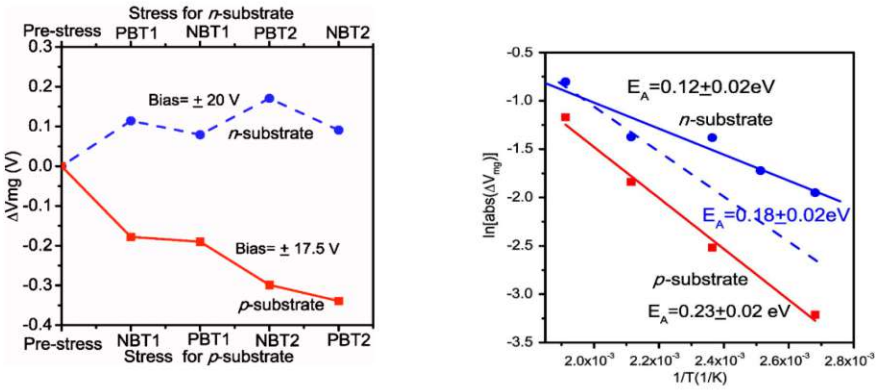


Figure 4.5.: Left: Midgap voltage shift (ΔV_{mg}) for n- and p-substrate 4H-SiC capacitors stressed at 150 °C. The applied biases were ±20 V (±17.5 V for n(p) substrate capacitors. The devices were stressed by deep depletion of the channel. The stress times were 20 min for the first set of biases and 60 min for the second set. From: [127]. Right: Midgap voltage shift as a function of the stress temperature for n- and p-substrate/4H-SiC capacitors stressed by accumulation for 20 min at 20 V (n-substrate capacitors) and −17 V (p-substrate capacitors) on the gates. From *Zhang E. X.,* et al. *"Bias-Temperature Instabilities in 4H-SiC Metal–Oxide–Semiconductor Capacitors." IEEE Trans. Device Mater. Relib., (2012) p. 393* [119].

4.1.4. ΔV_{fb} Shift and Hysteresis Width Under Specified Measurement Conditions

The magnitude of the V_{fb} shift and the hysteresis width are influenced not only by temperature but also by the sweep rate, sweep range, number of sweep cycles, frequency, and delay time [34], [128], [129], [130], [131], [132]. The stretch-out effect of the $C-V$ curves became more significant with each measurement cycle within the same voltage range sweeping from positive to negative values, indicating that more interface states were generated and the flatband voltage shift was estimated. Fig. 4.6 shows the bi-directional and single sweep instability of the $C-V$ curve. In the bi-directional measurements, a positive shift occurred with a positive stress bias, whereas a negative shift occurred with a negative stress bias. This hysteresis was entirely reversible and reproducible, requiring only a limited number of stress cycles and sweeps to determine the average bias stress shift. In single-sweep measurements, most bias instability occurs under negative bias stress [36]. Electrons trapped at deeper energy levels (∼0.2 eV below the conduction band edge) function as negative charges, resulting in a significant positive flat-band shift [77].

Additionally, in the bi-directional high-frequency (HF) $C-V$ curve of 4H-SiC MOS capacitors at 300 K, when the gate voltage was swept from −10 V to 10 V and then returned to −10 V, a clockwise hysteresis of 70 mV was observed. The observed

behavior may be explained by the polarity of the initial sweeping gate voltage, where a negative initial sweeping gate voltage results in a negative shift of V_{th}, whereas a positive initial sweeping gate voltage leads to a positive shift V_{th} which is attributed to the mobile ions [129]. A detailed review of the various trap types and their density of stes, which contribute to the discussed instability issues, is provided in the following section.

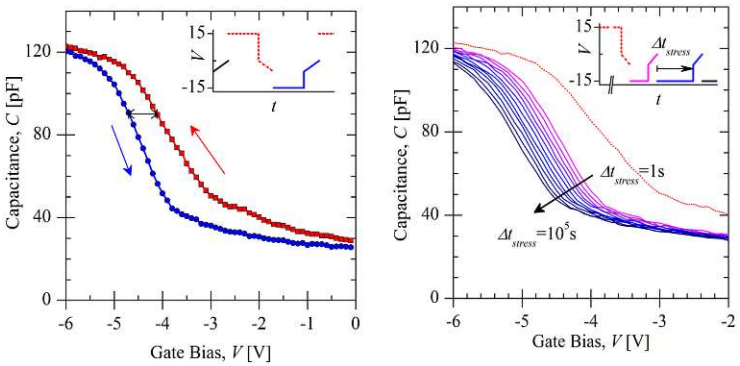


Figure 4.6.: Left: Bi-directional $C-V$ curves showing bias-stress instability. Right: One-way $C-V$ instability curves. From *Habersat D.,* et al. *"Improved Observation of SiC/SiO$_2$ Oxide Charge Traps Using MOS $C-V$." MSF., (2011) p. 367* [101].

4.2. DOS Characterization at the 4H-SiC/SiO$_2$ Interface and Interfacial Transition Layer

In the previous section, we mentioned that the observed reliability obstacles were related to the types of traps and their density of states. This chapter describes the different trap types and various improvement approaches. Furthermore, investigating the transition layer between 4H-SiC and SiO_2 plays a significant role in analyzing the spatial distribution of border traps in the oxide to extract the total trap distance from the interface, owing to the inelastic charge effect.

First analysis of 4H-SiC/SiO_2 interface properties of MOS structures formed by thermal oxidation of n-type SiC was presented by Friedrichs P. *et al.* [133]. Cooper J. A. *et al.* [3], [134] reviewed and summarized an advances in SiC MOS technologyas and measurement techniques, such as $C-V$, photo-$C-V$, hi-lo $C-V$ and AC conductance, that was adapted for investigating defects at different mostly for 6H-SiC/SiO_2 properties (see Fig. 4.8 [3]). At the same time, the interface state density for different polytypes was investigated by Afanasév V. V., Habersat D.B., *et al.* mostly by $C-V$ and $G-V$ measurements. It was demonstrated that for 4H-SiC, D_{it} is low at midgap and increases near the band edges [8], [32], [135]. The interface traps were carbon clusters at the SiC/SiO_2 interface and near-interfacial defects in the SiO_2 [32]. The most prominent Si/SiO_2 interface defects are the P_{b} centers, which can be passivated by hydrogen annealing. These centers may lead to degradation of

channel mobility by shifting the threshold voltage and causing a leakage current [32].

Various face orientations and p- and n-type substrates with distinct defect characteristics are investigated. When comparing the face density of states, the slopes of D_{it} for the $(11\bar{2}0)$ and $(03\bar{3}8)$ faces are inferior to those of the (0001) faces. Consequently, the $(11\bar{2}0)$ and $(03\bar{3}8)$ faces exhibit a lower interface state density near the conduction band edge than the (0001) surface [136], [137], [138]. Specifically, for the $(03\bar{3}8)$ orientation, the interface state density near the conduction band edge was approximately one order of magnitude lower than that of the (0001) face, as shown in Fig. 4.7 [7]. Although the $(03\bar{3}8)$ face exhibits better characteristics than the (0001) face, its fabrication is challenging [138]. The 4H-SiC/SiO_2 interface consists of an interface or border and a fixed trap, which are practically difficult to separate [39], [96], [135], [139], [140]. The trap parameters are listed in Table A.1. The interface properties depend on the three main faces ((0001) Si-face, $(000\bar{1})$ C-face, and $(11\bar{2}0)$) of 4H-SiC, on which the oxide is grown (see Fig. 4.14 [79], [83]).

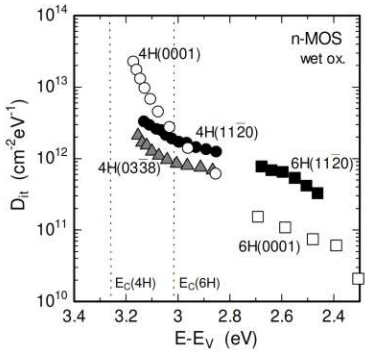


Figure 4.7.: Interface state density (D_{it}) of SiC MOS capacitors on various surface orientations. The energy position of D_{it} is plotted from the valence band edge. From *Yano H.,* et al. *"SiO_2/SiC Interface Properties on Various Surface Orientations." Mat. Res. Soc. Symp. Proc., (2003) p. K4.5.5* [7].

The trap concentration for the n-type near the conduction band was higher than that near the valence band, and had an exponential distribution. For the p-type, all traps were located close to the valence band at lower concentrations. Compared to interface defects, oxide defects are located sufficiently close to the interface, within several nanometers of the oxide. The wider bandgap of 4H-SiC permits a larger number of traps to be involved in charging and discharging kinetics. Simultaneously, when an electric field is applied, near-interface oxide traps with energy levels outside the SiC bandgap shift below the Fermi level and become charged or neutralized. In n-type SiC, the bulk Fermi level is consistently energetically positioned above the carbon cluster states; thus, no substantial interface charge is anticipated. In p-type SiC MOS structures, the positively charged carbon clusters serve as interface traps capable of capturing electrons [11]. The empty states of carbon clusters are energetically positioned well above the lower edge of the conduction band of SiC; therefore, they are unlikely to influence the electrical characteristics of the SiC/SiO_2 interface [8], [32]. Hole trapping in p-type SiC MOS structures induces positively charged interface states,

whereas electron trapping in n-type samples results in negatively charged interfaces, which appear as NBTI and PBTI shifts. The results indicate that traps can have different energy levels, either near the valence or conduction band or even beyond the bandgap, thereby intersecting the Fermi level differentially, which changes between p- and n-type substrates. This can lead to different positive and negative charges or to a neutral state, depending on the experimental conditions. Moreover, oxide traps can be located at a considerable distance from the interface in the oxide, which can also lead to different charge trap kinetics.

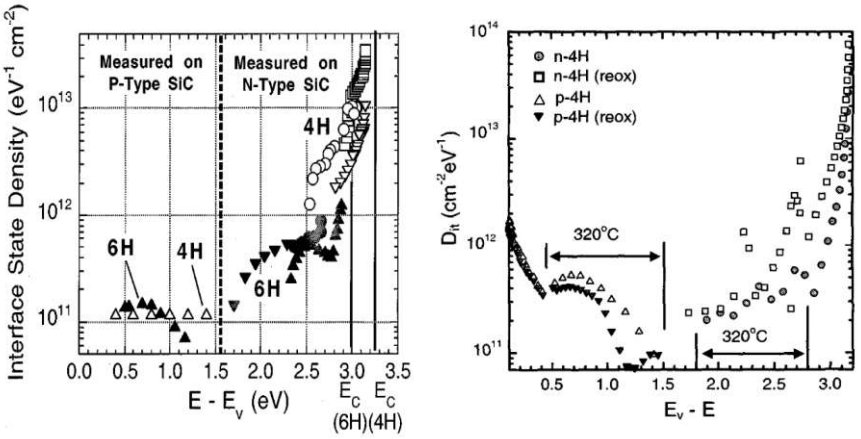


Figure 4.8.: Left: Interface state density for thermally grown SiO on 4H-SiC (open symbols) and 6H-SiC (solid symbols), as measured by the hi–lo technique (triangles) and the ac conductance technique (circles and squares). From *Cooper J.A.,* et al. *"Status and prospects for SiC power MOSFETs." TED., (2002) p. 662* [3]. Right: Interface state density for n- and p- 4H-SiC oxidized with and without post-growth reoxidation annealing. From *Cooper J.A.,* et al. *"Interface state densities near the conduction band edge in N-type 4H- and 6H-SiC." Aerospace Conf., (2000) p. 441* [141].

Deep state traps with higher energy between the conduction or valence bands (>0.3 eV) have a slow emission rate. Under typical voltage sweep settings, they maintained their initial charge states, resulting in the system not being at equilibrium and appearing as a fixed charge. This complicates the identification of the trap contributions in the measurements. Higher measurement temperatures are required to accelerate the capture and emission rates. The shallow state traps, possessing lower energy between the conduction and valence bands, result in faster capture and emission rates, enabling charge exchange and subsequent AC signal. A very small hysteresis effect was observed during the voltage sweeps at room temperature. As the temperature decreases, some shallow near-interface traps in n-type 4H-SiC MOS capacitors are unable to emit electrons during the down-voltage sweep at a specific sweep rate. These additional stored charges cause hysteresis in $C-V$ characteristics between the up- and down-voltage sweeps [34], [35], [36]. It was demonstrated that the defect concentrations were higher in p-type materials than in n-type materials with no influence on the corresponding doping species. The capture of holes is attributed to donor-like traps, whereas the electron injection results in a high concentration of acceptor-like trap states. This asymmetry in charge injection affects the magnitude of the thresh-

old voltage shift and its negative or positive direction. In addition to post-oxidation annealing, slow oxidation reduced the number of defects [33]. A highly N-doped surface leads to a reduction in the density of the interface states with an energy level of (0.1–0.6) eV below the conduction band during oxidation [37]. This indicates that implementing post-oxidation annealing in various gas atmospheres and incorporating additional technological steps to enhance the interface or oxide quality can decrease the density of the trap states, thereby potentially mitigating the BTI shift or hysteresis width. The method is described in detail in the following section.

Finally, near-interface defects (N_{it}) are typically located approximately 1-2 nm within the oxide and are influenced by the electrical field present in the oxide [36], [39].

4.2.1. Effect of Oxide Thickness on Interface Trap Density in 4H-SiC/SiO_2 Structures

D_{it} may also depend on oxide thickness. It is observed that the fixed oxide charge density (Q_{fix}) continuously increases with oxide thickness, as shown in Fig. 4.9. This proposal suggests that the fixed charges accumulated at the interface, likely because of the inhibited out-diffusion of carbon impurities during dry oxidation, which means that traps located close to the interface play a significant role in the trap kinetics [134], [142], [143].

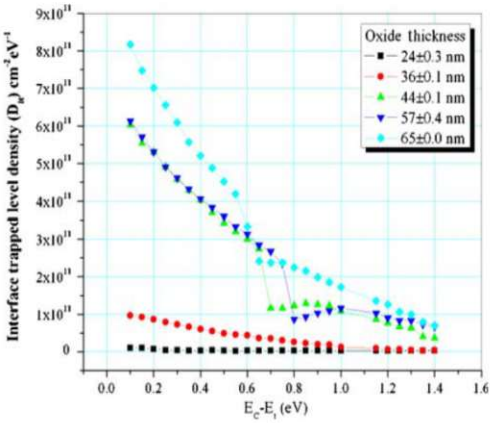


Figure 4.9.: Distribution of D_{it} within the bandgap of 4H-SiC for different oxide thicknesses. From *Gupta S.K.,* et al. *"Variation of interface trap level charge density within the bandgap of 4H-SiC with varying oxide thickness." Pramana - J Phys., (2011) p. 170* [142].

4.2.2. Trap Capture Cross Section Measurements and Analysis

Constant-capacitance deep-level transient spectroscopy (CCDLTS) and double-CCDLTS measurements were used to investigate the capture and emission kinetics of the interface states at the as-oxidized (AO) and nitrided interfaces of the 4H-SiC MOS capacitors. Measurements indicated that three distinct distributions of interface traps were present in the AO samples, whereas at least two types of interface states were present at the 4H-SiC/SiO_2 interface [116]. The three distinctly different values for the

capture cross section, ranging from 5×10^{-17} to 5×10^{-20}cm^2, clearly demonstrate that three different species of interface traps are present in the AO samples: (1) centered at $E_C-0.46$ eV, with a capture cross section of 4×10^{-17}cm^2; (2) centered at $E_C-0.24$ eV, with σ=7 $\times$ 10^{-19}cm^2; and (3) centered at $E_C-0.17$ eV with σ=4 $\times$ 10^{-20}cm^2, see Fig. 4.10. For NO with two trap distributions, one centered at $E_C-0.21$ eV, with σ=2$\times$ 10^{-20}cm^2, and the other at $E_C-0.16$ eV, with σ=8 $\times$ 10^{-21}cm^2. Using this method, the following were observed: (i) a large density of deep interface states with capture cross-sections ranging from 5×10^{-19} to 1×10^{-16}cm^2 that were fully passivated by NO annealing; (ii) near-interface states with smaller capture cross-sections ($\sim10^{-21}$cm^2) that were partially passivated by NO annealing; and (iii) trap states that remained after NO annealing, all of which had capture cross-sections ranging from 10×10^{-21} to 10×10^{-19}cm^2 [116].

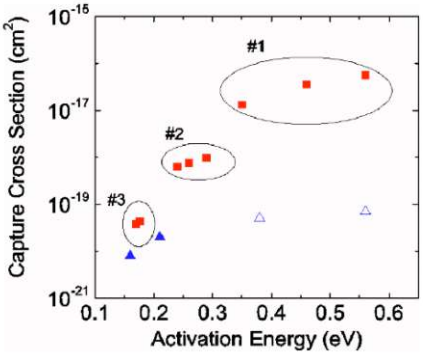


Figure 4.10.: Capture cross section and emission activation energy determined from double-CCDLTS solid symbols and CCDLTS open symbols measurements for the AO squares and the NO triangles samples. From *Chen X.D.*, et al. *"Electron capture and emission properties of interface states in thermally oxidized and NO-annealed SiO_2/4H-SiC." J. of App. Ph., (2008) p. 033701-5* [116].

4.2.3. Spatial Distribution of Traps (x_t) Near the 4H-SiC/SiO_2 Interface

To comprehensively evaluate trap kinetics, it is essential to consider not only their concentration and energy distribution but also their placement in space and the thickness of the transition region. The trap distance from the 4H-SiC interface in oxide x_t itself is a critical parameter in the non-radiative multiphonon NMP model, owing to the inelastic tunneling effect. Typically, the trapped charges are located in the oxide transition region within 1–6 nm from the SiC interface in the oxide and the same for Si- and C- faces [40], [62], [144], [145], [146], [147], [148], [149], [150], [151], [152]. Numerous defects, including those induced by carbon, oxygen, and hydrogen, have been identified as primary defects on both the substrate and the oxide sides of the interface [26]. The distance of the trap from the interface affects both capture and emission times. The deepest trap exhibited the longest duration and could be activated by increasing temperature [90], [147], [153], [154].

The difference between the Si/SiO_2 and SiC/SiO_2 interfaces was investigated using Z-contrast images from scanning transmission electron microscopy (STEM) with a

parallel electron energy loss spectroscopy (EELS) system. It was shown that away from the interface step, the Si/SiO2 interface appears very abrupt compared with SiC/SiO_2 where a transition region with 1-2 atomic layers thick (∼2 nm) is observed (see Fig. 4.11 [22]. The different trap types at the 4H-SiC interface are presented in Table A.1.

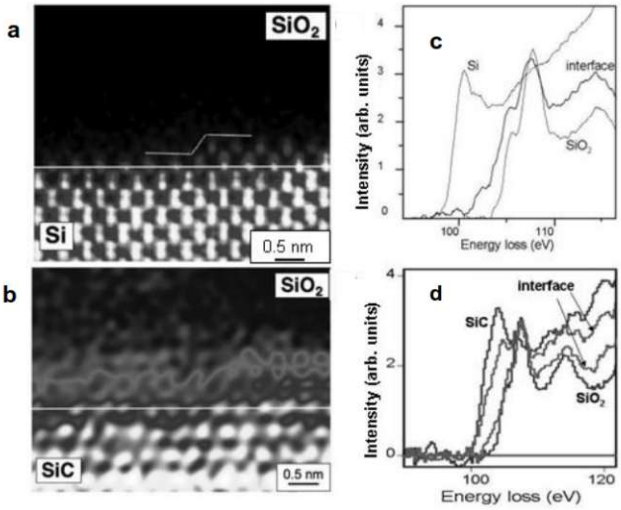


Figure 4.11.: Z-contrast images and EELS from a Si/SiO_2 interface (a,c) and a $4H\text{-}SiC/SiO_2$ interface (b,d). From *Pantelides S.T.,* et al. *"Si/SiO_2 and SiC/SiO_2 Interfaces for MOSFETs – Challenges and Advances." MSF., (2006) p. 938* [22].

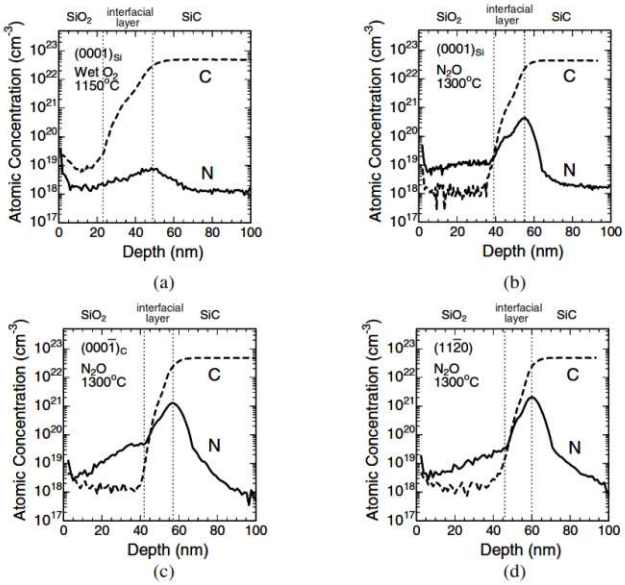


Figure 4.12.: N and C atom distributions for MOS structures on (a) O_2(wet)-oxidized 4H-SiC(0001), (b) N_2O-oxidized 4H-SiC(0001), (c) N_2O-oxidized 4H-SiC(000$\bar{1}$), and (d) N_2O-oxidized 4H-SiC(11$\bar{2}$0). From *Kimoto T.,* et al. *"MOS Interface Properties and MOSFET Performance on 4H-SiC0001 and Non-Basal Faces Processed by N_2O Oxidation." Mat. Res. Soc. Symp. Proc., (2004) p. J8.2.5* [79], [83].

To investigate the transition region in SiO_2/4H-SiC with different faces under various growth conditions, secondary ion mass spectrometry (SIMS) measurements were performed to investigate the distribution of N and C atoms near the interface and in the oxide (see Fig. 4.12 [79]).

SIMS measurements showed that a higher interfacial transition layer (SiC_xO_y) exists between SiO_2 and SiC and has different thicknesses owing to the different faces (see Fig. 4.12 with a typical oxide thickness of 70 nm). The thickness of the transition layer that may propagate up to 26 nm in the oxide layer depends on faces and decreases with POA (16 nm for (0001), 14 nm for $(000\bar{1})$, 13 nm for $(11\bar{2}0)$); see Fig. 4.12 [79]. Evidently, the higher transition region may depend on the oxidation technology and the thickness of the interfacial transition layer can be reduced by N_2O oxidation [83]. Using EELS measurements, it can be seen that the N signal is approximately centered in the transition region with a slight tail towards the SiO_2 interface. The full width of border traps of (0001) face is 2.1 ± 0.4 nm for $(11\bar{2}l)$ is 1.5 ± 0.4 nm with a typical oxide thickness of 42 nm.

4.2.4. Techniques for Enhancing and Controlling the Interfacial Properties of SiC/SiO_2 Structures

Simultaneously, in conjunction with the investigation of traps at the SiC/SiO_2 interface and their influence on device reliability, improved methods designed to decrease the number of traps or mitigate their impact have been introduced. One of the most widely used techniques is post-oxidation annealing (POA) with different parameters, particularly in various gases and their mixtures, to passivate dangling bonds at the interface. For example, the POA in NO reduces ΔV_{th} bias instability for a positive gate bias stress [101], [155]. All methods are listed in Table A.1. The function of nitrogen is to pair with carbon, thereby completely eliminating isolated carbon-induced defects and reducing the existing clusters to a lower quantity of carbon atoms. Modeling indicated that the isolated carbon atoms included single carbon atoms situated deep within the gap and clusters positioned near the conduction band edge [116]. D_{it} depends on the depth of the oxidized layer and the implanted N concentration, and the minimum value is $\approx 10^{10}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ in the investigated energy range (E_C−(0.1 to 0.6eV)). The flat-band voltage increases to negative levels, which is attributed to the generation of fixed positive charges. A thin surface-adjacent layer, which is extensively N-doped during chemical vapor deposition growth, results in a decrease in D_{it} only along the conduction band edge [37]. The implantation of nitrogen into n-type 4H-SiC (Si-/C-face) MOS capacitors before oxidation significantly decreased D_{it} compared with the non-implanted reference samples. Conversely, in p-type 4H-SiC (Si-face) MOS capacitors, the interface trap density is elevated. In p-type 4H-SiC (C-face) MOS capacitors, the presence of a high concentration of energetically deep interface states makes it difficult to determine the D_{it}. The incorporation of implanted N has been suggested to reduce the lattice mismatch between the nitrided oxide and SiC, resulting in a reduced density of the near interface traps (NITs). Indirect studies imply that residual C clusters may contribute to higher interface state densities and

passivation difficulties. Carbon clusters often have a higher density than dangling bonds [39]. Annealing with NO and N on the Si-face and C-face SiC interfaces led to different improvements. Excess carbon was not observed after annealing in NO on the Si face under the same conditions as in the C-face (2 at 1175 °C). This disparity may be linked to the higher quantity of extra carbon identified in the C-face samples compared to the Si-face samples [144]. In such situations, the Coulomb interaction between an electron and the N-induced positive charge in the C-cluster results in a downshift of the C-related interface states towards the valence band edge, thereby causing a reduction in the interface trap density in the top half of the SiC band gap [38], [155].

The most commonly used POA process to reduce trap density is nitridation of the interface using nitric oxide (NO) or nitrous oxide (N_2O) [156]. Nitrogen saturates Si dangling bonds and replaces oxygen in the strained Si-O-Si bonds [157]. The POA in NO allows N to compensate for the Si-C dangling bonds on the carbide side of the interface, resulting in Si-C-N environments and defects on the oxide side of the interface through the formation of Si-O-N structures. Therefore, NO has become the industry standard for compensating interface defects at the 4H-SiC/SiO_2 C-face interface [61]. Oxidation in an ozone gas atmosphere with O_3 molecules thermally dissociating into atomic oxygen resulted in a substantial decrease in D_{it}. However, passivation of the interface states can be achieved through nitridation, which involves oxidation in a nitrogen-containing gas mixture [26].

Thermal annealing using $POCl_3$ significantly reduced the interface state density. This POA method indicated a decrease in NIT compared to NO annealing in the n-type (0001) 4H-SiC epitaxial layer [158], [159].

Argon and hydrogen POA at various temperatures showed that the interface state density D_{it} decreased as the temperature of the hydrogen POA increased, which improved the D_{it} and reliability of the gate oxide [160]. The H_2 treatment reduced the negative charges at the interface (see Fig. 4.13 [160], [161]).

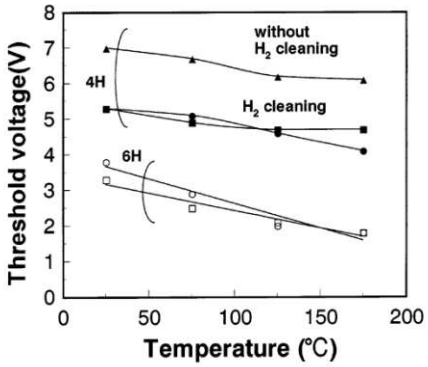


Figure 4.13.: The temperature dependence of field effect mobility for 6H-SiC and 4H-SiC. The threshold voltage was extracted from $\sqrt{I_D} - V_D$ plot for the gate-drain shorted configuration. From *Ueno K.,* et al. *"H_2 surface treatment for gate-oxidation of SiC metal-oxide-semiconductor field effect transisitsors." Mat. Science and Eng.: B, (1999) p. 474* [161].

Another method is to use dry oxidation at 1150 °C and 3 h or wet oxidation at 2 h for the 4H-SiC p-type epilayers. The fixed charge density (Q_f) is calculated using the following equation:

$$Q_f = \frac{C_{ox}}{q}\{V_{th} - V_{th,theory}\} \tag{4.1}$$

Where C_{ox}, q, $V_{th,theory}$ are the capacitance of the gate oxide, electrical charge, and theoretical threshold voltage, respectively. It has been shown that fixed charges include both real fixed charges and electrons trapped at interface states. In this case, the fixed charges are negative. During wet oxidation, the channel mobility is lower and the positive threshold voltage is higher (5∼6 cm^2/Vs and 3∼8 V). This may be explained by acceptor-like charged interface states that are part of the fixed charges generated by wet oxidation (-34.9×10^{11} cm^{-2} in wet conditions and -10.1×10^{11} cm^{-2} under dry oxidation conditions) [39], [88].

N_2O oxidation can significantly reduce D_{it} for all the three faces Fig. 4.14. The D_{it} values at $E_C-0.2$ eV were approximately $6\times10^{11}cm^{-2}eV^{-1}$ for (0001), $3\times10^{11}cm^{-2}eV^{-1}$ for $(000\bar{1})$, and $3\times10^{11}cm^{-2}eV^{-1}$ for $(11\bar{2}0)$. This indicates the important role of hydrogen in passivating the interface states in 4H-SiC MOS structures and reducing reliability issues [79], [162], [163], [164].

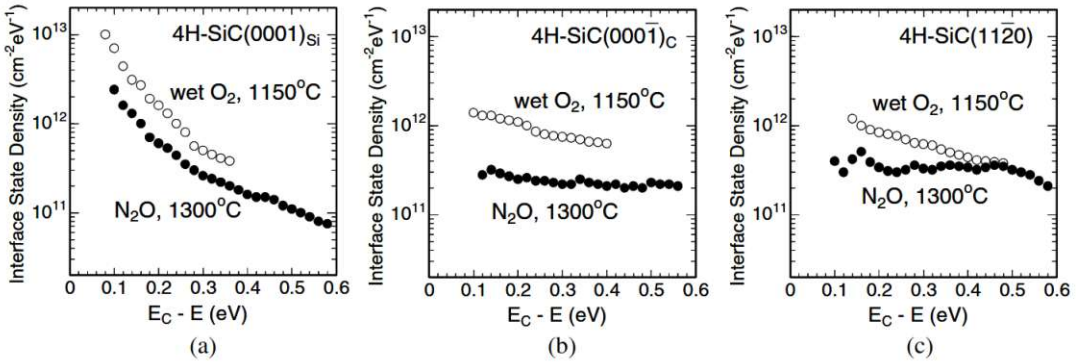


Figure 4.14.: D_{it} distributions of 4H-SiC MOS structures fabricated on (a) (0001), (b) $(11\bar{2}0)$, and (c) $(11\bar{2}0)$ faces. From *Kimoto T.*, et al. *"MOS Interface Properties and MOSFET Performance on 4H-SiC0001 and Non-Basal Faces Processed by N_2O Oxidation." Mat. Res. Soc. Symp. Proc, (2004) p. J8.2.2* [79].

The influence of four different POA (standard NO, NO annealing with 30% higher NO flow (NO+30%), 30% lower flow (NO-30%), and N_2 carrier gas only) on the BTI, hysteresis width, and subthreshold slope at $I_d - V_{gs}$ and $C - V$ of the trench 4H-SiC MOSFETs is shown in Fig. 4.15.

With NO anneal approximately 30% the hysteresis width appears to be slightly smaller, and using N_2 the subthreshold slope increases (see Fig. 4.15). This is because the NO POA reduced the interface traps at $E_C-0.13$ eV. In $C - V$ measurements, the curve with N_2 POA is stretched out more along the gate voltage. Significant accumulation cannot be achieved owing to the capture of charge carriers, which are

released only at a slow rate [162]. Hysteresis width reduction and channel mobility improvement may be achieved using either NH_3 or NO+NH_3 instead of NO. [60] The differences in the trap system before and after the POR can be observed to influence the shapes of the $I_d - V_{gs}$ and $C - V$ curves [60], [162].

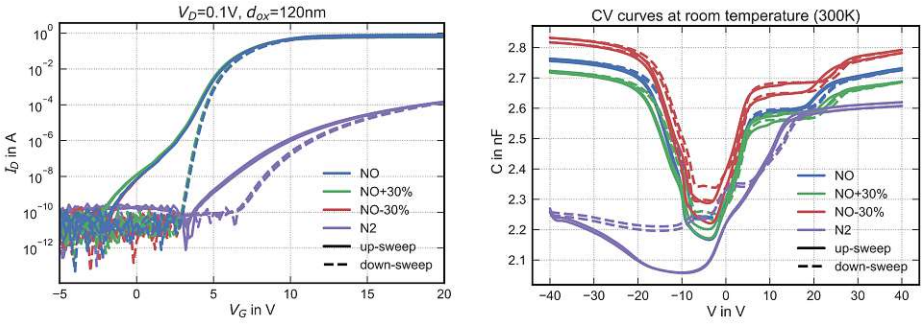


Figure 4.15.: Left: $I_d - V_{gs}$ swept from accumulation to inversion to accumulation for devices with 120 nm gate oxide and different POA. Right: $C - V$ measurements for processes with 120 nm gate oxide and different POA. The curves were taken at room temperature using a frequency of 100 kHz. The upsweep was measured first. Th. From *Berens J. "Cryogenic characterization of 4H-SiC high power MOSFET." Master Thesis. RWTH Aachen University, (2018) pp. 51-53* [162].

4.3. Hysteresis in the $C - V$ curve of MOSFETs

Interpreting capacitance-voltage ($C-V$) and conductance-voltage ($G-V$) impedance data at varying frequencies involves considerable difficulties. The observed phenomena were the stretch-out effect and hysteresis during the down-gate voltage sweep, which resulted from the charging and discharging of traps when a fast AC signal was applied at each gate voltage step. Lateral 4H-SiC MOSFETs generally exhibit a significant interface state density close to the conduction band, which is attributed to the rough and defective SiC/SiO_2 interface. Trench 4H-SiC MOSFETs have the potential to deliver enhanced performance characterized by higher channel mobility and lower R_{on}. However, they may also exhibit more complex or deeper traps because of varying oxidation and fabrication conditions. Simultaneously, the examination of trap distributions within the channel of vertical trenches leads to the appearance of non-uniform electric fields and charge distributions, as well as a complex doping profile. This adds complexity to the modeling and interpretation of $C - V$ data, particularly when it comes to differentiating between the interface and bulk traps. The sidewalls of the trench near the bottom corner, which is a hotspot for reliability issues, present challenges for $C-V$ measurements. Typically, these measurements cannot spatially resolve the location of the traps, making it difficult to distinguish the contributions from each region. The evaluation and modeling of trap kinetics in trench devices through impedance measurements involves two iterations. The first step was to obtain an appropriate quasi-static $C - V$ curve, followed by fitting a complex trap system.

The $C-V$ assessments demonstrated notable sensitivity to the slow defects present

within the oxide close to the interface during the up and down sweeps. At every point in the gate voltage, the defect states close to the Fermi level capture a charge and hold onto it during the down sweep [99], [100]. The width of the hysteresis is influenced by the charged defects, which exhibit short emission times. The measurements indicate that the hysteresis and stretching of the lateral $C-V$ curves are predominantly affected by three specific types of traps. Initially, the acceptor-like defects at the interface located near the conduction band exhibited a response to the small-signal frequency. The observed increase in trapped negative charges with increasing gate voltage can be explained by the existence of slower acceptor-like border traps, which have trap levels located close to the conduction band and within the midband gap region [99], [100]. The density of states for trench devices shows a clear structure: acceptor-like defects are located near the conduction band at lower concentrations, whereas donor-like defects are located closer to the valence band. Furthermore, donor-like border traps were observed just beneath the mid-gap. In conclusion, we propose that both devices exhibit consistent positive charge.

Understanding the various trap types and their influence on reliability issues can enable us to manage and reduce unnecessary effects. State-of-the-art technology in computer-aided design (TCAD) provides a powerful tool for investigating device behavior, calibrating simulations with measured data by utilizing appropriate trap parameters, and optimizing the device for desired targets. In the subsequent sections, the influence of interface traps on the capacitance-voltage ($C-V$) curves is investigated by applying the Shockley–Read–Hall (SRH) theory [100], [104], [165], [166] and [167], [168].

The results from our experiments and the calibrated model demonstrate that interface traps situated close to the valence or conduction bands, characterized by small capture and emission barriers, display fast behavior. In contrast, border traps positioned near the mid-bandgap exhibit slower dynamics. Despite numerous efforts to enhance the comprehension of $C-V$ measurements in silicon carbide (SiC) devices, a comprehensive simulation of a lateral 4H-SiC MOSFET, calibrated and validated with measurement data across various small-signal frequencies and temperatures, remains insufficient [99], [100].

4.3.1. Hysteresis in the $C-V$ Characteristics of Lateral and Trench MOSFETs

In our study, we utilized lateral 4H-SiC nMOSFETs (refer to Fig. 1.2a). For the measurements of the $C-V$ and conductance-voltage ($G-V$) curves, see Fig. 3.3 [103], [104]. Fig. 4.16 shows $C-V$ and $G-V$ curves measured at various temperatures and frequencies. The measured impedance was corrected for parasitic impedance [78]. The horizontal line indicates the reference capacitance ($C_{\mathrm{cut}} = 4.3 \times 10^{-12}\,\mathrm{F}$) at which we define the hysteresis widths $\Delta V_{\mathrm{H}}^{\mathrm{d-a}}$ and $\Delta V_{\mathrm{H}}^{\mathrm{d-i}}$ between the up and down sweeps respectively. One can see in Fig. 4.16a the $C-V$ curves are shifted by ΔV towards lower V_{gs} with increasing temperatures [100].

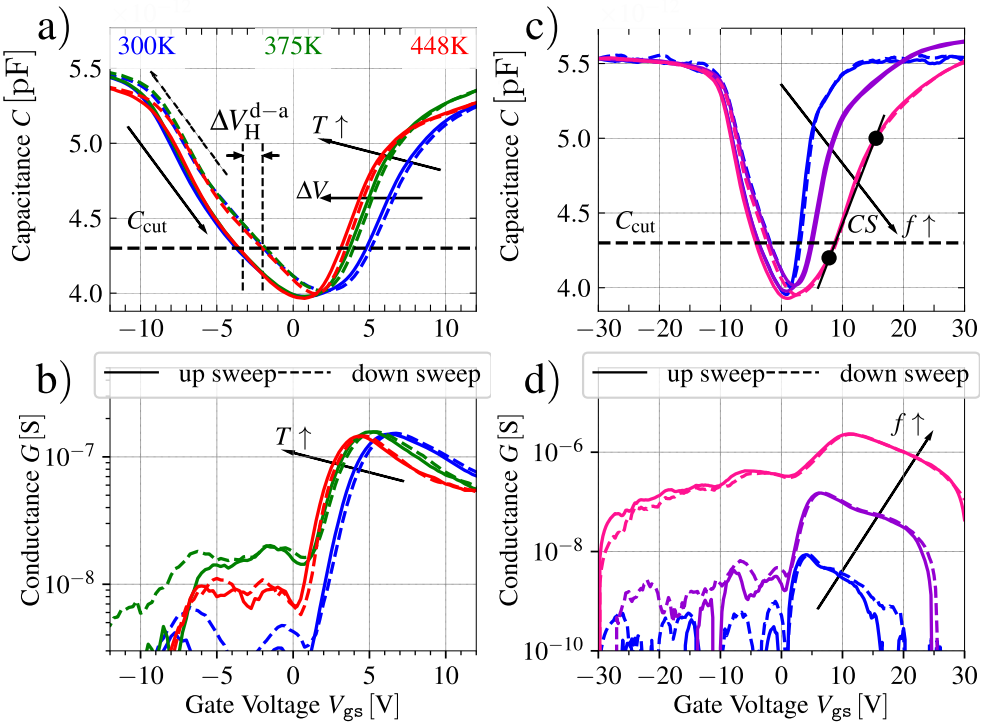


Figure 4.16.: a) $C-V$ characteristics and b) conductance of a lateral 4H-SiC MOSFET at 64 kHz and 300 K, 373 K, and 448 K. c) $C-V$ characteristics, and d) conductance of a lateral 4H-SiC MOSFET at 300 K and frequency 4 kHz, 64 kHz, and 1024 kHz. The horizontal line indicates the reference capacitance ($C_{cut} = 4.3 \times 10^{-12}$ F) at which we defined the hysteresis widths ΔV_H^{d-a} and ΔV_H^{d-i} between the up and down sweeps respectively. Two reference capacitances are used for extracting the capacitance swing (CS) [100].

The peak of conductance shifts towards a lower gate voltage by 3 V with increasing temperature, as shown in Fig. 4.16b and the hysteresis width in the depletion to accumulation region ΔV_H^{d-a} is wider than in the depletion to inversion region ΔV_H^{d-i}, whereby they slightly decrease with increasing temperature. We attribute this behavior to slow and border traps located a few nanometers away from the SiC/SiO_2 interface [100], [169], [170] (see Fig. 1.2a). Fig. 4.16c shows that the $C-V$ curves are shifted towards higher V_{gs} values when the frequency is increased. A frequency-dependent peak in the conductance at approximately 2–8 V indicates the presence of interface states, as shown in Fig. 4.16, respectively. Two reference capacitances are used to extract the capacitance swing ($CS = \partial V_{gs}/\partial C$) [100].

The $C-V$ curves of planar and trench MOSFETs exhibit distinct shapes influenced by their geometry [162], [171], [172], [173], [174] and different values owing to the oxide thickness, as shown in Fig. 4.17. The planar device exhibited a lower hysteresis, with a greater hysteresis noted after positive stress than before stress. In contrast, the trench device displays a larger hysteresis from depletion to accumulation region, which narrows following a positive stress [175], [176], [177], [178], [179].

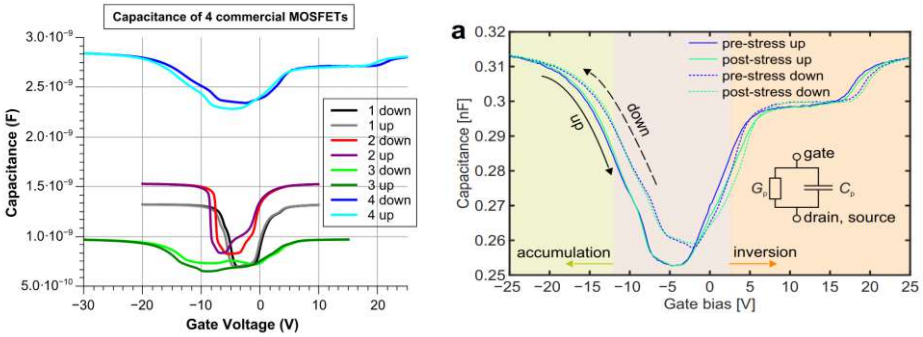


Figure 4.17.: Left: example of the measured input capacitance C_{iss} of 4 commercial SiC nMOSFET (1,2 - planar, 3,4 trench) as a function of bias conditions. It should be noted that there is a wide discrepancy between the capacitance characteristics, and that the sweep direction has a strong effect. From *Asllani B.,* et al. *"V_{th}-Hysteresis and Interface States Characterisation in SiC Power MOSFETs with Planar and Trench Gate." IRPS, (2019) p. 3* [175]. Right: Example of the capacitance C_p from the equivalent circuit (see inset in a) that was used to interpret the measured impedance, as shown for a stress frequency of 500 kHz. From *Feil M. W.,* et al. *"On the Frequency Dependence of the Gate Switching Instability in Silicon Carbide MOSFETs." MSF, (2023) p. 113* [176].

4.4. Hysteresis in the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ Characteristics of MOSFETs

The first hysteresis in room-temperature transfer characteristics between the up- and down-gate voltage sweeps in n-channel depletion/accumulation-mode 4H–SiC MOSFETs was reported by Chatty K. *et al.* [180]. The transfer characteristics demonstrate a parallel V_{th} shift towards negative voltages, which is dependent upon the initial gate voltage and the sweep direction. Additionally, at high temperatures, the hysteresis between the up- and down-gate voltage sweeps decreased [180]. This temperature-dependent behavior is consistent with the assumption proposed by Pensl and Afanasév V.V. *et al.* [36]. The effect of charge kinetics on the positive starting gate voltages was explained by acceptor traps near the conduction band, which became negatively charged and shifted towards positive gate voltages. In the case of a negative starting voltage, the donor traps near the valence band edge are positively charged and shift toward lower gate voltages. Mobile ions are not involved in the charge exchange and do not contribute to the hysteresis width at room temperature [180], [181]. In addition, in planar 4H-SiC nMOSFETs, the effective channel mobility strongly depends on the 4H-SiC faces ((0001), (000$\bar{1}$), and (11$\bar{2}$0) are 26, 43, and 78 $\mathrm{cm^2V^{-1}s^{-1}}$, respectively) [77], [79].

In some measurement cases, the hysteresis (calculated as the difference between the positive and negative stresses) increased with the temperature. In this case, at T>70 °C, the trapped carriers can penetrate further into the oxide at elevated positive stresses, thereby increasing V_{th} [182]. A significant contribution to the examination of V_{th} instability and hysteresis in 4H-SiC MOSFET characteristics was made by A. J. Lelis *et al.* [40]. Typical $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves are shown in Fig. 4.18 [40]. It was

demonstrated that during fast $I_d - V_{gs}$ measurements, V_{th} shifted to higher positive values under a positive bias and to more negative values under a negative bias. These measurements enabled the differentiation of positive and negative V_{th} shifts and revealed that the majority of the drain current deterioration occurs under a positive bias. Throughout the gate voltage sweep, the hysteresis width ΔV_{th} expands with the stress bias in both directions; however, it is more pronounced under a negative bias stress. It was hypothesized that two distinct physical mechanisms were implicated because of the amphoteric interface traps, with acceptor-like types in the top half and donor-like types in the lower half of the bandgap [183]. This investigation did not entail any temperature variations [12]. The V_{th} instability increased with the gate bias stress time. The electrons tunnel to and from traps that are approximately uniformly scattered within a distance of 5 nm from the SiC/SiO_2 interface [40], [89], [135].

Furthermore, it was shown that the measurement time is a very important factor that influences the magnitude of V_{th} instability. Simultaneously, the threshold voltage decreased with increasing temperature. Instability at room temperature was the most significant for three samples (DMOSFET B, C, and D), and anomalously increased for sample A. Fig. 4.19, left. At room temperature, the V_{th} instability increases with stress time, as shown in Fig. 4.19, right. The temperature-dependent results are affected by the manufacturing process and may differ from device to device. The hysteresis width for lateral 4H-SiC MOSFETs exhibits varying temperature dependencies at different points of application (POA). ΔV_{th} increases with aging from 50 °C and exhibits a smaller value when NO is utilized compared to O_2 and N_2O, which is attributed to a lower D_{it}. The distribution exhibited two distinct peaks, with the low-energy peak being particularly influenced by nitrogen-containing atmospheres during post-oxidation annealing [184], [185], [186], [187].

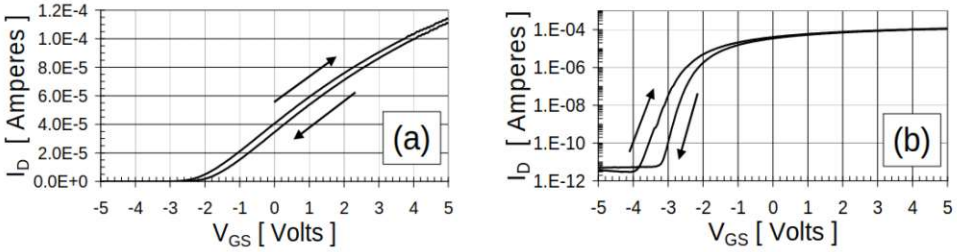


Figure 4.18.: Typical $I_d - V_{gs}$ curves showing bias stress-induced instability, with drain current plotted on both (a) linear, on the left, and (b) logarithmic, on the right, scales. From *Lelis A. J.,* et al. *"Bias Stress-Induced Threshold-Voltage Instability of SiC MOSFETs." MSF, (2006) p. 1318* [40].

A positive average shift suggests charge tunneling into and out of near-interfacial oxide traps. Conversely, a negative average shift indicates the existence of another process. The action of this mechanism corresponds to the movement of mobile ions within the oxide owing to the applied gate-bias stresses. Under a positive gate voltage shift and high temperature, these positively charged ions become mobile and migrate

towards the SiC/SiO_2 interface, causing a decrease in the threshold voltage, an increase in the channel carrier concentration, and consequently, the drain current [11], [121], [122], [164], [188].

Slow $I_d - V_{gs}$ measurements, applying approximately 1 s or longer, indicate a threshold voltage instability of approximately 0.25–0.33 V. Faster $I_d - V_{gs}$ measurements indicated a considerably wider range of instability than previously discussed, even during short stress intervals. This outcome aligns with charge tunneling into the oxide traps that are spatially distributed in the near-interfacial region. A tunneling process results in a linear-with-log-time bias stress response, whereby approximately 50% of the threshold voltage instability appears within the initial microseconds of a 1 s bias stress. The measurement time was significantly affected by the bias during the sweep. A longer measurement time enhances the observable effects of the initial bias stress [164]. This instability may be due to more than one trap type, where E' centers are the dominant oxide trap [97], [189].

The subthreshold drain current hysteresis $\Delta V_{th,sub}$ during the gate voltage up and down sweeps was analyzed for planar 4H-SiC Si-face (0001) and trench a-face $(11\bar{2}0)$ MOSFETs by Rescher G. *et al.* [190]. The a-face devices exhibited more pronounced hysteresis, which was attributed to an increased border state density near the midgap. Additionally, they demonstrated a higher mobility resulting from a reduced border state density near the conduction band edge of 4H-SiC [68], [190]. Both devices exhibited opposite temperature dependences with respect to the hysteresis width. At elevated temperatures, planar MOSFETs demonstrate a decrease in hysteresis width, whereas trench devices display an opposing trend. These results must be considered when operating trench devices because they are influenced by the starting gate voltage and temperature conditions. [191], [192]

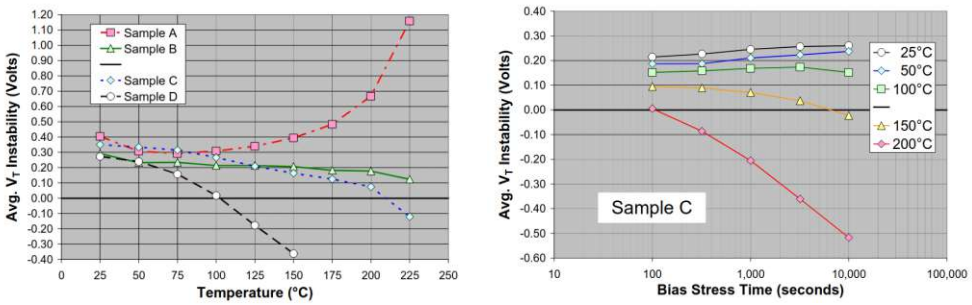


Figure 4.19.: Left: Average threshold voltage instability effect as a function of temperature for several different samples fairly representative of the state-of-the-art. Right: Avg. instability of Sample C as a function of temperature and bias-stress time. The instability was calculated by alternately applying a positive bias stress, followed by a negative bias stress. Bias stress was applied each time for three minutes with the full cycle of measurements repeated three times and averaged. From *Lelis A. J.,* et al. *"Temperature-Dependence of SiC MOSFET Threshold-Voltage Instability." MSF, (2009) pp. 809-810* [122].

Finally, planar devices have a more significant negative V_{th} shift during the OFF

blocking state, which may lead to a higher drain leakage current compared with the conventional $I_d - V_{gs}$ curves. The positive V_{th} shift in the ON state slightly increases R_{dson} which is acceptable for power converter applications [146], [184], [193], [194]. An additional significant process resulting from charge trap dynamics is the reduction in the effective channel mobility caused by Coulomb scattering and the decreasing number of free carriers [151], [189], [195].

4.4.1. Hysteresis in the $I_d - V_{gs}$ Characteristics of Lateral MOSFETs at Various Temperature

The transfer characteristics or $I_d - V_{gs}$ were utilized to investigate the relationship between the drain current and the gate voltage sweep while maintaining a constant drain voltage bias. This measurement determined the device conditions at each time step. It is recommended that the gate voltage be swept as quickly as possible while maintaining a constant time step to suppress the nonlinear effects. It is important to analyze the influence of traps with shorter capture and emission times to observe a significant threshold voltage shift. The hysteresis measurement method was used to obtain the $I_d - V_{gs}$ curves of the lateral 4H-SiC MOSFET over a broad temperature range as shown in Fig. 4.20. This device demonstrated notable subthreshold hysteresis and a threshold voltage shift of up to 11 V towards higher gate voltages, particularly at lower temperatures. This behavior is attributed to the high border trap concentration near the SiC/SiO_2 interface, which can capture and emit electrons and influence the shift. We suppose that at high temperatures, the traps become neutralized, which decreases the threshold voltage shift. Furthermore, we were unable to detect a zero-temperature coefficient (ZTC) point, indicating a positive temperature coefficient.

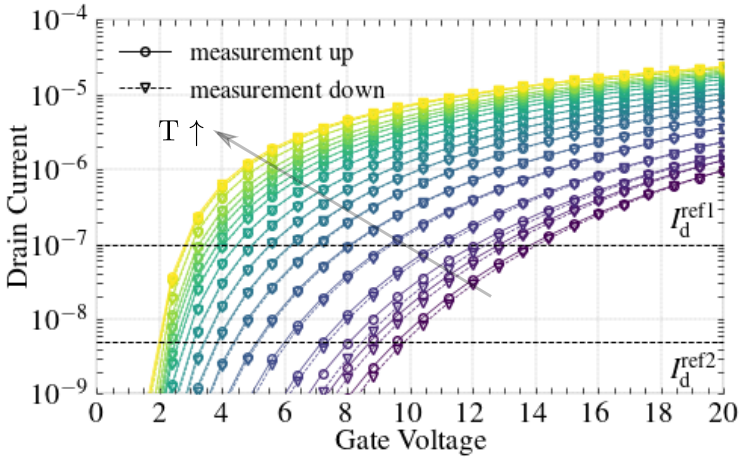


Figure 4.20.: Measured $I_d - V_{gs}$ curves over a wide temperature range of 110 to 600 K using up/down V_{gs} sweeps. Two reference drain currents $I_d^{ref1,2}$ were used to determine two hysteresis widths ΔV_{H1} and ΔV_{H2} as the difference in the corresponding voltages during the up and down V_{gs} sweeps.

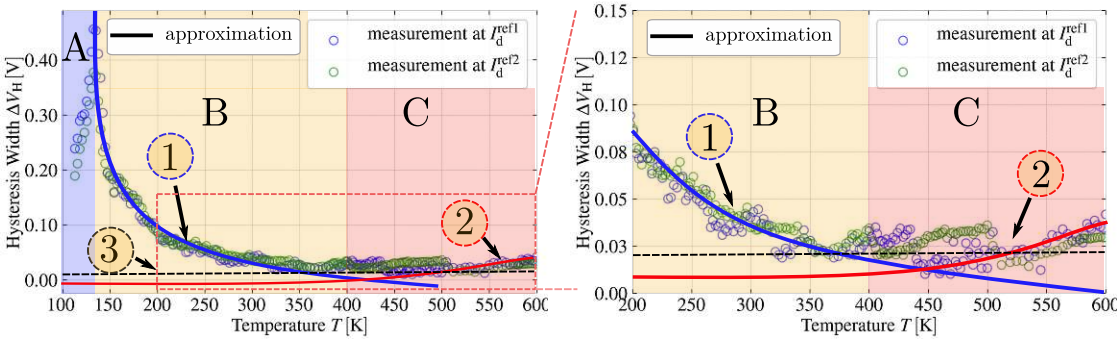


Figure 4.21.: Extracted measured hysteresis widths $\Delta V_{H1,2}$ using two different reference drain current levels (I_d^{ref1} red circles, I_d^{ref2}) blue circles. The red and blue solid lines represent the possible approximations based on several trap types. Three hysteresis behaviors were observed: A, when the hysteresis width was small and increased with temperature; B, the typical hysteresis width with increasing temperature; and C, the small anomalous hysteresis width increased with increasing temperature. We assume that three possible trap candidates may explain this hysteresis behavior over a given temperature range.

The hysteresis width across a broad temperature range was calculated as the difference between the down- and up-threshold voltages at the two reference drain currents, as illustrated in Fig. 4.21.

Three distinct regions of hysteresis width behavior with respect to temperature were identified. In Region A hysteresis width increased with increasing temperature. It is assumed that all carriers are in a frozen state and that the capture and emission times are too long for any charge to be released into the channel within an application-relevant time frame. Simultaneously, the BTI was notably elevated, suggesting that the traps effectively maintained their initial charges. As the temperature increased, there was a tendency to capture charges and subsequently emit them; however, the capture process remained the dominant phenomenon. Upon reaching 150 K during normal operation, the hysteresis width diminishes with increasing temperature alongside the BTI, suggesting that at elevated temperatures, the emission time increases and the traps are likely to neutralize. In regime C, from 400 K, we observed an anomalously weak increase in the hysteresis width, suggesting the involvement of a different type of trap that is activated at elevated temperatures. Consequently, we can hypothesize and estimate this curve by using three potential types of border traps. Type (1) is primarily responsible for region B. Type (2) is associated with an increase in the hysteresis width with temperature in region C, whereas type (3) is primarily responsible for a constant hysteresis width that remains unaffected by temperature, as shown in Fig. 4.21. The origin of all these trap types will be discussed in Section 6.2. The behavior of the hysteresis width is dependent on the POA, resulting in varying D_{it} values for lateral MOSFETs, as illustrated in Fig. 4.22 [184].

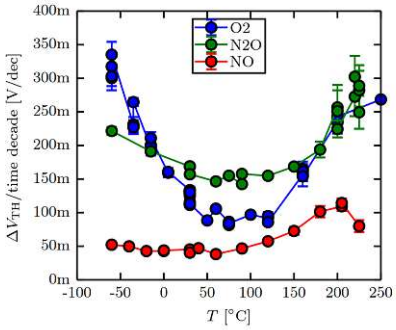


Figure 4.22.: Temperature dependence of the ΔV_{th} dynamic at $V_{\mathrm{gs}} = 10\,\mathrm{V}$. Owing to the specific temperature dependence, the instability may either be enhanced or reduced for different atmospheres during the POA. Nitric oxide (NO), however, leads to a general decrease of the instability effect. From *Pobegen. G.,* et al. *"Instabilities of SiC MOSFETs during use conditions and following bias temperature stress." IRPS, (2015) p. 6C.6.3* [184].

4.4.2. Hysteresis in the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ Characteristics of Lateral and Trench MOSFETs at Various Sweeps

The ΔV_{th} hysteresis plays a crucial role in the gate driver design of SiC MOSFETs, particularly with regard to the dynamic characteristics when driven by varying the OFF-state starting voltage ($V_{\mathrm{G}}^{\mathrm{OFF}}$). The hysteresis width shape of $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves varies between the planar and trench devices, which means that different trap systems are involved in the trap kinetics. A smaller $V_{\mathrm{G}}^{\mathrm{OFF}}$ results in an increasing in ΔV_{th} when the device turn-on, as illustrated in Fig. 4.23 [10]. The lower the start voltage of the up-sweep and the lower the drain current, the greater is the hysteresis observed between the up-sweep and down-sweep, resulting in a reduced subthreshold swing.

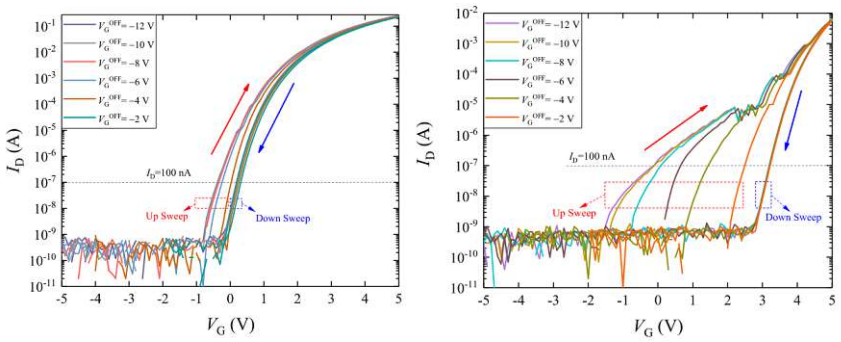


Figure 4.23.: Example of the ΔV_{H} hysteresis of SiC MOSFETs. Left: D-MOSFET (planar). Right: AT-MOSFET (Asymmetric trench) at various sweeps. From *Cai. Y.,* et al. *"Effect of Threshold Voltage Hysteresis on Switching Characteristics of Silicon Carbide MOSFETs." TED, (2021) p. 5016* [10].

Compared with planar devices, the up-sweep curves of the trench MOSFET exhibited wider hysteresis and mostly equal V_{th} values at the down voltage sweep. The interface states exhibit a positive charge when a negative gate voltage is applied and return to a neutral state under a positive gate bias. This provides definitive evidence that hysteresis is induced by holes trapped at the interface. The amount of time required for charging and neutralization depends on the free carrier densities in both the off and on states, which are influenced by the gate bias in these states [112], [178], [192], [196], [197].

Fig. 4.24 shows the V_{T} hysteresis for the trench and the planar SiC (DMOSFET) devices under negative-bias overstress (NBO) (typically from µs to ks). Hysteresis was measured when applying $V_{\mathrm{GS(low)}}$ and $V_{\mathrm{GS(high)}}$, hysteresis was measured. In addition, the NBO gate stress increased during the measurement sequence. The surface potential accumulated at higher negative gate biases, increasing the number of holes in the channel. This may be responsible for the dramatic increase in the V_{T} hysteresis of the trench-geometry devices and, consequently, their high NBO sensitivity. One clear distinction as to why V_{T} is higher in trench devices is that, unlike the Si-face of planar DMOSFETs, the gate oxide for trench devices is generated on the a-face, which leads to a different trap type and distribution [198].

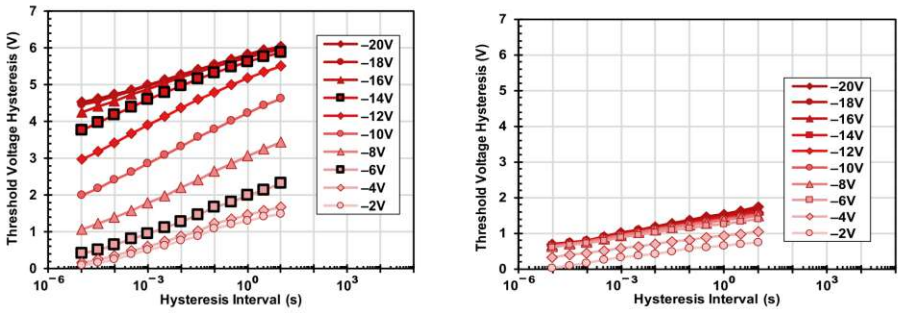


Figure 4.24.: Left: Effect of negative gate bias, $V_{\mathrm{GS(low)}}$, on the magnitude of V_{T} hysteresis observed in a SiC MOSFET with a trench design. $V_{\mathrm{GS(high)}}$ was kept constant at +22 V. Right: A much smaller V_{T} hysteresis effect owing to negative-bias overstress (NBO) is observed in a planar SiC DMOSFET. From *Lelis A. J.*, et al. *"Effect of Dynamic Threshold-Voltage Instability on Dynamic ON-State Resistance in SiC MOSFETs." TED, (2022) pp. 5651-5652* [198].

4.5. Gate Switching Instability and Hysteresis

In 2017, Okunishi *et al.* [107] used fast drain current measurements to investigate the positive bias temperature instability (PBTI) in 4H-SiC DMOSFETs. The results indicate that the V_{th} shift is a saturation phenomenon and that the maximum V_{th} shift can be predicted using an electron capture and emission model. Compared with the conventional fast $I_{\mathrm{d}} - V_{\mathrm{gs}}$ method, the fast I_{d} method estimates unexpectedly larger V_{th} shifts [107]. Subsequently, Puschkarsky *et al.* introduced a measurement technique that facilitates the determination of the real V_{th} of trench MOSFETs during application-relevant bipolar AC gate stress [56], [59], [91]. The threshold voltage hys-

teresis ΔV_{th} introduced by an application-like bipolar AC gate signal with a frequency of 50kHz for different V_{high} and V_{low} values was studied. The large and quickly fully recoverable short-term hysteresis increased to 4 V, which may explain the results of Okunishi *et al.* [107].

The rapid reduction in V_{th} observed in the SiC MOSFETs under negative gate stress is attributed to the capture of holes, which occurs with capture times less than 1 µs. The observed increase in V_{th} during the V_{high} signal can be attributed to two factors: the acceleration of recovery associated with an increase in V_{gs} and the capture of electrons occurring during positive gate bias stress. The capture times for the hole capture were significantly faster than those for the electron capture, as evidenced by the rapid saturation of the V_{low} signal. Furthermore, short-term hysteresis during a bipolar AC period was modeled using capture and emission time (CET) maps. The simulation results are derived from the superposition of the negative and positive ΔV_{th}, which are calculated using the respective PBTI and NBTI CET maps, as a consequence of the bipolar AC stress. The observed hysteresis ΔV_{th} following the AC conditions 25 V/5 V and AC 25 V/0 V had the same power-law exponent as that of the DC stress, whereas the degradation following AC 25 V/0 V was $\approx 40\%$ lower than that at 25 V/5 V and 70% lower than that of the DC stress. Hysteresis measurements taken both before and after AC stress confirmed that hysteresis did not increase with the duration of AC stress [56], [59], [111].

Lelis *et al.* [90] demonstrated that back-and-forth, or bi-polar stress, creates a significantly larger ΔV_{T} instability compared to what is observed during unipolar stress. This linear increase in ΔV_{T} hysteresis with a logarithmic time factor is typically observed, which is attributed to the direct tunneling mechanism associated with the charging of near-interfacial oxide traps. Traps situated within one or two initial oxide monolayers exhibited continuous fluctuations in the charge state. A longer stress leads to deeper penetration of the tunneling front into the gate oxide, resulting in increased ΔV_{T} instabilities [90].

In 2020, Jiang *et al.* [199] demonstrated that the threshold voltage drift depends on the switching frequency or total number of switching cycles experienced by the device, in addition to the cumulative time under a positive or negative DC gate bias condition. In addition to the DC stress, the threshold voltage drift may be driven by the switching stress but only when the dynamic gate stress is bipolar. The device is mostly exposed to static stress at a low switching frequency (0.1 Hz), and the threshold voltage drifts caused by the static positive and negative gate biases cancel out each other. However, when dynamic bipolar gate stress was applied with a switching frequency of 150 kHz, the threshold voltage drifted rapidly, as shown in Fig. 4.25 on the left. The switch event brings an additional threshold voltage drift, which is also found in the 4H-SiC pMOS (see Fig. 4.25, right [199]). The threshold voltage drift during the switching stress in the trench 4H-SiC MOSFETs was shown to be greater than that in planar MOSFETs, as shown in Fig. 4.26. Because of the influence of the asymmetric interface traps from their acceptor- and donor-like types with varying concentrations, the asymmetric relationship suggests that V_{GSon} and V_{GSoff} do not equally contribute to the dynamic threshold voltage drift [14], [15], [150], [200], [201]. Bipolar AC gate stress, including

$V_{\mathrm{GSoff}} < 0\,\mathrm{V}$, can lead to a higher threshold voltage drift than the corresponding static gate stress.

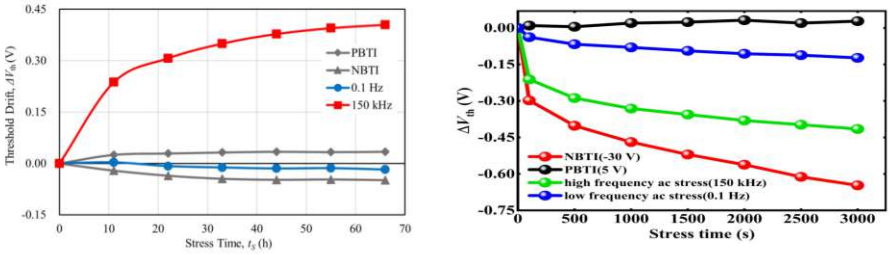


Figure 4.25.: Left: The nMOS threshold voltage drifts of under static and dynamic gate stress. PBTI: +15 Vstatic gate stress; NBTI: 10 V static gate stress at junction temperature of 175 °C. From *Zhong X.,* et al. *"Bias Temperature Instability of Silicon Carbide Power MOSFET under AC Gate Stresses." Trans. Power Electron., (2021) p. 2001* [15]. Right: pMOS threshold voltage drifts under static and dynamic stress. Wherein, NBTI and PBTI were performed under -30 V and 5 V, respectively. From *Yang L.,* et al. *"Gate Oxide Instability of 4H-SiC p-Channel MOSFET Induced by AC Stress at* 200 °C*." TED, (2023) p. 380* [199].

The threshold voltage shift at post-mid-to high-frequency stress (between 50 kHz and 5 MHz) was observed in [202], [203], [204]. This is because the inversion channel electrons tunnel into the oxide border traps and at the interface during the positive half of the rising edge of the stress cycle, causing a positive V_{th} drift.

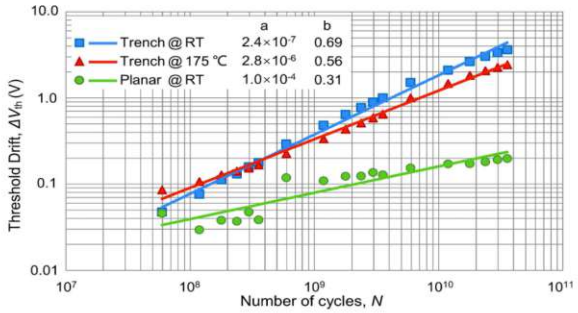


Figure 4.26.: Threshold voltage drift under bipolar dynamic gate stressing as function of accumulated number of switching cycles. The tested data followed a power law in the form of $\Delta V_{\mathrm{th}}^{\mathrm{SW}} = a \times N^b$, where a and b are constants. From *Jiang H.,* et al. *"Dynamic Gate Stress Induced Threshold Voltage Drift of Silicon Carbide MOSFET." EDL, (2020) p. 1286* [14].

$$\Delta V_{\mathrm{th}}^{\mathrm{AC}} = \Delta V_{\mathrm{th}}^{\mathrm{DC}} + \Delta V_{\mathrm{th}}^{\mathrm{SW}} \tag{4.2}$$

$$\Delta V_{\mathrm{th}}^{\mathrm{DC}} = \Delta V_{\mathrm{th}}^{\mathrm{PBTI}} + \Delta V_{\mathrm{th}}^{\mathrm{NPTI}} \tag{4.3}$$

$$\Delta V_{\mathrm{th}}^{\mathrm{SW}} = a \times N^b \tag{4.4}$$

Here, a is a constant that depends on frequency.

Currently, there are two potential competing models for GSI. The first is based on either electron-hole recombination or a locally enhanced electric field [112], [204], [205]. The second method is based on defect-assisted electron-hole recombination with several recombination pathways and different types of interface defects. These defect transitions, based on electron-hole recombination, are known as recombination-enhanced defect reactions (REDRs). Only non-radiative recombination or the NMP model can generate an REDR because the released energy is not converted into a photon, but rather utilized in a reaction involving the defect itself [114], [206] and [23], [207].

According to the locally enhanced electric field hypothesis, it is posited that all forms of electron-hole recombination associated with GSI involve an interface defect. GSI is determined by the total number of switching events rather than the stress duration. The charging time constant increases (from nanoseconds to hours or more) when the traps are located deeper in the gate oxide at the interface. An increased electric field increases the likelihood of tunneling, thereby driving more electrons into the oxide [204]. During turn-on, the positive interface states are neutralized by the capture of electrons from the conduction band. An increase in V_{high} resulted in a greater number of free electrons within the inversion channel, thereby accelerating the neutralization of the interface traps. In the turn-off state, when $V_{\mathrm{low}} < V_{\mathrm{th}}$ the Fermi level is shifted significantly below the conduction band. The interface trap state located above the Fermi level acquires charge by capturing holes from the valence band. As the Fermi level decreases, the number of positively charged interface states increases. Consequently, V_{th} decreased as V_{low} decreased. Note that the hysteresis observed in this AC test was fully reversible, regardless of the bias applied [112], [208] and [91].

After the pulse ends in AC test, there is a net negative shift in V_{th}, indicating that the net trapped charges are due to the interface and border traps that follow the stress and are positive. The captured charge saturates to a constant value for high-frequency pulses (above 500 kHz) because it does not have sufficient time to discharge. Consequently, it can be said that the defects that occur during AC BTI stress are mostly donor-like interface traps and not only border-trapped defects [205]. Because the traps were filled, the greater subthreshold leakage caused by these traps was not noticeable when the threshold voltage was measured. The depth is of the order of nanometers for a normal switching speed, which is one order of magnitude less than the gate oxide thickness (t_{ox}) [198], [202].

In 2023, Feil *et al.* [206] demonstrated that gate switching leads to the creation of fast, acceptor-like interface defects that lead to a shift in the threshold voltage, and hence appear to be responsible for GSI. The principal and distinguishing characteristic of the GSI is that it is only dependent on the cumulative number of switching cycles N (up to at least 2 MHz), whereas the stress time (t_{stress}) and duty factor α in typical experimental ranges (kHz to MHz) do not influence the drift, see Fig. 4.27. The dependency on N applies not only to ΔV_{th} but also to the entire capacitance-voltage ($C-V$) characteristics. GSI degradation decreases with increasing temperature [55], [76], [114], [176], [207], [209].

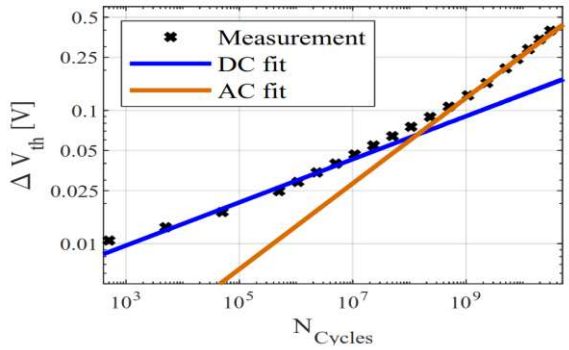


Figure 4.27.: Two different slopes are visible, the first corresponding to a typical DC-like drift behavior (DC fit"). The second largest slope is due to the bipolar AC stress effect ("AC fit"), which sets beyond 10^8 switching cycles under these stress conditions. From *Salmen P.,* et al. *"A new test procedure to realistically estimate end-of-life electrical parameter stability of SiC MOS." IRPS, (2021) p. 3* [113].

ΔV_{th} at stress times with increasing frequency did not follow a single straight line and two different drift regions could be observed. Upon reaching the GSI field at approximately 10^3s, the drift began to depend on the frequency.

The $C-V$ method demonstrated that devices with a predominant GSI component do not show a bias-independent shift post-stress, indicating that a locally enhanced electric field model does not result in the inclusion of a quasi-permanent charge; thus, it was expected to have a second-order effect rather than a primary cause [55]. The newly created acceptor-like interface defects were identified by measuring $C-V$ curves before and after GSS while sweeping the gate voltage from accumulation to inversion.

A frequently observed hysteresis in the current-voltage characteristics during up and down sweeps is also evident in the capacitance characteristics, as shown in Fig. 4.17.

The local shift of the $C-V$ curve agrees well with the result for ΔV_{th} from the MSM measurement [114], [176]. A short measured recovery time did not reveal a significant difference in hysteresis. Newly formed interface defects are likely generated by previously inactive precursor states. In addition, the charging and discharging processes of these interface defects occur at a rate that exceeds the detection capabilities of our hysteresis measurements, which are less than 1 µs.

According to the $C-V$ measurement, it can be concluded that any type of electron-hole recombination associated with GSI is linked to an interface defect. Defect-assisted electron-hole recombination may occur at either the rising or falling edge of the gate stress signal. There are several recombination pathways that are assisted by different types of interface defects, and a single one is sufficient to trigger GSI. Note that the ΔV_{th} drift is not necessarily caused by quasi-permanently trapped charges [55], [114], [176] and [23], [207].

4.6. Summary

This chapter discusses the reliability issues observed in MOSCAPs, planar MOSFETs, lateral MOSFETs, and trench MOSFETs. The temperature-dependent hysteresis width varies across different surfaces because of the distinct density of states. During the down sweep, the traps maintained their charge states, and hysteresis often arose when the emission time exceeded the capture time. Two potential trap candidates, "slow" and "fast" were assumed. At elevated temperatures, the hysteresis width is often reduced owing to the enhanced capture and emission rates. In some cases, anomalous widening of the hysteresis at elevated temperatures and counterclockwise (negative) behavior were observed, which were attributed by some authors to the presence of positive mobile ions. The hysteresis width in the p-substrate is wider than that in the n-substrate, and the changes in V_{fb} and V_{th} are contingent upon the measurement conditions. The density of states is complex and generally includes two exponential distributions from the conduction and valence bands, two Gaussian distributions near the mid-gap, and a constant trap throughout the entire band gap. Measurements of the capture cross-section showed the presence of at least three types of traps. The transition layer where the traps are situated is dependent on the technology and POA, typically measuring up to 6 nm in width from the interface. DOS can be reduced by employing various oxide deposition techniques and post-oxidation annealing, often in NH_3, NO+NH_3, NO, and H_2 ambient gases. This lowering enhances the subthreshold voltage slope, channel mobility, threshold voltage drift, and hysteresis width in both the planar and trench 4H-SiC MOSFETs. The different hysteresis characteristics of the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves, along with the gate switching instability and hysteresis width of the planar and trench 4H-SiC MOSFETs, are outlined.

5. Overview of Trap Kinetics Simulation Methods for the SiC/SiO_2 Interface

Modeling charge trapping kinetics is essential for understanding and predicting the behavior of charge carriers (electrons and holes) in semiconductors, insulators, and their interfaces. Traps or defects can capture and release carriers, thereby influencing the electrical, optical, and thermal properties of the materials. Trap kinetics models facilitate the identification of trap types, energy levels, and defect densities in a material. This model describes carrier dynamics and provides insights into the duration of carrier trapping and the rate of their release, which in turn affects the conductivity and recombination rates. Modeling is used to optimize and enhance device performance by analyzing the impact of different trap types and their quantities on reliability and lifespan. Finally, the models enable the interpretation of experimental data and the extraction of meaningful parameters for trap characterization.

In 2006, A. Pérez-Tomás *et al.* [210], [211] applied the Lombardi model to analyze the effects of charge trapping and scattering at the interface states, identifying these phenomena as primary contributors to the reduction in mobility in thermally oxidized SiC MOSFETs, although they did not consider trap kinetics. S. Potbhare, A. Lelis *et al.* [151], [212], [213] in the same year, developed a physics-based device simulator for the numerical analysis of 4H-SiC MOSFETs. This simulator utilizes an enhanced mobility model that accounts for the effects of bulk and surface phonons, surface roughness, and Coulomb scattering resulting from occupied interface traps and fixed oxide charges. The extracted densities of the state profiles of the interface traps were used for the simulations. A charge-trapping model was not implemented; therefore, the ΔV_{th} shift was not simulated. Subsequently, by employing simulations to align the experimental $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves before and after stress, it was possible to calculate the changes in the trapped charges in the oxide as a function of the stress voltage and stress duration. This roughly aligns with the charge, which can be analytically derived by observing the shift in the threshold voltage ($\Delta N_{\mathrm{OT}} = \Delta V_{\mathrm{T}} \cdot C_{\mathrm{ox}}/q$) [212], [214]. Simultaneously, a proper investigation of the band offsets at the SiC/SiO_2 interfaces is important for simulating the energy relations between the band edges and trap levels to simulate the exact capture and emission times and predict the trap occupations. For the SiC/SiO_2 interface, the $\Delta E_{\mathrm{C}}/\Delta E_{\mathrm{V}}$ band offsets are 2.7 eV/2.9 eV [8], [215].

Subsequently, in 2008 S. Potbhare, A. Lelis *et al.* [216] developed a methodology to evaluate the transient response and dynamics of the interface traps in 4H-SiC MOSFETs. This methodology incorporates a time- and energy-dependent interface trap occupation model. In fact, this generation-recombination model for traps and surface electrons resembles the Shockley-Read-Hall recombination mechanism. The correla-

tion between the simulated and experimental DC and transient drain currents enabled the extraction of the density and effective capture cross-sections of the interface traps, as illustrated in Fig. 5.1. Trap states located near the band edges can be occupied faster and exhibit a notably larger effective capture cross-section than traps positioned near the midgap. It was proposed that fast interface traps have large capture cross-sections, whereas those with smaller capture cross-sections consist of a mixture of mid-gap interface states and slow oxide traps. The analysis of trap dynamics indicates that long-term device stability can be enhanced by minimizing oxide traps, whereas short-term stability can be improved by reducing interface traps [216]. The density of states computed using the DFT approach was used to simulate the performance of the 4H-SiC MOSFETs. The density of states reaches energies up to 200 meV inside the conduction band. The results were used to compute the occupied trap densities for the simulation $I_d - V_{gs}$ and compare this curve with the measured data, as shown in Fig. 5.2. The reliability issues of 4H-SiC MOSFETs can be attributed to the significant presence of occupied traps. Negatively charged traps at the interface contribute to Coulomb scattering, resulting in additional degradation of the transconductance, $I_d - V_{gs}$ and $C - V$ characteristics [217], [218], [219].

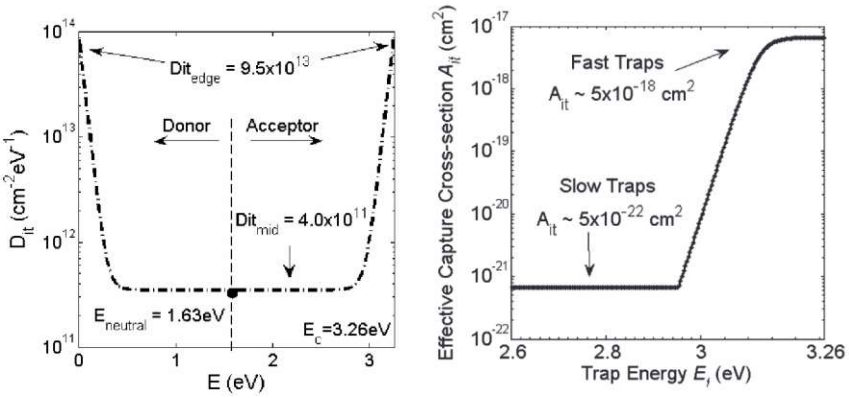


Figure 5.1.: Left: Example of the extracted interface trap DOS profile for 4H-SiC, showing a constant distribution in the mid-gap region, and an exponential rise near the band edges. From *Potbhare S.*, et al. *"Characterization of 4H-SiC MOSFET Interface Trap Charge Density Using a First Principles Coulomb Scattering Mobility Model and Device Simulation." SISPAD, (2005) p. 96* [145]. Right: An energy-dependent trap capture cross-section profile was simulated to match the measured transient current. Two distinct levels were identified: fast traps near the conduction band and slow traps mid-gap. The energy scale spans from 0 eV (valence band) to the conduction band minimum (2.6 eV) for the 4H-SiC. From *Potbhare S.*, et al. *"Energy- and Time-Dependent Dynamics of Trap Occupation in 4H-SiC MOSFETs." TED, (2008) p. 2066* [216].

To calculate the influence of defects on the thermal dielectric relaxation current (TDRC) spectra the Shockley-Ramo-Theorem was used. According to this theorem, a larger contribution from NITs leads to higher current density [39]. A charge sheet model was used to estimate the quantity of inversion charge density $Q_{inv} = qN_{inv}$ in the 4H–SiC MOS devices. This model simplifies the calculation of Q_{inv} by assuming

that the inversion layer is a sheet of charge with an infinitely small thickness. Thus, Q_{inv} at any surface potential is simply the difference between the total semiconductor space charge Q_{sc} and depletion layer charge Q_{B}. By fitting the $\mathrm{D_{it}}$ distribution and positive fixed charges to the measured data, it is possible to evaluate the real trap distribution [220].

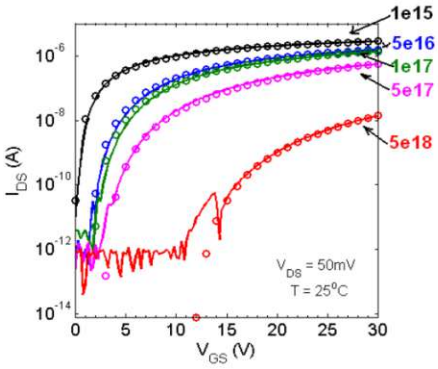


Figure 5.2.: Simulated (circles) and measured (lines) subthreshold $I_{\mathrm{d}} - V_{\mathrm{gs}}$ characteristics of 4H-SiC MOSFETs with various channel doping values 10^{15}–$10^{18}\,\mathrm{cm}^{-3}$. From *Potbhare S.,* et al. *"Modeling the Effect of Conduction Band Density of States on Interface Trap Occupation and its Influence on 4H-SiC MOSFET Performance." SISPAD, (2009) p. 1* [217].

The quasi-static and high-frequency $C-V$ characteristics obtained using numerical simulations allow the extraction of a non-uniform distribution of traps in the SiC epilayer, in addition to interface traps. Parameters related to relatively large trap concentrations, including energy levels and deep-level densities, were obtained from capacitance–voltage ($C-V$) measurements. The disparity observed in the $C-V$ curves of n-type MOS capacitors when measured in quasi-static mode versus high frequency mode at room temperature is directly related to the density of the interface traps that possess energy levels near the semiconductor conduction band. Using acceptor-like traps with energy levels close to the conduction band and two shallow donor-like trap levels ($\mathrm{E_D}$) showed good agreement between the analytical calculations and the measured high-frequency $C-V$ curves of the Si-face 4H-SiC/SiO_2 MOSCAPs over a wide temperature range. At low temperature, the "kink" at high-frequency $C-V$ characteristics, in case where the Fermi level is equal to the deeper donor trap level ($\mathrm{E_F} \approx \mathrm{E_D}$), confirms that electrons are freezed-out [117].

Maresca L. *et al.* [168] demonstrated a TCAD model of a commercial SiC planar MOSFET by considering a non-uniform trap distribution along the SiO_2/SiC interface. The $C-V$ and $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves were fitted using two acceptor-like interface traps: one with a peak in the density of states near the conduction band, the other with a donor-like peak near the valence band and fixed positive charges in the oxide. The kinetics of the traps introduced by two calibrated capture cross-sections for both electrons and holes were used in the SRH model. The hysteresis width was determined, and the more the capture cross section increased, the more the hysteresis effect increased.

Traps located near the valence and conduction bands found to be fast, whereas those located near the mid-bandgap were found to be slow. An appropriate comparison of the hysteresis width across a broader temperature range has not yet been accurately conducted [104], [221].

In 2013, Uhnevionak *et al.* [222] implemented two active types of traps: donor- and acceptor-like traps (both energetically located near the conduction band of the 4H-SiC substrate), fixed charge, and mobility degradation models to describe the observed electrical characteristics of the Si-face 4H-SiC nMOSFET. A temperature-independent TCAD model was developed using trap-assisted tunneling to match the observed experimental data in [223], [224].

In 2018, He Y. J. *et al.* [225] performed simulations of the hysteresis width of $C-V$ curves of MOSCAPs. This was achieved using a two-dimensional electrical interface model that incorporated both interface and near-interface traps. The model utilized the phonon-assisted tunneling process to account for temperature effects together with the interface Shockley–Read–Hall model. The entire process involves two types of traps: deep oxide traps and shallow oxide traps. This indicated that the near-interface traps led to an increase in the threshold voltage shift in the SiC MOSFETs as the temperature increased. With an increase in temperature, both the deep and shallow oxide traps become quicker during charge capture. However, shallow oxide trap charges dominate because the capture processes are enhanced at elevated temperatures, leading to an increased capture of charges by the oxide traps. Shallow oxide-trapped charges can be released in a short time, whereas deep oxide-trapped charges remain unreleased [225]. The reaction–diffusion model was used to investigate the PBTI and hysteresis in $I_\mathrm{d}-V_\mathrm{gs}$ curves for stress times up to 10^4 s and different temperatures. This model describes the generation of defects at the SiC/SiO_2 interface resulting from the breaking of passivated Si-H bonds. The released hydrogen diffuses from the interface into the oxide layer and may recombine during the recovery process [94].

To better investigate the phonon-assisted tunneling process to account over a wide temperature range of 200–350 K, in 2018, Tyaginov S. E. *et al.* [226] applied the two state non-radiative multiphonon (NMP) model for simulating BTI. Two border traps were incorporated into the simulations: deep donor and acceptor traps with energy levels of ∼3.0 eV and ∼1.7 eV, respectively, above the valence band edge.

Afterwards, C. Schleich *et al.* [105], [106], [227], in 2019, by using the two state NMP model successfully describe the measurements (extended MSM (eMSM), pulse eMSM (pMSM), and ramped voltage stress (RVS)) with long stress and recovery times conducted on lateral and trench SiC technologies. Two electron trap bands, characterized as shallow and fast, along with hole trap bands, were identified for PBTI and NBTI in lateral devices (see Fig. 5.3). The modeled shallow traps indicate the intrinsic charge-trapping behavior of SiO_2, which is corroborated by a comparison with the slow V_th drifts observed in vertical devices.

Finally, Grasser T., Feil M. W., *et al.* [23], [55], [207] in 2023 successfully modeled the Gate Switching Instability (GSI). It has been demonstrated that recombination events at the interface lead to recombination-enhanced defect reactions (REDRs),

which in turn leads to tzhe creation of fast acceptor-like interface defects. These comprehensive physical models for GSI are based on the NMP model. The subsequent sections provide a comprehensive description of the key models used to model trap kinetics.

parameter	TB1	TB2	TB3	TB4	
$\overline{E}_T \pm \sigma_{E_T}$	1.87±0.08	1.73±0.165	-1.12±0.24	-1.77±0.04	eV
$\overline{S} \pm \sigma_S$	-	4.93±1.95	5.2±4.89	-	eV
R	-	0.437	1.19	-	1
N_T	$2.8 \cdot 10^{19}$	$3.44 \cdot 10^{19}$	$1.26 \cdot 10^{19}$	$7.3 \cdot 10^{18}$	cm^{-3}

Figure 5.3.: The extracted defect band parameters for fast EB (TB1), shallow EB (TB2) and donor like traps (TB3,4). From *Schleich C.,* et al. *"Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs." IEDM, (2019) p. 4* [105], [106], [227].

5.1. Capture and Emission Time (CET) Maps

A capture-emission time (CET) map is a two-dimensional logarithmic plot that represents the trap density in relation to the corresponding logarithmic capture and emission times. CET maps were generated by numerically differentiating a series of ΔV_{th} recovery curves. This method has demonstrated the ability to explain a broad range of NBTI and PBTI stress and recovery patterns including DC, AC, and duty-factor stresses [228]. The activation energies associated with the charge transfer can be characterized as a combination of two Gaussian distributions. The first distribution refers to defects characterized by short capture and emission times, referred to as the recoverable component r. The second distribution refers to permanently charged defects with a large emission time p [111].

The primary parameters of this analytic density distribution $g(E_c, E_e)$ from equation 5.1 include the mean values μ_c and $\mu_{\Delta e}$ of the capture and emission activation energies $E_{a,c}$ and $E_{a,e}$, respectively, along with their standard deviations σ_c and $\sigma_{\Delta e}$ [229]. Terms σ_c and $\sigma_{\Delta e}$ represent the distribution widths in both directions, as shown in Fig. 5.4. Additionally, the emission activation energies $E_{a,e}$ increased with the capture activation energies $E_{a,c}$, following the relationship $E_{a,e} = E_{a,c} + \Delta E_{a,e}$. An implicit correlation is observed between the standard deviations, expressed as $\sigma_e^2 = p \cdot \sigma_c^2 + \sigma_{\Delta e}^2$, where p denotes the correlation between the capture and emission activation energies. A value of $p = 0$ indicates no correlation, whereas $p = 1$ denotes strong correlation, as shown in Fig. 5.4. Consequently, the charged trap densities μ_c and $\mu_{\Delta e}$ for each component with amplitude A were determined as follows:

$$g(E_c, E_e) = \frac{A}{2\pi\sigma_c\sigma_{\Delta e}} \cdot \exp\left(-\frac{(E_c - \mu_c)^2}{2\sigma_c^2} - \frac{(E_e - (rE_c + \mu_{\Delta e}))^2}{2\sigma_{\Delta e}^2}\right) \tag{5.1}$$

The shift in the threshold voltage, corresponding to a specified stress and recovery period, is determined by integrating the activation energy map across all defects, both

recoverable and permanent, which have been charged up to the stress period and have not yet been discharged by the recovery period [111].

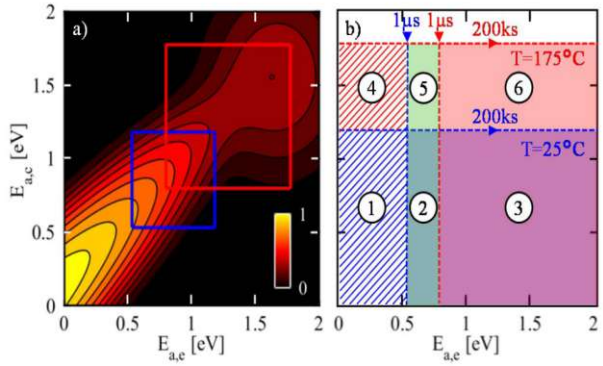


Figure 5.4.: Example of activation energy distribution from [111]. Left: Analytical activation energy map obtained using stress and recovery data with recovery traces for stress times from 1 µs to 200 ks. The charged trap density g is shown to be dependent on the capture and emission activation energies, and is normalized to 1 [228]. The measurement range from 1 µs to 200 ks is marked in blue for T=25 °C and in red for T=175 °C. Right: Charge trap occupation map for DC stress at T=25 °C and T=175 °C. The blue and red rectangles mark the traps occupied for a stress time of 200 ks and measurement delay of 1 µs. The blue and red patterned areas indicate the regions of the activation energy map outside the measurement range at T=25 °C and T=175 °C, respectively. The green region marks the traps with activation energies within the measurement range at T=25 °C, and is captured when stressing at T=175 °C and measuring V_{th} at T=25 °C. From *Puschkarsky K.,* et al. *"Understanding and Modeling Transient Threshold Voltage Instabilities in SiC MOSFETs." IRPS, (2018) p.3B.5-3* [111].

To relate the experimentally observed trap kinetics to their physical origin, the capture–emission map results can be compared with DFT calculations to identify the atomic structures and energy levels of the corresponding defect types.

5.2. Density Functional Theory (DFT)

With advancements in computing capacity, the use of DFT for trap density computations at interfaces and substrates has been made feasible. Previous studies have investigated oxygen-, nitrogen-, and hydrogen-related defects, including Si-Si bonds (O vacancies), Si_2-C-O structures, peroxy linkages, and hydrogen bridges (Si-H-Si) [25], [26]. Oxide or NIT and substrate defects with energy levels close to the SiC conduction or valence band mus are fast and may be easily involved in charge trap kinetics, whereas defects with higher energy levels are slow and require more time, voltage, or temperature to capture or emit charges. The recently calculated trap types are listed in Table 5.1 (assuming that $E_{\mathrm{V}}^{\mathrm{SiO_2}} = 0\,\mathrm{eV}$, $E_{\mathrm{V}}^{\mathrm{SiC}} = 3.3\,\mathrm{eV}$, $E_{\mathrm{C}}^{\mathrm{SiC}} = 6.3\,\mathrm{eV}$, and $E_{\mathrm{C}}^{\mathrm{SiO_2}} = 8.9\,\mathrm{eV}$). Furthermore, DFT calculations showed that, similar to nitrogen, phosphorus can also passivate the $(C_i)_2$ defect and therefore reduce its concentration. Although the diffusion of nitrogen into SiC is difficult, it has been shown that phosphorus can be

easily incorporated into SiC [230]. Charge transition levels or states can be explained by considering a neutral trap in which the state represents as zero. If this trap captures an electron, the transition is denoted as $(0/-)$ and if it captures a hole $(0/+)$. There can be further charge states that may be more negative when capturing electrons or less negative or neutral when capturing a hole, and with the acceptor-like trap, the states are $(-/--)$, $(--/-)$, and $(-/0)$. For a donor-like trap, the transitions are $(+/0)$, $(++/+)$, and $(+/++)$ for capturing electrons and holes, respectively.

Table 5.1: DFT calculated type of Substrate/Interface Traps.

Trap type	Trap energy level	Transition states	References
$(C_i)_2$ SiC	E_C^{SiC}−0.04 eV	$(--/-)$	Devynck F., *et al.* [25], [26], [230]
	E_C^{SiC} − 0.23 eV	$(-/0)$	
	E_V^{SiC}+0.71 eV	$(+/0)$	
	E_V^{SiC}+0.49 eV	$(++/+)$	
Si_2−C−O SiO_2	E_C^{SiC}+0.81 eV	$(--/-)$	
	E_C^{SiC}+0.21 eV	$(-/0)$	
	E_V^{SiC}−0.04 eV	$(+/0)$	
Si−H−Si SiO_2	E_C^{SiC}+0.1 eV	$(-/0)$	
	E_V^{SiC} + 1.73 eV	$(+/0)$	

5.3. Trap Density of States (DOS)

The previous chapters discussed the occurrence of various trap types in the SiC/SiO_2 system, including the following:

- Fixed positive charges in oxide.
- Acceptor-like traps which change their state during a bias sweep.
- Donor-like traps which also change their state.
- Neutral traps with energy level location mostly close to mid-gap. During application of a gate bias, they may change to positive or negative states.
- Amphoteric P_b or P_{bC} trap centers.

The energy distribution of these traps may have a complex form, and can be represented as follows:

Uniform distribution	$D_{it};\quad \text{for } E_t - \frac{1}{2}\cdot E_G < E < E_t + \frac{1}{2}\cdot E_G$
Exponential distribution (tails)	$D_{it,A}\cdot e^{\left(\frac{E_t - E_C}{W_{ta}}\right)};\ D_{it,D}\cdot e^{\left(\frac{E_t - E_V}{W_{td}}\right)}$
Gaussian distribution	$D_{it,A}\cdot e^{\left(-\left(\frac{E_{ga} - E_t}{W_{ga}}\right)^2\right)};\ D_{it,D}\cdot e^{\left(-\left(\frac{E_t - E_{gd}}{W_{gd}}\right)^2\right)}$

D_{it} is the trap concentration for bulk materials in $eV^{-1}cm^{-3}$, and for interfaces in $eV^{-1}cm^{-2}$. Here, E_t is the trap energy, E_C is the conduction band energy, and E_V is the valence band energy. $W_{td}, W_{ta}, W_{gd}, W_{ga}$ are characteristic decay energies. E_{gd} and E_{ga} are the energy peaks for Gaussian distribution in eV. In certain instances, the trap energy level is referenced to the Fermi level, whereas in some TCAD programs, it is referenced to the mid-gap level. Precise band offsets for 4H-SiC were used in this study [8], [231].

5.4. Shockley–Read–Hall model

The widely known SRH model has been extensively employed for the simulation and validation of N_{it} and D_{it} using the electrical measurements of 4H-SiC MOSFETs. Commercial TCAD software, such as Synopsys, Silvaco, and GTS, offers this model [232], [233], [234]. Shockley–Read–Hall (SRH) recombination, which implicitly relies on traps, does not explicitly model these traps. The model explicitly considers the fixed charges and trap occupation by the stored space charges in the bulk and at the interface.

The total charge generated by the traps was deduced from the right-hand side of Poisson's equation. The overall charge density is determined by

$$Q_t = q\left(N^+_{it,D} - N^-_{it,A}\right) \tag{5.2}$$

Where $N^+_{it,D}$ and $N^-_{it,A}$ are the densities of the occupied (ionized) donor-like and acceptor-like traps, respectively. The occupied DOS depends on the trap density and the probability of occupation:

$$N^+_{it,D} = D_{it,D} f_p \tag{5.3}$$

$$N^-_{it,A} = D_{it,A} f_n \tag{5.4}$$

5.4.1. Trap Occupation Dynamics

Based on the SRH theory [235], four potential carrier transitions between the trap states and the valence or conduction bands are treated: the capture of electrons from the conduction band $r^C_{12,n}$, the emission of captured electrons from the trap to the

conduction band $r^{\mathrm{C}}_{21,n}$, hole capture when the trapped electron moves to the valence band (the hole is captured by the trap) $r^{\mathrm{V}}_{12,p}$ and hole emission when an electron from the valence band is captured (the hole is released from the vacant trap to the valence band) $r^{\mathrm{V}}_{12,p}$. As we can see, the SRH theory is a 2-state process. Thus, we suggest that the capture path proceeds from state 1 to state 2, whereas the emission path is reversed from state 2 to state 1, where the trap energy level for state 1 is E_{t} and that for state 2 is $E_{\mathrm{C,V}}$. Consequently, we can reformulate the capture transition rate of electrons from the conduction band according to SRH theory as $k^{\mathrm{C}}_{12,n}$ and the electron emission rate from the trap to the conduction band as $k^{\mathrm{C}}_{21,n}$. For holes, $k^{\mathrm{C}}_{12,p}$ and $k^{\mathrm{C}}_{21,p}$.

Trap occupation dynamics were linked to capture and emission rate models. The electron occupation probability f_n of a trap may be between 0 and 1 and depends on the capture and emission rates. The general rate equation is as follows:

$$\frac{\partial f_n}{\partial t} = \sum_i r^i_n \tag{5.5}$$

$$r^i_n = (1 - f_n)\, k^i_{12,n} - f_n k^i_{21,n} \tag{5.6}$$

Here, $k^i_{12,n}$ denotes the electron capture rates for empty traps and $k^i_{21,n}$ denotes the electron emission rate from the occupied traps.

To convert the electron representation into a hole representation, the following relationships were utilized:

$$k^i_{12,p} = k^i_{21,n} \tag{5.7}$$

$$k^i_{21,p} = k^i_{12,n} \tag{5.8}$$

$$f_p = (1 - f_n) \tag{5.9}$$

$$r^i_p = -r^i_n \tag{5.10}$$

$$\tag{5.11}$$

Under steady-state conditions, the rate equations at defect energy E_1 are

$$r^{\mathrm{C}}_{12,n} - r^{\mathrm{C}}_{21,n} = r^{\mathrm{V}}_{12,p} - r^{\mathrm{V}}_{21,p} \iff R^{\mathrm{SRH}}_n = R^{\mathrm{SRH}}_p = R^{\mathrm{SRH}} \tag{5.12}$$

These rates can be described in relation to the electron occupation fraction as follows:

$$r^{\mathrm{C}}_{12,n} = k_{12,n}\,(1 - f_n)\,\mathrm{D_{it}} \tag{5.13}$$

$$r^{\mathrm{C}}_{21,n} = k_{21,n} f_n \mathrm{D_{it}} \tag{5.14}$$

$$r^{\mathrm{V}}_{12,p} = k_{12,p} f_p \mathrm{D_{it}} \tag{5.15}$$

$$r^{\mathrm{V}}_{21,p} = k_{21,p}\,(1 - f_p)\,\mathrm{D_{it}} \tag{5.16}$$

$$\tag{5.17}$$

where:

$$k_{12,p} = v_{\mathrm{th,p}}\sigma_p p \mathrm{e}^{-\beta\epsilon_{12}} \tag{5.18}$$
$$k_{21,p} = N_{\mathrm{V}} v_{\mathrm{th,p}}\sigma_p \mathrm{e}^{-\beta E_{21}} \tag{5.19}$$
$$k_{12,n} = v_{\mathrm{th,n}}\sigma_n n \mathrm{e}^{-\beta\epsilon_{12}} \tag{5.20}$$
$$k_{21,n} = N_{\mathrm{C}} v_{\mathrm{th,n}}\sigma_n \mathrm{e}^{-\beta E_{21}} \tag{5.21}$$
$$\tag{5.22}$$

where $\beta = 1/kT$, $\epsilon_{12} = E_{\mathrm{t}} - E_{\mathrm{V}}$ is the capture energy barrier for holes and $\epsilon_{12} = E_{\mathrm{t}} - E_{\mathrm{C}}$ is the capture energy barrier for electrons.

If $\mathrm{E}_1 < \mathrm{E}_2$ (E_1 is a trap energy and E_2 is a conduction or valence band energy), the barrier for the capture process of electrons and holes ϵ_{12} is 0 eV, we can rewrite

$$k_{12,p} = v_{\mathrm{th,p}}\sigma_p p \tag{5.23}$$
$$k_{21,p} = N_{\mathrm{V}} v_{\mathrm{th,p}}\sigma_p \mathrm{e}^{-\beta E_{\mathrm{V}t}} \tag{5.24}$$
$$k_{12,n} = v_{\mathrm{th,n}}\sigma_n n \tag{5.25}$$
$$k_{21,n} = N_{\mathrm{C}} v_{\mathrm{th,n}}\sigma_n \mathrm{e}^{-\beta E_{\mathrm{C}t}} \tag{5.26}$$
$$\tag{5.27}$$

Here $\mathrm{E}_{\mathrm{C}t} = E_{\mathrm{t}} - E_{\mathrm{C}}$ and $\mathrm{E}_{\mathrm{V}t} = E_{\mathrm{V}} - E_{\mathrm{t}}$. The two situations can be combined when the trap energy level is in the bandgap or outside the bandgap, and we denote the barrier for transitions $1 \to 2$ and $2 \to 1$ as $\epsilon_{12} = \max(E_{12}, 0)$ and $\epsilon_{21} = \max(E_{21}, 0)$.

This indicates the neglect of an energy barrier for the electron capture process when $E_t < E_{\mathrm{C}}$ (electrons 'descend') and the neglect of an energy barrier for the hole capture process when $E_t > E_{\mathrm{V}}$ (holes 'ascend'). It is important to note that the established traditional SRH theory does not consider charge-carrier tunneling or the potential existence of thermal barriers [18], [235].

The SRH recombination rate in the steady-state case is [236]

$$R^{\mathrm{SRH}} = \frac{\mathrm{D}_{\mathrm{it}} v_{\mathrm{th}}^n v_{\mathrm{th}}^p \sigma_n \sigma_p \left(np - n_{\mathrm{i}}^2\right)}{v_{\mathrm{th}}^n \sigma_n \left(n + n_1\right) + v_{\mathrm{th}}^p \sigma_p \left(p + p_1\right)} \tag{5.28}$$

Every capture and emission step links the trap to the carrier reservoir. In a stationary state, the trap reaches an equilibrium with the reservoir. This principle of detailed balance connects the capture and emission rates.

$$k_{21,i} = k_{12,i} e^{\left(\frac{E_t - E_{\mathrm{F}}}{kT}\right)} \tag{5.29}$$

5.4.2. Capture Cross-Section Model

The capture and emission times determined by the SRH model were insufficient for forecasting the hysteresis effect in the lateral and trench 4H-SiC MOSFETs at both

upward and downward sweep rates, even over a broad temperature range. However, the BTI has been effectively described in several instances, as discussed in previous sections. To simulate the hysteresis effect, asymmetry in the capture and emission processes is required, which increases the corresponding time. To achieve this, the conventional SRH model may be modified by incorporating an additional factor $\exp(-x_t/x_0)$ to account for the effect of electron tunneling or dependencies, particularly for the cross-sections σ_n and σ_p. Alternatively, we used the equations with a small energy barrier.

To simulate the hysteresis Heiman F. P. and Warfield G. modified the σ_n and σ_p which now depend on their distance in the insulator x_t [237].

$$\sigma_n\left(x_t\right) = \sigma_n e^{-k_n x_t} \tag{5.30}$$

$$\sigma_p\left(x_t\right) = \sigma_n e^{-k_p x_t} \tag{5.31}$$

where

$$k_n^2 = \frac{2m_n\left(E_\mathrm{C} - E_{tA}\right)}{\hbar^2} \tag{5.32}$$

$$k_p^2 = \frac{2m_p\left(E_{tD} - E_\mathrm{V}\right)}{\hbar^2} \tag{5.33}$$

are the evanescent wavevectors of the semiconductor electron and hole states during their tunneling into the insulator, E_{tA} and E_{tD} energy levels for acceptor-like and donor-like traps, respectively. The modified SRH model cannot be used in simulations based on the established atomistic theories [18], [92], [238]. A modified capture cross-section model was used to calculate the capture and emission rates of the interface and oxide defects. Consequently, increased trap occupation leads to channel mobility degradation owing to Coulomb scattering, linking trap kinetics directly to the electrical performance of 4H-SiC MOSFETs.

5.5. Channel Mobility Degradation Model

The channel mobility in 4H-SiC MOSFETs can be represented as a combination of various mobility components that incorporate the following scattering mechanisms: (1) Coulomb scattering of ionized impurities in the bulk (μ_{II}), (2) Coulomb scattering at the interface charges (μ_C), (3) surface-roughness scattering (μ_{SR}), (4) surface-phonon scattering (μ_{SP}), and (5) bulk phonon scattering (μ_{PB}) [145], [211], [239], [240], [241].

We assumed that only Coulomb scattering at the interface charges was dominant, because of the large number of electrically active interface traps. Therefore, we can rewrite using Matthiessen's rule.

$$\mu = \left(\frac{1}{\mu_C} + \frac{1}{\mu_\mathrm{others}}\right)^{-1} \tag{5.34}$$

In Sentaurus Device (s-device) this model is included in the form [233]

$$\mu_C = \frac{\mu_1 \left(\frac{T}{300\text{K}}\right)^k \left\{1 + \left[c/\left(c_{\text{trans}}\left(\frac{N_{\text{it}}}{N_0}\right)^{\eta_1}\right)\right]^\nu\right\}}{\left(\frac{N_{\text{it}}}{N_0}\right)^{\eta_2} \cdot D \cdot f\left(F_\perp\right)} \tag{5.35}$$

where N_{it} is the interface charge density and N_0 is $1 \times 10^{11}\text{cm}^{-2}$ or$1 \times 10^{18}\text{cm}^{-3}$ is the interface charge density. $c = n$ for electron mobility or p for hole mobility and:

$$f\left(F_\perp\right) = 1 - e^{\left[-\left(F_\perp/F_0\right)^\gamma\right]} \tag{5.36}$$

$$D = e^{-x/l_{\text{crit}}} \tag{5.37}$$

x is the distance from the interface, F is the electric field (V/cm), $F_\perp$ is the transverse electric field normal to the semiconductor–insulator interface, l_{crit} is the fit parameter, D is the damping that switches off the inversion layer terms farther from the interface.

N_{it} is linked to the DOS and SRH models in the self-consistent simulations. The temperature coefficient for the inversion mode is important and can be modified. In a simplified way the coulomb component is proportional to $\mu_C \propto \mu_0(T/300)^\alpha/N_{\text{it}}$. In this study, $\mu_0 = 10\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, $\alpha = 2.8$, and $N_{\text{it}}(T)$ are temperature-dependent interfacial charge densities in cm^{-2} [99], [242].

5.6. Amphoteric or Defect-Pool Model

The SiC/SiO$_2$ system contains both P_b and P_{bC} centers, which are attributed to Si and C dangling bonds. They may acquire either a positive or negative charge, making them amphoteric, that is, they can capture holes or electrons [243]. If the concentration of carbon atoms at the SiC/SiO$_2$ interface increases, they may build up into larger clusters exhibiting graphite-like band structure, similar to those found in the narrow energy gap of amorphous carbon-hydrogen layers. These graphite-like clusters exhibit amphoteric behavior [32]. Consequently, the amphoteric centers exhibiting a wide energy distribution along the entire SiC bandgap may explain the continuum of interface states observed in SiC/SiO$_2$ D$_{\text{it}}$ [8], [22], [25], [26].

The charge states of amphoteric defects were determined using the SRH model. This amphoteric or defect-pool approximation is valid only if: (1) the defect distribution of amphoteric defects is represented by two identically shaped energy distributions of acceptor- and donor-like defect states, separated by the effective correlation energy (the energy between two trap states); (2) the ratios of the capture cross-sections for charged and neutral trap states are significantly asymmetric; (3) the defect density increases between the quasi-Fermi levels for the trapped carriers [244], [245], [246].

$$\mathrm{D}_{\mathrm{ox}}^{+} = \mathrm{D}_{\mathrm{ox}} f^{+} \tag{5.38}$$
$$\mathrm{D}_{\mathrm{ox}}^{0} = \mathrm{D}_{\mathrm{ox}} f^{0} \tag{5.39}$$
$$\mathrm{D}_{\mathrm{ox}}^{-} = \left(\mathrm{D}_{\mathrm{it}} + \mathrm{D}_{\mathrm{ox}}\right) f^{-} \tag{5.40}$$
$$\tag{5.41}$$

where $\mathrm{D}_{\mathrm{ox}}^{+}, \mathrm{D}_{\mathrm{ox}}^{0}, \mathrm{D}_{\mathrm{ox}}^{-}-$ are the occupied densities of the positive, neutral, and negative amphoteric traps, and f^{+}, f^{0}, f^{-} are the probabilities of the occupation of the positive, neutral, and negative amphoteric traps, respectively.

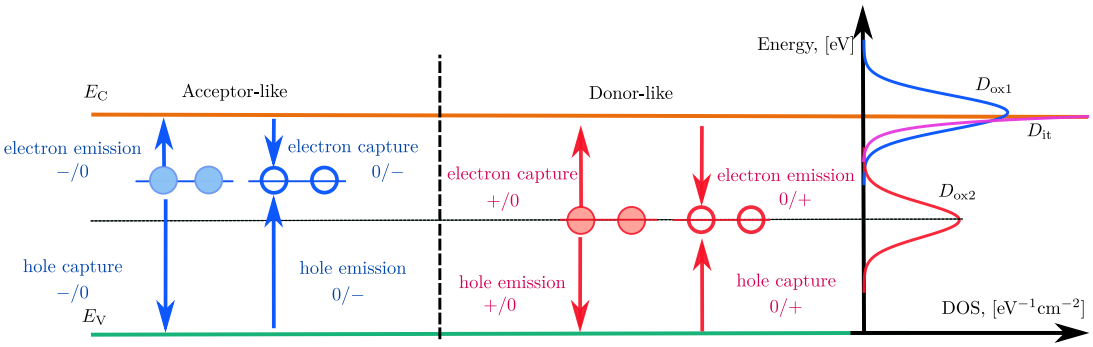


Figure 5.5.: Schematic plot of the amphoteric DOS and configuration coordinate diagram.

$$f^{-} = 1 - f^{0} - f^{+} \tag{5.42}$$

The total charge generated by the amphoteric traps was deduced from the right-hand side of the Poisson's equation. The overall charge value is determined by

$$Q_t = q \int_{E_{\mathrm{V}}}^{E_{\mathrm{C}}} \left(\mathrm{D}_{\mathrm{ox}}^{+} - \mathrm{D}_{\mathrm{ox}}^{-}\right) dE \tag{5.43}$$

The application of the amphoteric model to explain the BTI at the SiC/SiO_2 interface is contentious and its origins remain ambiguous. Thus, to better explain the behavior of the defects in the SiC/SiO_2 interface that prevail in BTI, we use a multi-level NMP model demonstrating significant recovery.

5.7. 4-state Non-Radiative-Multiphonon (NMP) model

Because the SRH model demonstrates a limited temperature dependence of τ_c and small time constants, it was modified by Kirton and Uren [247] by incorporating a term with field-independent energy barriers, ΔE_b. The introduction of these barriers

has been motivated by the theory of non-radiative multi-phonon transitions (NMP) process [18], [248].

The time-dependent effective threshold voltage V_{th} can be expressed as a function of the randomly changing occupancy of the defects over time. However, in a large device, the sum of all trap occupancies behaves predictably. Within the charge sheet approximation it reads: [18]:

$$\mathrm{V_{th}}\left(\mathrm{V_G}, t, T\right) = \mathrm{V_{th0}} - \frac{\mathrm{Q_{it}^{\mathit{i}}}\left(\mathrm{V_G}, t, T\right) + \mathrm{Q_{ox}}\left(\mathrm{V_G}, t, T\right) + \mathrm{Q_{fix}}\left(T\right)}{\mathrm{C_{ox}}} \tag{5.44}$$

where $\mathrm{C_{ox}} = \epsilon_0 \epsilon_{\mathrm{r}} / t_{\mathrm{ox}}$ is the capacitance per area and t_{ox} is the oxide thickness. If the interface defects are too fast, $\mathrm{Q_{it}}\left(\mathrm{V_G}, t\right)$ is written as $\mathrm{Q_{it}}\left(\mathrm{V_G}\right)$. The charge of the bulk oxide defects $\mathrm{Q_{fix}}$ under most conditions does not depend on the time and gate voltage sweep $\mathrm{V_G}$. For oxide defects that are located close to SiC/SiO_2, i.e. border traps, and too slow to follow the gate bias change, we can write (the temperature T dependence is hidden for simplicity):

$$\mathrm{Q_{ox}}\left(\mathrm{V_G}, t\right) = q \frac{1 - x_t / t_{\mathrm{ox}}}{WL} \eta_r f\left(t\right) \tag{5.45}$$

or for an evaluation of the trap depth-dependent contribution of a defect

$$\mathrm{V_{th,i}} = -q \frac{1}{C_{\mathrm{ox}}} \left(1 - \frac{x_{\mathrm{t}}}{t_{\mathrm{ox}}}\right) \tag{5.46}$$

where $f\left(t\right)$ is the trap occupancy probability, x_t is the depth of the defect in the oxide, and W and L are the channel width and transistor length, respectively. To evaluate the deviation from the charge sheet approximation, the empirical parameter η_r which can have values up to 10, was introduced [18].

For each defect state, occupancy was calculated using the chemical master equation:

$$\frac{df_i}{dt} = -f_i \sum_{j \neq i} k_{ij} + \sum_{j \neq i} f_j k_{ji} \tag{5.47}$$

$$\sum_i f_i = 1 \tag{5.48}$$

where $i, j \in \{1, 1', 2, 2'\}$ and k_{ij} are the transition rates between states i and j. The trap charge depends on the occupation probabilities of the states f_i and their corresponding charges q_i [232].

In general, the transition rates from state i to state j can be written as [249]:

$$k_{ij}\left(E\right) = \int_{-\infty}^{\infty} D\left(E\right) f\left(E\right) A_{ij}\left(E\right) \mathrm{e}^{-\varepsilon_{ij}(E)/(k_{\mathrm{B}}T)} dE \tag{5.49}$$

The configuration coordinate diagram for the four-state NMP model incorporating valence and conduction band transitions is shown in Fig. 5.6 [249].

The model is based on neutral state 1 and positively charged state 2, with the corresponding positions q_1 and q_2 in the configuration coordinate diagram, respectively. Each charge state has an additional metastable state, $1'$ and $2'$. The transitions between 1 and $1'$ and between 2 and $2'$ are structural reconfigurations across an energy barrier that are accurately characterized by the Arrhenius law. Consequently, the transition rates of the relaxation processes $k_{11'}$, $k_{1'1}$, $k_{22'}$, $k_{2'2}$ are independent of the bias [18], [92], [232]. The energy minima of V_1 correspond to the trap energy level E_t. The energy minima of V_2 correspond to the conduction and valence bands, respectively. The transitions between 1 and $2'$ and between 2 and $1'$ involve the exchange of charges with carriers in the MOSFET channel and the interface or border traps.

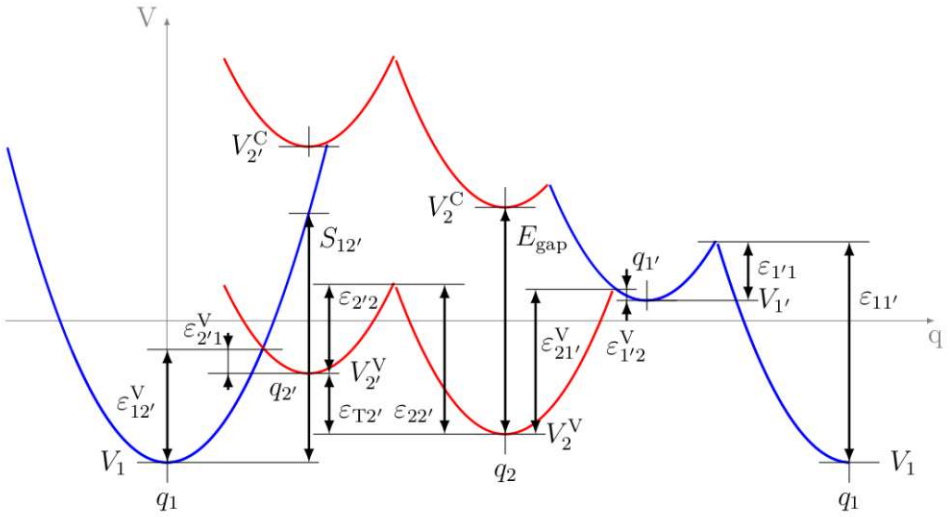


Figure 5.6.: Schematic configuration coordinate diagram illustrating all states of the NMP four-state model incorporating valence and conduction band transitions with all significant barriers and energy levels. From *Rzepa, Gerhard. Microscopic modeling of NBTI in MOS transistors. Diss. 2013. p. 25* [249].

Table 5.2: Important NMP parameters in the configuration coordinate diagram.

Symbol	Description	Unit
$\varepsilon_{12'}^{C}$	Energy barrier for calculating the capture rate w.r.t conduction band	eV
$\varepsilon_{2'1}^{C}$	Energy barrier for calculating the emission rate w.r.t conduction band	eV

Continued on next page

Table 5.2: Important NMP parameters in the configuration coordinate diagram. (Continued)

Symbol	Description	Unit
$\varepsilon^{\mathrm{V}}_{12'}$	Energy barrier for calculating the capture rate w.r.t valance band	eV
$\varepsilon^{\mathrm{V}}_{2'1}$	Energy barrier for calculating the emission rate w.r.t valance band	eV
$E^{\mathrm{s}}_{\mathrm{C}}$ ($V_2^{\mathrm{C.min}}$)	Conduction band ($E^{\mathrm{s}}_{\mathrm{V}} + E_{\mathrm{g}}$)	eV
$E^{\mathrm{s}}_{\mathrm{V}}$ ($V_2^{\mathrm{V.min}}$)	Valance band (ref. 0)	eV
E_{t} (V_1^{min})	Trap energy level ($E^{\mathrm{s}}_{\mathrm{V}} + E_{\mathrm{t}}$)	eV

Based on this model and its energy barriers, the transition rates can be rewritten as [249]:

$$k_{12'} = k^{\mathrm{C}}_{12'} + k^{\mathrm{V}}_{12'} = n v_{\mathrm{th,n}} \sigma_{0,n} \lambda_n \mathrm{e}^{-\beta\left(\varepsilon^{\mathrm{C}}_{12'} - E^{\mathrm{s}}_{\mathrm{C}} + E_{\mathrm{F}}\right)} + p v_{\mathrm{th,p}} \sigma_{0,p} \lambda_p \mathrm{e}^{-\beta \varepsilon^{\mathrm{V}}_{12'}} \tag{5.50}$$

$$k_{2'1} = k^{\mathrm{C}}_{2'1} + k^{\mathrm{V}}_{2'1} = n v_{\mathrm{th,n}} \sigma_{0,n} \lambda_n \mathrm{e}^{-\beta \varepsilon^{\mathrm{C}}_{2'1}} + p v_{\mathrm{th,p}} \sigma_{0,p} \lambda_p \mathrm{e}^{-\beta\left(\varepsilon^{\mathrm{V}}_{2'1} - E^{\mathrm{s}}_{\mathrm{V}} - E_{\mathrm{F}}\right)} \tag{5.51}$$

$$k_{21'} = k^{\mathrm{C}}_{21'} + k^{\mathrm{V}}_{21'} = n v_{\mathrm{th,n}} \sigma_{0,n} \lambda_n \mathrm{e}^{-\beta \varepsilon^{\mathrm{C}}_{21'}} + p v_{\mathrm{th,p}} \sigma_{0,p} \lambda_p \mathrm{e}^{-\beta\left(\varepsilon^{\mathrm{V}}_{21'} - E^{\mathrm{s}}_{\mathrm{V}} - E_{\mathrm{F}}\right)} \tag{5.52}$$

$$k_{1'2} = k^{\mathrm{C}}_{1'2} + k^{\mathrm{V}}_{1'2} = n v_{\mathrm{th,n}} \sigma_{0,n} \lambda_n \mathrm{e}^{-\beta\left(\varepsilon^{\mathrm{C}}_{1'2} - E^{\mathrm{s}}_{\mathrm{C}} + E_{\mathrm{F}}\right)} + p v_{\mathrm{th,p}} \sigma_{0,p} \lambda_p \mathrm{e}^{-\beta \varepsilon^{\mathrm{V}}_{1'2}} \tag{5.53}$$

$$k_{11'} = \nu_0 \mathrm{e}^{-\beta \varepsilon_{11'}} \tag{5.54}$$

$$k_{1'1} = \nu_0 \mathrm{e}^{-\beta \varepsilon_{1'1}} \tag{5.55}$$

$$k_{22'} = \nu_0 \mathrm{e}^{-\beta \varepsilon_{22'}} \tag{5.56}$$

$$k_{2'2} = \nu_0 \mathrm{e}^{-\beta \varepsilon_{2'2}} \tag{5.57}$$

where $\sigma_{0,n}, \sigma_{0,p}$ are the capture cross-sections; λ_n, λ_p are the tunneling factors; n, p are the carrier concentrations; $v_{\mathrm{th,n,p}}$ are the thermal velocities of the electrons and holes, respectively; and $\beta = (k_{\mathrm{B}} \cdot T)^{-1}$. The transition rates of the relaxation processes ($k_{11'}, k_{1'1}, k_{22'}$ and $k_{2'2}$) are independent of the gate bias.

For the four-state NMP model, the barrier $\varepsilon_{\mathrm{T}2'}$ must be larger than 0 eV, and V_1' must be larger than V_1 to ensure the metastable nature of states $1'$ and $2'$. For 4H-SiC/SiO$_2$ we did not observe metastable states; therefore, we modified the four-state NMP model to a two-state NMP model. In this case, $\varepsilon_{\mathrm{T}2'}$ must be equal to 0 eV, V_1' must be equal V_1 and V_2' must be equal V_2.

The charge trapping barriers were approximated from the strong quadratic electron-phonon coupling regimes. The intersection point of the parabolas of the states i and j gives the energy barrier for calculating capture/emission rates [21], [250]:

$$S_{ij} = \mathbf{S}_{ij}\hbar w = c_i \left(q_j - q_i\right)^2 \tag{5.58}$$

$$R_{ij}^2 = \frac{c_i}{c_j} \tag{5.59}$$

$$\Delta E_{ij} = V_j^{\min} - V_i^{\min} \tag{5.60}$$

$$\varepsilon_{ij} = \frac{S_{ij}}{\left(R_{ij}^2 - 1\right)^2} \left(1 - R_{ij}\sqrt{\frac{S_{ij+\Delta E_{ji}}\left(R_{ij}^2 - 1\right)}{S_{ij}}}\right)^2 \tag{5.61}$$

where $\mathbf{S}_{ij}$ is the Huang-Rhys factor, R_{ij} curvature relation.

The trap-level of a defect shifts with the applied gate voltage, depending on the trap position.

$$E_{\mathrm{t}}\left(V_{\mathrm{gs}}\right) = \frac{-q\left(V_{\mathrm{gs}} - \psi_{\mathrm{s}}\right)}{t_{\mathrm{ox}}} x_{\mathrm{t}} + E_{\mathrm{t}}\left(0\right) \tag{5.62}$$

$$\tag{5.63}$$

where ψ_{s} is the surface potential, x_{t} is the position of the trap at the interface, and $E_{\mathrm{t}}\left(0\right)$ is the trap level at zero gate bias.

5.8. Combined REDR-NMP Model

The existence of different trap types indicates that the conventional four-state NMP model is insufficient to accurately represent the trap kinetics observed in 4H-SiC MOSFETs under GSI conditions, necessitating modifications for improved accuracy. Three defect types were assumed to better understand GSI. First, defects of type **A** are pumped during the GSI, at which site the pumped energy is released in the form of recombination events. This occurs because, during each recombination event, energy approximately equal to the SiC bandgap must be dissipated. This process leads to the stimulation of local vibrational modes at the defect site, which may subsequently initiate a local reaction. Such recombination-enhanced defect reactions (REDRs), or "phonon kicks," have been observed previously, particularly for wide-bandgap semiconductors, and their features are consistent with those observed during the GSI. Second, defects of type **B** (newly created defects with $\mathrm{E_t}$ adjacent to E_{C}). Third, species of type **X** are intermediate species that transfer the released energy from site **A** to defects **B** and activate them. This model predicts that saturation will occur at times $1/c$ (where c is a rate) despite the concentration of defect **A**. The reaction at site **B** was reduced by species **X** released from **A**. Alternatively, according to optical experiments, species **X** might be a photon that can be absorbed at site **B** and initiate both forward and backward reactions. By switching the MOSFET between accumulation and inversion, holes and electrons are provided [23].

The conventional nonradiative multiphonon (NMP) model for charge trapping was reformulated to describe REDR for a donor-like or acceptor-like defects with two states, 1 and 2 (neutral/positive or neutral/negative), or A^0 and A^* respectively, see Fig. 5.7

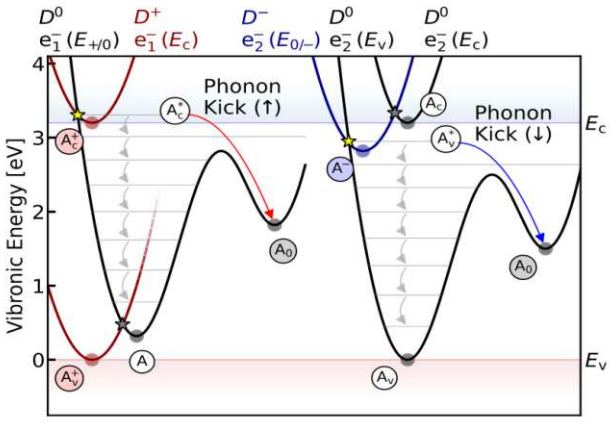


Figure 5.7.: PECs and states for an amphoteric defect A. One of the two intersection points leads to a large energy release (yellow stars). Once in A^*, the defect normally relaxes thermally to A or rarely via a phonon kick to A^0. On the left, the $+/0$ transitions are shown, whereas the $0/$ transitions are on the right. According to *Grasser T., et al. "Gate switching instability in silicon carbide MOSFETs—Part II: Modeling." IEEE Transactions on Electron Devices (2024), p. 4219* [23].

At quasi-equilibrium, the three-state model reduces to an effective two-state model with the effective rates as follows [23]:

$$k_{21}^{\text{eff}} = k_{A^+A^*} = n\sigma_n v_{\text{th}} \mathrm{e}^{-\beta\varepsilon_{21}^{\text{C}}} \tag{5.64}$$

$$k_{12}^{\text{eff}} = k_{A^*A^+} \mathrm{e}^{-\beta\varepsilon_{12}^{\text{C}}} = N_{\text{c}}\sigma_n v_{\text{th}} \mathrm{e}^{-\beta\varepsilon_{12}^{\text{C}}} \tag{5.65}$$

$$\tag{5.66}$$

where n is the electron concentration in the SiC channel, σ_n is the capture cross section, v_{th} is the thermal velocity, $\beta = 1/(k_{\text{B}}T)$, $\varepsilon_{12}^{\text{C}}$ is the barrier from state 2 to 1 (or from A^* to A^+) given by the intersection of the PECs for an electron originating from E_{C}, $\varepsilon_{12}^{\text{C}}$ is the barrier from state 1 to state 2 (or from A^+ to A^*).

The "source" defect **A** must possess energy levels that extend to the valence band E_{V} (type $+/0$), as SiC MOSFETs exhibit a substantial presence of such donor-like defects, which contribute to hysteresis and stretch-out in $C-V$ measurements. Given that the GSI is influenced by both V_{H} and V_{L}, and considering the observed dependence on the fall time, defect **A** is amphoteric, featuring an additional acceptor-like $0/-$ energy level close to E_{C}. This implies that the PECs exhibit additional transition rates at intersection points (yellow stars), not only from $D^+ \rightarrow D^0$ but also from $D^0 \rightarrow D^-$ (refer to Fig. 5.7 and Fig. 5.8) [23]. During the pumping process, a type **A** defect

releases an intermediate species **X**, which may be hydrogen, carbon, subsequently causing degradation at a nearby site by activating the precursor defect $\mathbf{B}_0$ into its active form **B**. With the continued release of **X**, some active **B** defects are converted into inactive $\mathbf{B}_2$ defects, manifesting as a reversal of degradation, as illustrated in Fig. 5.8 [23], [207].

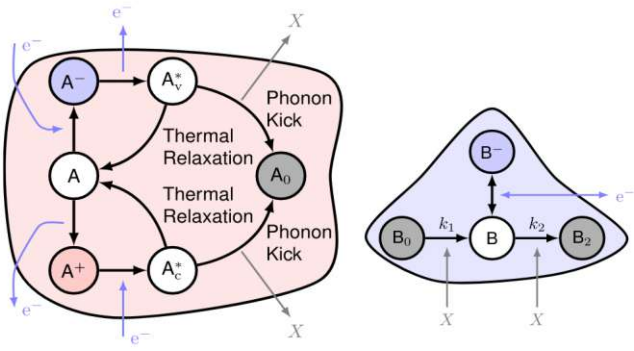


Figure 5.8.: States and reactions of defect **A** (left) and **B** (right). Red is positively charged and blue negatively. Electron (e^-) exchange with E_C and E_V leads to a change in the charge state. Occasional phonon kicks take **A** to the precursor state $\mathbf{A}_0$, which releases **X**. **X** triggers reactions from $\mathbf{B}_0$ to the active **B** as well as to the again inactive $\mathbf{B}_2$, which are assumed to be unidirectional because of the required high temperatures to anneal GSI damage. Based on *Grasser, Tibor et al. "Gate switching instability in silicon carbide MOSFETs—Part II: Modeling." IEEE Transactions on Electron Devices (2024), p 4219* [23].

5.9. 2-state Non-Radiative-Multiphonon Model

The two-state model characterizes the BTI well during stress and recovery in 4H-SiC MOSFETs [251] as shown in Fig. 5.9 [252]. The two-state model represents a specific instance of the four-state model and can effectively describe the charge trapping effects. Although the four-state model includes all transitions, the two-state model excludes pure thermal transitions and has been successfully applied and demonstrated in [21], [169], [194], [227], [252]. A single defect is described in the 4-state NMP model with nine parameters, whereas a simple 2-state NMP defect that does not consider metastable states can be described using three instead of nine parameters. Additionally, the two-state approximation for reliable lifetime extrapolation effectively represents degradation in a physical context.

The simplification and transformation includes several steps: 1) we assume that the no metastable states are occurs due to minimization the related barriers, 2) we assume normal distributions of E_T and S and uniform trap distributions in space x_T, R is approximated to be constant and equal 1, 3) due to we have different trap types, the each type has his own E_T, S, x_T and σ's parameter set 4) where individual contribution of ΔV_{th} shifts will be sum in post-processing mode (we assume no charge exchange between traps, only through the channel path).

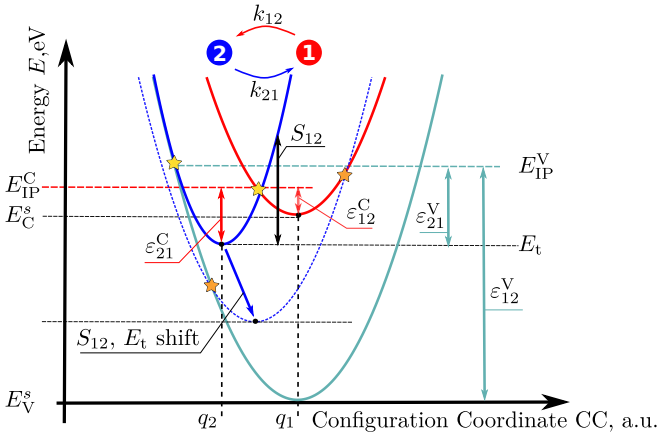


Figure 5.9.: Schematic configuration coordinate diagram with the potential energy surface along the transition path for neutral state 1 and charged state 2. The capture path was 1 $\rightarrow$ 2, with the corresponding energy barriers ε_{12}^{C} and ε_{12}^{V}. The emission path was 2 $\rightarrow$ 1, with corresponding energy barriers ε_{21}^{C} and ε_{21}^{V}. The high values of these barriers depend on the parabolic intersection points E_{IP}^{C} and E_{IP}^{V}. The capture and emission barriers are the main trap parameters that can be modified by varying the S and E_t values, respectively. The curvature ratio was mostly equal one 1.

Table 5.3: Important NMP parameters to calculate the capture/emission barriers.

Symbol	Description	Unit
N_t	Trap concentration	cm^{-3}
E_t	Trap energy level	eV
x_t	Trap transition layer	nm
σ_E	Trap energy distribution	eV
S_{12} (or S)	Relaxation energy	eV
σ_S	Relaxation energy distribution	eV
R	Curvature ratio	1
σ_R	Curvature ratio distribution	1

5.9.1. Capture and Emission Energy Barriers. Impact of the Relaxation energy S

According to the two-state NMP model, the capture and emission energy barriers ($\varepsilon_{ij,ji}^{C,V}$) govern the dynamics of the trapped charges. One of the most significant impacts of these energy barriers is the relaxation energy S (where $S = S\hbar\omega$, S is Huang-Rhys factor, ω is the phonon frequency). For example, Fig. 5.10 shows a configuration coordinate diagram with two S values: 0.5 eV on the left and 5 eV on the right.

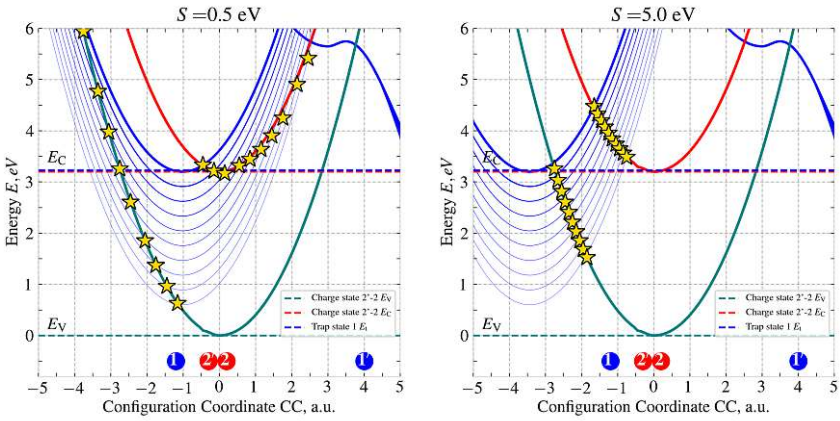


Figure 5.10.: Schematic configuration coordinate diagram with potential energy surface along the transition path for neutral state 1 and charged state 2 at two S values (0.5 eV on the left and 5 eV on the right). Note that we did not use the metastable states, where the energy barrier between 2 and 2′ is zero and the energy barrier between 1 and 1′ is high to avoid transitions. The stars represent the crossing points of the conduction and valence bands with the trap potential energy surfaces, which shift owing to the trap energy levels or applied gate voltage bias. At higher S values, the minima of the trap energy level shift toward lower configuration coordinates, which significantly affects the capture and emission barriers.

Assuming that the positive state is denoted by 2 and the neutral state is denoted by 1, the time constants are defined as $\tau_c = \tau_{12}$ with the corresponding capture energy barriers ($\varepsilon_{12}^{\mathrm{C,V}}$), as shown in Fig. 5.9.

In Fig. 5.11, we observe the extracted capture and emission barriers for the two S values. When the trap energy level is close to the conduction band and V_{gs} =0 V, the intersection with the conduction band for electron exchange has a smaller $\varepsilon_{12'}^{\mathrm{C}}$ barrier (left) than the intersection with the valence band $\varepsilon_{12'}^{\mathrm{V}}$ barrier (right) for hole exchange. Simultaneously, traps with smaller S values exhibited faster electron-capture dynamics because of a lower capture barrier (see Fig. 5.11, left, red lines). In contrast, traps with larger S values capture more slowly because they are associated with higher capture barriers (see Fig. 5.11, left, blue lines). With an increase in the voltage V_{gs}, the emission energy behavior becomes the opposite at different S values. This leads to different electron-phonon coupling regimes, which are based on the S value for electron emission from and capture by the traps. The emission barrier increased when S was small and decreased when S was high, when the effective trap energy level shifted towards the valence band. The strong asymmetry between the capture and emission barriers inherent to the NMP model enabled us to represent the hysteresis width in our simulation. Finally, by fitting the S parameter, we can obtain three regimes: strong electron-phonon coupling when V_{gs} is increased, and the increase in $\varepsilon_{12'}^{\mathrm{C}}$ is always negative, positive weak electron-phonon coupling when V_{gs}, and an increase in $\varepsilon_{12'}^{\mathrm{C}}$ is always negative, negative weak electron-phonon coupling when V_{gs} decreases, and $\varepsilon_{12'}^{\mathrm{C}}$ decreases. This implies that the hysteresis width behavior can be controlled at different temperatures and gate voltages by up and down sweeps [18], [21], [249] and [92], [253].

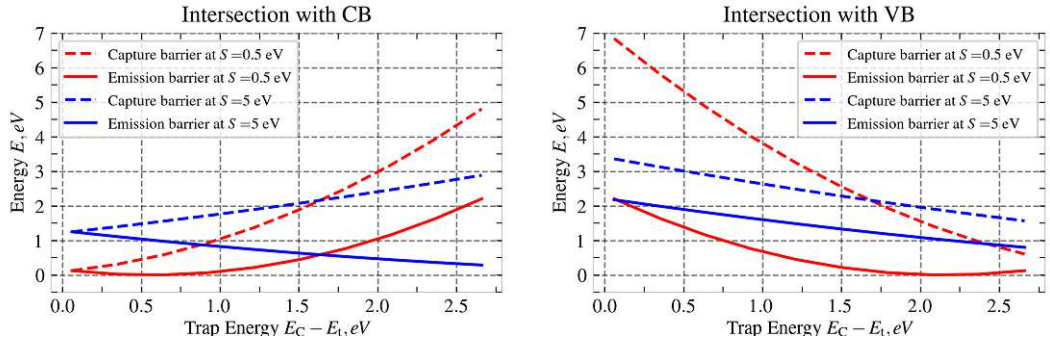


Figure 5.11.: The calculated capture and emission barriers at two S values with respect to the intersection points with conduction (left) and valance (right).

5.9.2. Simulation of Hysteresis Behavior in $I_d - V_{gs}$ Characteristics

The $I_d - V_{gs}$ curves of the planar and trench 4H-SiC MOSFETs demonstrate different hysteresis shapes during the up and down gate voltage sweeps, as shown in Fig. 4.23. The previously mentioned hysteresis effect is caused by traps that store charge states during the sweeps. The shape or behavior of these curves depends on many trap parameters, such as the density of states (DOS) or the initial trap charge. The main parameters of the two-state NMP model in Table 5.3 allow us to model this shape with good accuracy. Fig. 5.12 illustrates the planar and trench $I_d - V_{gs}$ curves that were simulated using only the NMP model.

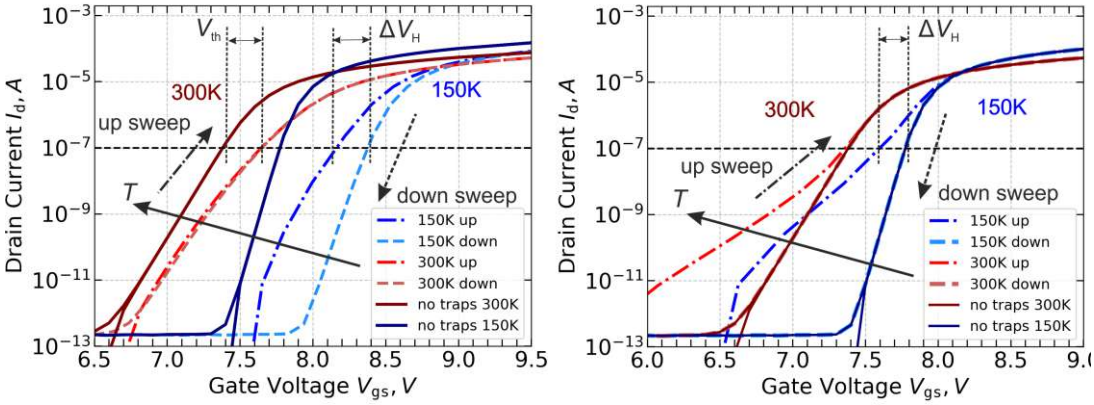


Figure 5.12.: Illustration of simulated $I_d - V_{gs}$ characteristics of 4H-SiC MOSFETs using only the NMP model for border trap dynamics. Left: planar 4H-SiC MOSFET at 150 K (blue) and 300 K (red). Right: Trench 4H-SiC MOSFET. The solid lines represent the ideal $I_d - V_{gs}$ curves without traps. The dash-dotted line represents the up sweep curve, whereas the dashed line indicates the down sweep curve. The hysteresis width is determined by the difference between V_{th} values during the downward and upward sweeps at the reference drain currents. The hysteresis width decreased at elevated temperatures for all devices, and the shape varies as shown in Fig. 4.23.

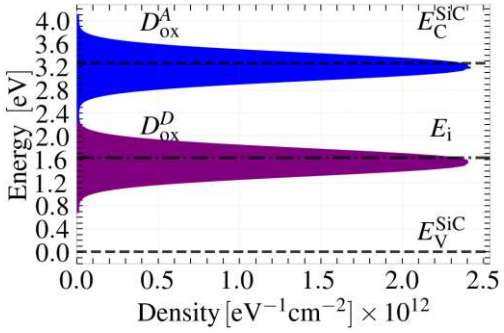


Figure 5.13.: Sketch of a trap density of states for planar (blue) and trench (purpure) 4H-SiC MOSFETs.

Table 5.4 shows examples of the NMP parameters used to simulate the trap kinetics of planar and trench MOSFETs. Examples of the density of acceptor-like trap states used for planar devices and the density of donor-like trap states used for trench devices are presented in Fig. 5.13.

Table 5.4: Example of NMP parameters for simulating the $I_d - V_{gs}$ curves of planar and trench 4H-SiC MOSFETs.

Symbol	Planar	Trench	Unit
Trap type	acceptor-like $0/-1$	donor-like $1/0$	
N_t	2.4×10^{12}	2.4×10^{12}	cm^{-2}
E_t	E_C	$E_g/2$	eV
x_t	1	1	nm
σ_E	0.2	0.2	eV
S_{12} (or S)	0.8	2.2	eV
σ_S	0.1	0.1	eV
R	1	1	1
σ_R	0.01	0.01	1

The simulated $I_d - V_{gs}$ curves for the planar and trench 4H-SiC MOSFETs are shown on the left side of Fig. 5.12. For planar MOSFETs, the trap kinetics may be explained by the predominant accelerator-like $(0/-1)$ traps located near the conduction band $(E_t \approx E_C)$. A positive shift in V_{th} or PBTI in relation to the ideal $I_d - V_{gs}$ curves indicates that the traps become more negatively charged under both temperature conditions. During the up-gate voltage sweep, when $V_{gs} < V_{th}$, the capture and emission barriers were approximately equal $(\varepsilon_c^C \approx \varepsilon_e^C)$ and small, respectively, resulting in high rates at elevated temperatures. In this regime, electrons are emitted into the channel, traps are generally unoccupied, and the shift in V_{th} is small. Compared to the low temperature, the capture and emission rates were small, and the shift in V_{th} was more significant. When $V_{gs} > V_{th}$, E_t is set below the Fermi level of the channel,

resulting in the capture of electrons by defects, thereby leading to trap saturation.

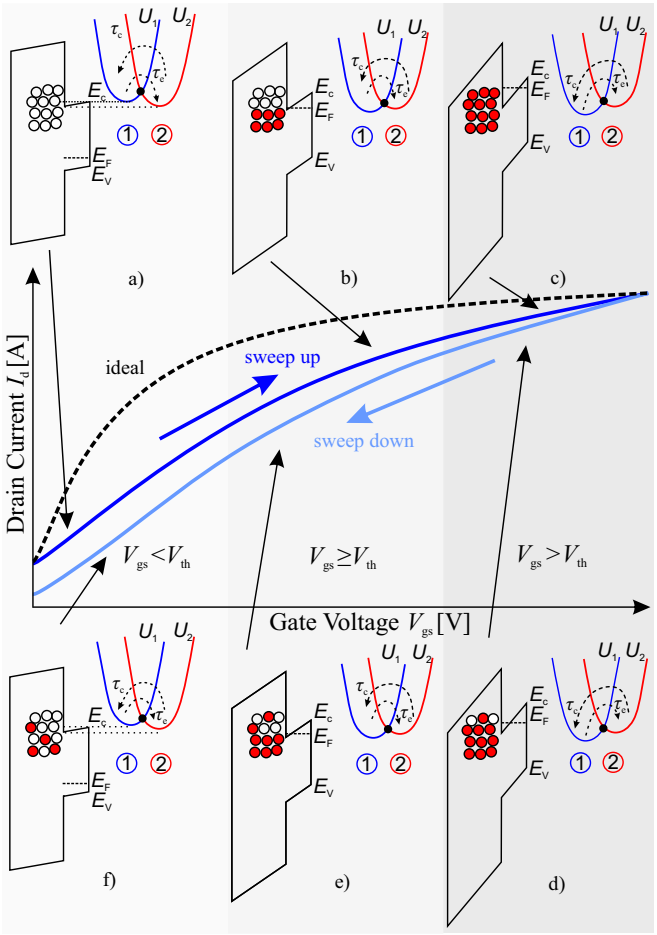


Figure 5.14.: The hysteresis of the transfer characteristics of the 4H-SiC MOSFET is schematically shown (center). In addition, the band diagrams of the SiC/SiO_2 interface region with acceptor-like border traps close to $E_{c,SiC}$ are schematically shown at different times during the gate bias up and down sweeps (a)–(f). The harmonic approximations of the potential energy surfaces for the average defects charged state 1 (blue) and neutral state (red), that is, $E_{c,SiC}$ are displayed, showing the energetic barriers for calculating the capture and emission times, which are determined by the intersection point (black dot). This barrier is changed by shifting the parabolas relative to each other by altering the gate bias. Initially, the capture time was large, that is, a large capture barrier and defects remained in the neutral state (a). With increasing gate bias, the capture barrier is reduced, and more defects become negatively charged, thereby shifting the $I_d - V_{gs}$ curve towards a more positive bias (b)–(c). At the subsequent down sweep, the barrier for electron emission towards the channel is reduced again, however, some of the previously charged defects do not fully discharge during the down sweep, as their emission time constants exceed the sweep duration, even at lower biases (d)-(f). The strong asymmetry between the capture and emission times inherent to the NMP model enabled us to capture this effect in our simulation. From: [99]

During the downward gate voltage sweep, the traps retained their charge state, resulting in hysteresis, particularly at lower temperatures. The hysteresis widths at the two reference low and high drain currents were largely consistent with the measurements. The configuration of the planar MOSFET that exhibits electron trapping is shown in Fig. 5.14. The simulated $I_d - V_{gs}$ curves for the trench 4H-SiC MOSFETs are shown on the right side of Fig. 5.12. Donor-like (+1/0) traps located in the mid-gap were the predominant features of this device. A negative shift in V_{th}, or NBTI, relative to the ideal $I_d - V_{gs}$ curves indicates that the traps were initially positively charged at both temperatures. During the up-gate voltage sweep, when $V_{gs} < V_{th}$, the emission barrier was smaller than the capture barrier ($\varepsilon_e^V < \varepsilon_c^V$), resulting in high rates at elevated temperatures. As the gate voltage increased and $V_{gs} > V_{th}$, electrons were injected into the channel, resulting in the traps becoming positively charged. When $V_{gs} > V_{th}$, electrons are captured by the defects, resulting in charge neutralization and subsequent trap emptying. During the down gate voltage sweep, the curves approached the ideal $I_d - V_{gs}$ as the traps remained neutral [99].

5.9.3. Effect of NMP Parameters on Hysteresis Width Across Temperatures

In the previous section, the influence of trap energy level and trap type on the $I_d - V_{gs}$ shape was discussed. To investigate the hysteresis width at different temperatures, the influence of the other parameters of the NMP model in Table 5.3 is presented. In Fig. 5.15, the variation in the width of hysteresis is illustrated within the temperature range of 150–450 K, relative to the traps position from the surface.

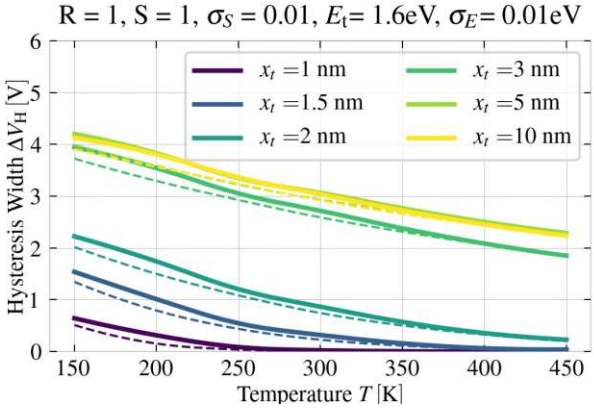


Figure 5.15.: The hysteresis width at temperature range from (150–450) K at trap position from surface, x_t. The E_t, S_{12} and R_{12} parameters are constant. Note that The dashed line indicates the minimum drain reference current, while the solid line denotes the maximum drain reference current at which the hysteresis width was determined. Two reference drain currents $I_d^{ref1} < I_d^{ref2}$ were used to determine the hysteresis widths ΔV_{H1} (solid) and ΔV_{H2} (dashed). Note that $E_g/2$ =0 eV means that $E_t = E_C$ =1.6 eV.

The mean number of oxide defects N resulting from a two-state NMP defect band was calculated as [250]:

$$N_t = WLN_{ox}\left(x_{t,max} - x_{t,min}\right) \tag{5.67}$$

where W and L are the effective gate oxide width and length, respectively, and N_{ox} is the defect concentration located away from the channel interface. According to (5.67), an increased number of defects correlates with a broader transition region, resulting in an expanded hysteresis width. This is an adjustable coefficient of the constant part of the hysteresis width.

The variation in the width of the hysteresis is illustrated in Fig. 5.16 within the temperature range of 150–450 K in relation to the energy level of the traps. In the case of an n-MOSFET subjected to a positive gate voltage sweep in both the upward and downward directions, the traps near the valence band did not affect the hysteresis width. Evidently, for planar MOSFETs, traps located near the conduction band better represent hysteresis behavior. In addition, for the constant part of the hysteresis width, traps positioned near the mid-gap with a broader distribution are beneficial.

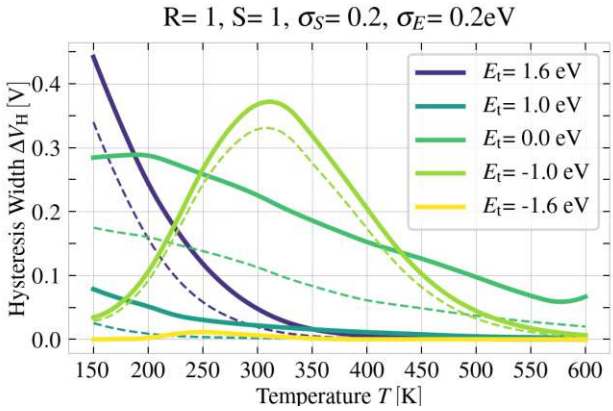


Figure 5.16.: The hysteresis width at temperature range from (150–600) K at trap energy level. The S_{12} and R_{12}, x_t, parameters are the constant (dashed line $I_{d,ref1}$ = 1e-8A, solid line $I_{d,ref2}$ = 1e-7A). Note that $E_g/2$ =0 eV means that $E_t = E_C$ =1.6 eV and $E_t = E_V$ =−1.6 eV.

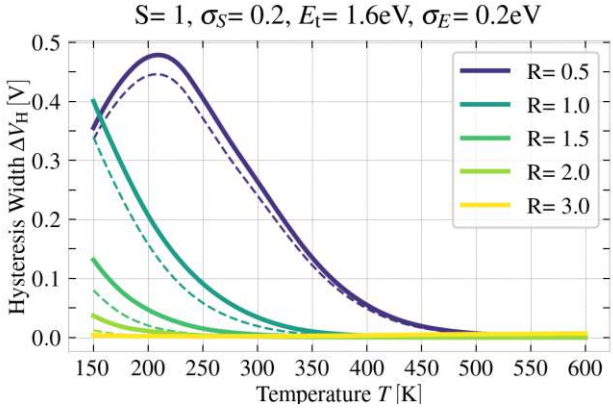


Figure 5.17.: The hysteresis width at temperature range from (140–600) K at R_{12}. The E_t, S_{12} and x_t parameters are the constant. Note: the R should be constant and equal 1 (dashed line $I_{d,ref1}$ = 1e-8A, solid line $I_{d,ref2}$ = 1e-7A). Note that $E_g/2$ =0 eV means that $E_t = E_C$ =1.6 eV.

The subsequent parameter from the NMP model that affects the hysteresis width is

denoted as R, as shown in Fig. 5.17. This parameter adjusts the maximum hysteresis peak to higher temperatures. For simplicity, it is advisable to maintain this parameter at 1.

Another significant parameter is S. Fig. 5.18a-d, shows the relationship between the hysteresis width and S together with the trap energy level over a wide temperature range. The effect of this parameter on the $I_d - V_{gs}$ characteristics is discussed in detail in the previous section. As the S value increased, the hysteresis peak shifted toward higher temperatures, while the amplitude decreased.

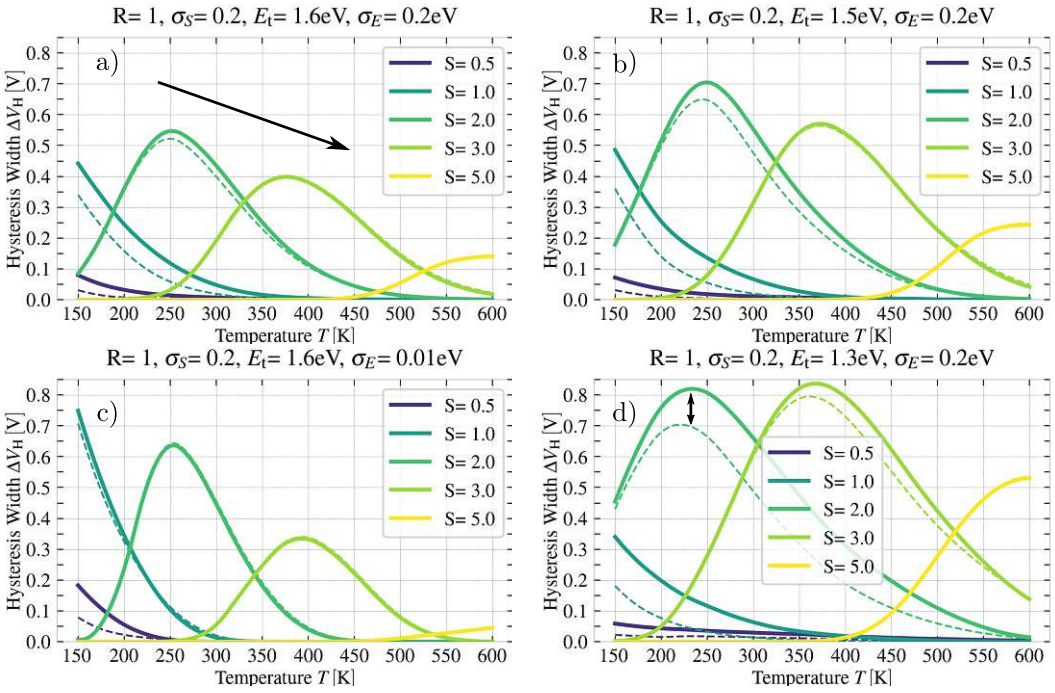


Figure 5.18.: The hysteresis width at temperature range from (150–600) K at S_{12} in eV. The E_t, R_{12} and x_t parameters are the constant (dashed line $I_{d,ref1}$ = 1e-8A, solid line $I_{d,ref2}$ = 1e-7A). d) The increased distance between the solid and dashed lines indicates that the hysteresis width is non-uniform across varying reference drain currents. Note that $E_g/2$ =0 eV means that $E_t = E_C$ =1.6 eV and E_t =1.3 eV means E_C−0.3 eV.

At lower S values, decay predominantly occurs below room temperature, as reported in various publications [252], [254]. The elevated S values indicate an increase in the hysteresis width at the highest temperatures, which can be utilized for simulation purposes and to elucidate the observed anomalous increase in the hysteresis, as illustrated in Fig. 4.3. This is because of the different electron-phonon coupling regimes, which influence the capture and emission barriers. The broader distribution of the hysteresis width is associated with a wider trap energy distribution, as illustrated in Fig. 5.18a, b, and d, in contrast to Figure Fig. 5.18c. If E_t shifts to the mid-gap with a higher S value, the difference in hysteresis between the low and high reference drain currents increases. This indicates that the curvatures of $I_d - V_{gs}$ for the up- and down-sweeps are different, as shown in Fig. 5.18d.

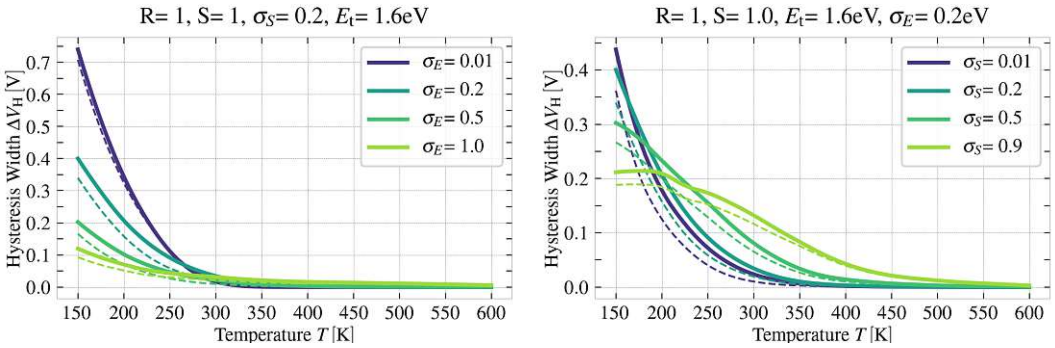


Figure 5.19.: The hysteresis width at temperature range from 140–450 K at various sweep rate (dashed line $I_{\mathrm{d,ref1}}$ = 1e-8A, solid line $I_{\mathrm{d,ref2}}$ = 1e-7A).

The distributions of both parameters, S and E_{t} are correlated with the distributions of the amplitude and hysteresis width, as shown in Fig. 5.19.

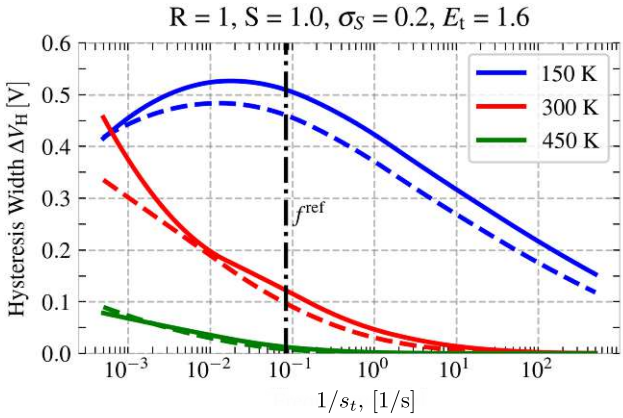


Figure 5.20.: The hysteresis width at temperature range from 140–450 K at various sweep rate. At a very long sweep rate, we did not observe any hysteresis effect because the charges had sufficient time to be emitted to the channel, and the traps were empty. If the traps are too slow (especially at low temperatures) at a lower sweep rate, the hysteresis width decreases because the charges cannot be captured by the traps, and the traps maintain their initial states during sweeps. Two reference drain currents $I_{\mathrm{d}}^{\mathrm{ref1}} < I_{\mathrm{d}}^{\mathrm{ref2}}$ were used to determine the hysteresis widths ΔV_{H1} (solid) and ΔV_{H2} (dashed).

The sweep rate is a critical parameter for determining the hysteresis width, as shown in Fig. 5.20. The observation of hysteresis is dependent on the trap parameters and associated capture and emission times; in certain instances, hysteresis may not be detectable. As illustrated, the traps operated too quickly, allowing sufficient time for discharge at a longer sweep rate.

5.9.4. Post-Processing Steps for $I_{\mathrm{d}} - V_{\mathrm{gs}}$ and $C - V$ Fit

To accurately fit the measured and simulated "up-and-down" $C-V$ characteristics and minimize simulation time, the applied signal was split into two components, as shown in Fig. 5.21. Both the small signal and gate voltage for the up- and down-sweeps

were applied simultaneously. For analytical simplification, we propose that a fast interface state can be accurately represented using an SRH model. This methodology produces results similar to those of the NMP model within the specified measurement range but with a reduced capture/emission barrier or by varying S and E_t parameters [255]. A comprehensive NMP model was utilized for slow-border traps.

The effective gate voltage shifts for the up- and down-sweeps were calculated using Eq. 5.68 by considering the complex trap system at the 4H-SiC/SiO_2 interface.

$$\begin{aligned} V_{\text{eff}}(f, \text{SR}, T) = V_{\text{ideal}}(T) + \Delta V_{\text{it}}(f, T) + \Delta V_{\text{ox}}^{1}(\text{SR}, T) + \\ + \Delta V_{\text{ox}}^{2}(\text{SR}, T) + \Delta V_{\text{fix}}(T) \end{aligned} \tag{5.68}$$

Where V_{ideal} is the ideal $I_d - V_{gs}$ or $C-V$ curve without any defects; ΔV_{it} is the shift caused by the interface traps; ΔV_{ox}^{1} is the shift caused by slow traps located close to the conduction or valence band and depends on the sweep rate (SR) and temperature; ΔV_{ox}^{2} is the shift caused by slow traps located close to the mid-gap; and V_{fix} is the fixed oxide positive charges.

The changes in V_{th} from all models are summarized, and the overall curve shift is compared with the measured shift, as shown in Fig. 5.22. As previously illustrated in Fig. 4.21, a minimum of three types of border traps and one type of interface trap contribute to the hysteresis width and the BTI shift.

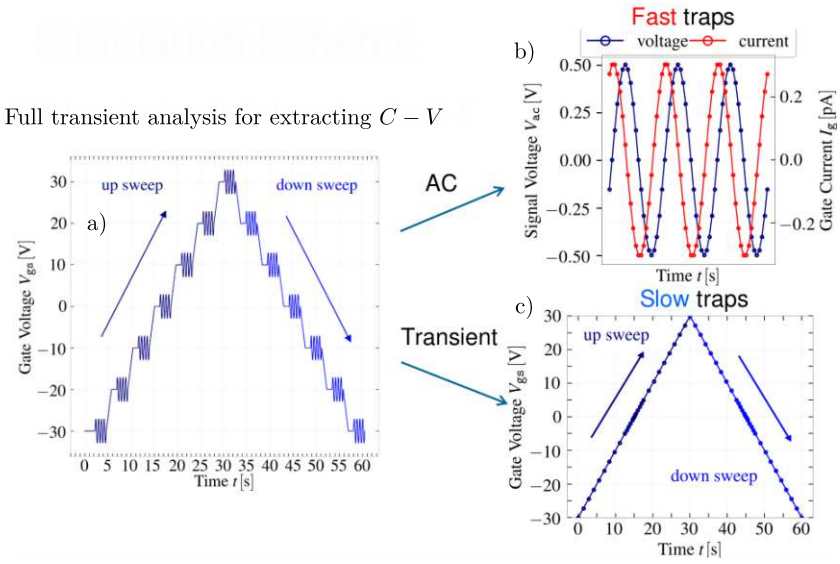


Figure 5.21.: The V_{GS} waveform is applied to the gate to simulate the "up-and-down" $C-V$ characteristics. Due to the presence of fast traps in 4H-SiC/SiO_2, which contribute to the stretch-out effect at high frequencies, and slow traps that are responsible for the hysteresis width BTI, the applied signal can be divided into two components. b) AC analysis for fast traps utilizing the SRH model for accurate electrostatic considerations. c) Transient analysis by performing an up and down gate voltage sweep to simulate hysteresis using the NMP model, which is primarily utilized for simulating $I_d - V_{gs}$ curves.

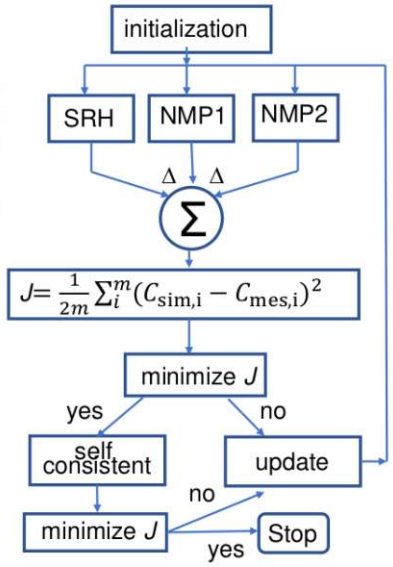


Figure 5.22.: Overview of the device optimization process utilizing post-processing steps. The total V_{th} values were calculated and compared with the measured data. The cost function is minimized; otherwise, the process is repeated using the updated trap parameters.

5.10. Summary

To summarize, in this chapter, a two-state NMP framework was derived to calculate the charge-trapping kinetics of slow-border traps for lateral and trench 4H-SiC MOSFETs. In addition, SRH theory was used to simulate fast interface traps and their contribution to calibrating the channel mobility model owing to the Coulomb scattering effect. The influence of the NMP model parameters on the hysteresis width was simulated. The defect have been assumed to have amphoteric behavior. Thus, post-processing optimization was used to fit the parameters of the three different traps to predict the measured hysteresis width. To accurately characterize the device electrostatics and analyze the subthreshold swing, stretch-out effect, threshold voltage drift, and hysteresis width at the $I_{\text{d}} - V_{\text{gs}}$ and $C - V$ curves across different temperatures, we utilized the TCAD tool with a complicated transient analysis and specified models: mobility degradation, SRH for fast interface traps, NMP for slow border traps, and fixed positive traps in the oxide. The parameters were optimized for both lateral and trench devices.

6. Results of Investigating Defects in 4H-SiC MOSFETs

This chapter explores the influence of temperature on the hysteresis observed in the transfer characteristics and $C-V$ curves of 4H-SiC lateral and trench MOSFETs. The hysteresis width was experimentally characterized as the difference in the threshold voltage between the sweeps up and down within a temperature range of 100 to 600 K. The temperature-dependent hysteresis behavior was categorized into three primary regions. A reduction in the hysteresis was observed within the cryogenic temperature range of 125–100 K. This phenomenon appears to be associated with the impact of freeze-out carriers. [256]. The typical hysteresis decreases from 150 to 300 K because of the slow border traps located near the 4H-SiC conduction band. Finally, an increase in anomalous hysteresis was observed at elevated temperatures ranging from 350 to 600 K. The addition of slow-border traps is responsible for this phenomenon. As the gate voltage increased, the threshold voltage moved towards positive gate voltages, and this movement decreased as the temperature increased. This shift still exists throughout the subsequent down sweep, as traps retain their charge states. The traps are located close to the SiC/SiO_2 interface and may exhibit characteristics similar to either donor- or acceptor-like fast interface traps, slow border traps, or fixed positive charges. Furthermore, the examination of the hysteresis behavior across multiple cycles indicated that the hysteresis observed in both the $I_d - V_{gs}$ and $C-V$ measurements for the trench device can be associated with the same trap system. Although $C-V$ measurements provide a more precise evaluation of the density of states, they are more complex to simulate and differentiate between each trap type. The differences in the hysteresis width observed in the lateral and trench 4H-SiC MOSFETs can be attributed to the involvement of distinct traps. A two-state non-radiative multi-phonon model was employed to compute the capture and emission times for the evaluation of trap occupancy. It has been demonstrated that the hysteresis width is associated with the charge accumulated in these traps [99].

6.1. Hysteresis and BTI of Lateral MOSFETs

The SiC/SiO_2 interface exhibits a significant defect density with an electrically active border and interface traps, resulting in a severely perturbed device channel mobility during regular device operation compared to Si-based devices [3], [215], [257]. Furthermore, the accumulation of charge within these traps leads to the degradation of the electrostatic properties of the device. Due to the coupling of the defects to the surrounding phonon system, the charge transfer kinetics are strongly temperature-

dependent. This effect is believed to be responsible for the temperature dependence of threshold voltage shift (ΔV_{th}) (Fig. 6.1, top) and the hysteresis width ΔV_{H}. This width is determined as the threshold voltage difference between the up and down sweep of V_{gs} at a chosen reference current $I_{\mathrm{d}}^{\mathrm{ref}}$ (Fig. 6.1, bottom). Previous experiments showed that hysteresis is a recoverable phenomenon that does not increase with operating time [91], [258]. However, during the operation of the circuit, the device can turn-off at a higher V_{gs} than turn-on, due to the hysteresis effect [112]. This margin between the on- and off-switching bias needs to be considered within the gate control at the circuit level at all times [258].

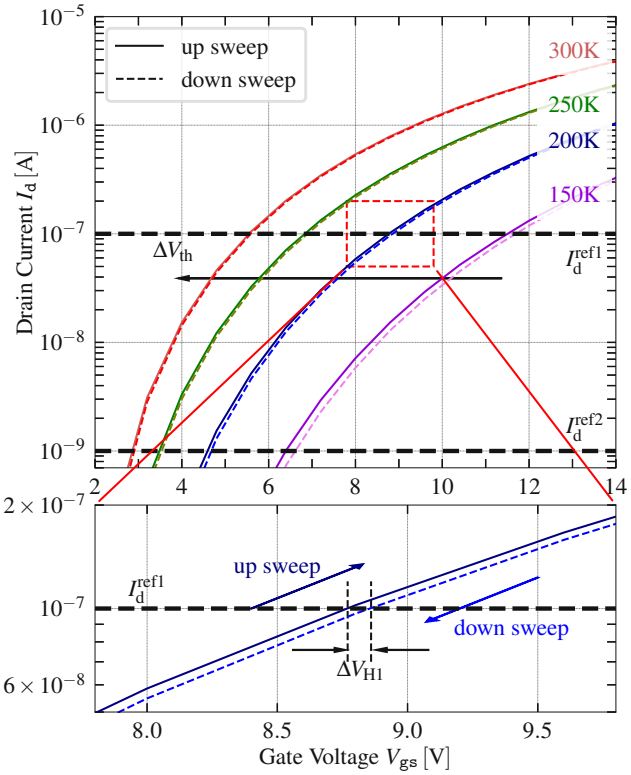


Figure 6.1.: Measured $I_{\mathrm{d}}-V_{\mathrm{gs}}$ curves at T=150, 200, 250, and 300 K using up/down V_{gs} sweeps. Two reference drain currents $I_{\mathrm{d}}^{\mathrm{ref1,2}}$ were used to determine the hysteresis widths ΔV_{H1} and ΔV_{H2} (for visual clarity, only ΔV_{H1} for T=200 K is presented, bottom) as the difference in the corresponding voltages during the up and down V_{gs} sweeps. From: [99].

Lateral 4H-SiC nMOSFETs (see Fig. 1.2a) with the hysteresis measurement method were used to measure the transfer characteristics, see Fig. 3.2, left. Fig. 6.1 demonstrates that the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ characteristics exhibit a shift of approximately 5.5 V towards elevated V_{gs} values at reduced temperatures. This behavior is attributed to a change in the charge state of the interface and border traps situated within a few nanometers of the SiC/SiO_2 interface [105], [169], [170], [259]. As the gate-source voltage (V_{gs}) increases, defects may alter their charge state, resulting in ΔV_{th}, which is typically

identified as BTI. Additionally, a positive ΔV_{th} shift is noted during the down sweep in comparison to the up sweep in the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves, with this effect being more pronounced at lower temperatures [99].

To accurately analyze the device electrostatics and the subthreshold swing and threshold voltage drift across different temperatures the Sentaurus TCAD tool along with specified models was used [233]: mobility degradation [145], [211], [241], SRH for fast interface traps [239], [240], NMP for slow border traps [18], [21], [260]. The mobility models include the phonon scattering μ_{Ph} and Coulomb scattering μ_{C} components [145], [211], [241]. Coulomb scattering predominates because of the significant presence of charge centers at the interface. The concentration of these charge centers is temperature-dependent and adversely affects the channel mobility. In long channel MOSFETs characterized by moderate to low channel doping levels, the mobility of the inversion layer is constrained by phonon scattering [241]. The effective mobility can be expressed as $1/\mu_{\mathrm{eff}} = 1/\mu_{\mathrm{Ph}} + 1/\mu_{\mathrm{C}}$: In this equation, the Coulomb component is represented by $\mu_{\mathrm{C}} \propto \mu_0 (T/300)^{\alpha}/N_{\mathrm{it}}$. We utilize $\mu_0 = 10\,\mathrm{cm^2V^{-1}s^{-1}}$, $\alpha = 2.8$, and $N_{\mathrm{it}}(T)$ represents the temperature-dependent interface trap density measured in cm^{-2} [99].

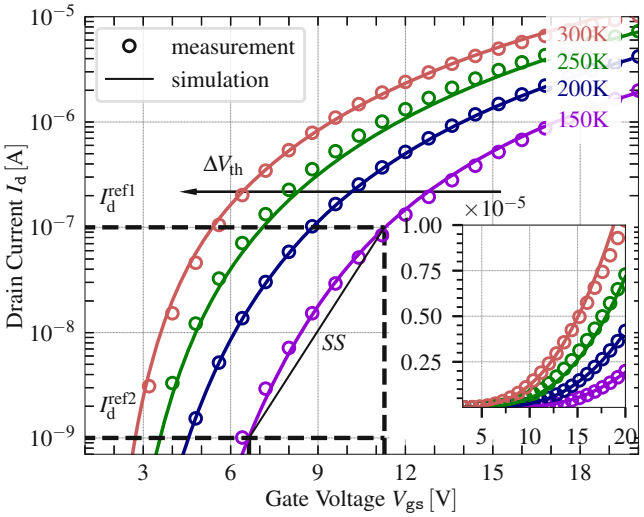


Figure 6.2.: Simulated vs. measured $I_{\mathrm{d}} - V_{\mathrm{gs}}$ up sweep curves at T=150, 200, 250 and 300 K. Two reference drain currents $I_{\mathrm{d}}^{\mathrm{ref1,2}}$ were used to determine two threshold voltages and subthreshold swings. From: [99].

To better replicate the measured $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves in the TCAD simulation presented in Fig. 6.1, acceptor-like interface traps were added to the SRH model, as previously identified in the SiC/SiO_2 system [31], [49], [145], [239], [255], [261], [262]. In contrast to border traps, interface traps exhibit a more limited range of time constants and primarily influence the subthreshold swing of transfer characteristics.

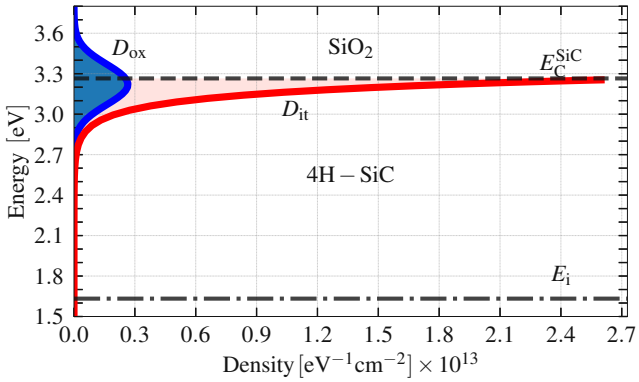


Figure 6.3.: The densities of the interface traps D_{it} (red, exponential distribution) and border acceptor-like traps D_{ox} (blue, Gaussian distribution) were used in the simulation. From: [99].

The traps exhibited a rapid response and attained their thermodynamic equilibrium state within the measurement duration, thus not contributing to the hysteresis observed during the gate voltage sweep [263]. Consequently, electrically active interface traps were considered to enable the mobility degradation model. The SRH model parameters are listed in Table 6.1. The application of these parameters enables precise reproduction of the measured gate-voltage up-sweep, as demonstrated in Fig. 6.2. The defect density of acceptor-like traps D_{it} exhibited an exponential increase as it approached the SiC conduction band edge, as illustrated in Fig. 6.3 (red) [239]. Nonetheless, the elevated concentration of acceptor-like traps leads to a significant positive threshold voltage shift, which is considerably greater than observed experimentally. Therefore, fixed positive charged traps N_{it}^{fix} were added to the TCAD simulation setup to reproduce the significant shift in V_{th} [99], [261].

Parameter	**Value**
Interface trap concentration D_{it}, $eV^{-1}cm^{-2}$	2.6×10^{13}
Acceptor-like defect density D_{ox}, cm^{-2}	2.4×10^{12}
Positive interface trap concentration N_{it}^{fix}, cm^{-2}	7.0×10^{11}
Exponential energy distribution σ_E, eV	0.1
Capture cross section for electrons σ_e^0, cm^{-2}	10^{-10}
Capture cross section for holes σ_h^0, cm^{-2}	10^{-12}

Table 6.1.: Parameters for Interface Traps. From: [99]

It is assumed that both the interface and border traps contribute to the threshold voltage shift. The concentration of these traps was determined by replicating the experimental data in our simulations, taking into account the ΔV_{th} shift and the hysteresis width $\Delta V_{H1,2}$ at $T = 200\,K$, as illustrated in Fig. 6.4. The acceptor-like traps exhibiting a 0/-1 charge transition level near the conduction band edge, denoted by $E_t^A \sim E_C$, were assumed to follow a normal distribution with a standard deviation

of $\sigma_{E_t^A}$.The mean energy level of the distribution is set to level is set at 0.15 eV, accompanied by a defect density of approximately $D_{ox} \sim 2.4 \times 10^{12}\,\mathrm{cm}^{-2}$, as illustrated in Figure Fig. 6.3 (blue) [169].

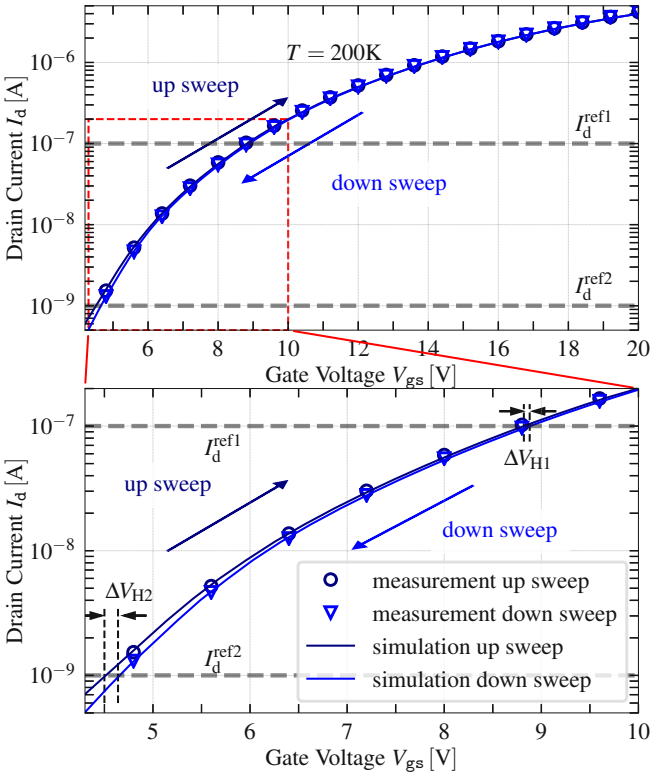


Figure 6.4.: Simulated vs. measured $I_d - V_{gs}$ curve at $T = 200\,\mathrm{K}$. The V_{th} shift and $\Delta V_{H1,2}$ widths were obtained using the non-radiative multiphonon model with the effect of charging acceptor-like traps. From: [99].

During V_{gs} sweeps, acceptor-like traps participate in the charging and discharging kinetics, characterized by their respective capture and emission times. As V_{gs} increases, the average capture time of all traps significantly decreases compared to the emission time, resulting in the traps becoming charged [18]. The energy barriers between the charge states of the acceptor-like trap were characterized within the NMP model using a relaxation energy of $S = 0.1 \pm 0.01\,\mathrm{eV}$ and a parabolic curvature ratio of $R = 1.0 \pm 0.01$. An asymmetry in the capture and emission times is introduced because of the differing forward and backward barriers [18], [21]. The distribution of the NMP parameters is a consequence of the amorphous nature of the gate insulator (SiO_2) and thus the structural variations of the defect sites. In this scenario, only defects that influence the hysteresis at the specified gate bias and temperature are considered owing to the rapid sweeping rates. Consequently, a reduced relaxation energy with a narrower distribution was utilized in the simulation in comparison with that extracted from long-term BTI experiments [169], [252]. The trap energy distribution is sufficiently broad

to generate a range of barrier heights necessary for calculating the charge transitions. Several traps from the broad ensemble included in our simulation exhibited excessively delayed responses (i.e., extended emission times) and could not return to their original charge state during the downward sweep of the gate voltage. These charged traps were responsible for the observed hysteresis width. At elevated temperatures, both the previously stated processes are significantly accelerated, resulting in a more rapid discharge of traps, which leads to a decrease in both ΔV_{th} and $\Delta V_{\mathrm{H1,2}}$ [99].

Fig. 6.4 shows the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curve simulated for T=150, 200, 250 and 300 K, where one can see that our modeling framework accurately captures the transfer characteristics. In particular, the trends for the temperature dependence of V_{th}, see Fig. 6.5, and subthreshold swing SS, see Fig. 6.6, are well represented by the simulation. As the

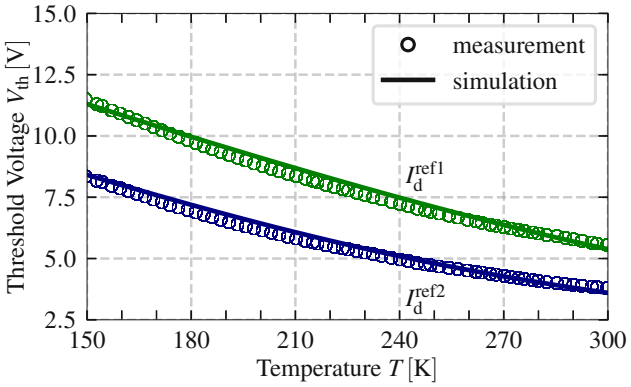


Figure 6.5.: Comparison of simulated and measured threshold voltages across different temperatures, along with two references for the drain current. At higher T the threshold voltage shift decreases because traps can capture a charge; however, at the same time, most of these are emitted faster. At lower T traps emit a charge slower and the threshold voltage shift increases. From: [99].

gate voltage increases, the acceptor-like interface traps become charged, intensifying Coulomb scattering in the inversion layer and resulting in a positive threshold voltage shift. As the temperature increases, the transition rates, particularly the emission rates, increase, but the quantity of charged traps decreases. Hence, a reduced change in V_{th} was observed, as illustrated in Fig. 6.5, which is analogous to the subthreshold swing depicted in Fig. 6.6. As the charge stored in defects at the interface decreases, Coulomb scattering becomes less significant with increasing temperature, thereby improving the mobility of the inversion layer [211], [264]. The simulation setup accurately reproduced the hysteresis observed during upward and downward sweeps. Fig. 6.4 illustrates the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curve simulated at $T = 200$ K. Fig. 6.7 illustrates the hysteresis $\Delta V_{\mathrm{H1,2}}$ as a function of temperature T. At low temperatures, $\Delta V_{\mathrm{H1,2}}$ is substantial, whereas it decreases at higher temperatures. To clarify the hysteresis behavior, we computed the average capture and emission times of a substantial ensemble of defects along with their trap occupancy, as illustrated in Fig. 6.8 [99]. Our simulation indicates that during the up sweep, when $V_{\mathrm{gs}} < V_{\mathrm{th}}$, the emission time τ_{e} is less than the capture time τ_{c}, $\tau_{\mathrm{e}} \ll \tau_{\mathrm{c}}$ (Fig. 6.8a). Consequently, electrons were emitted into the

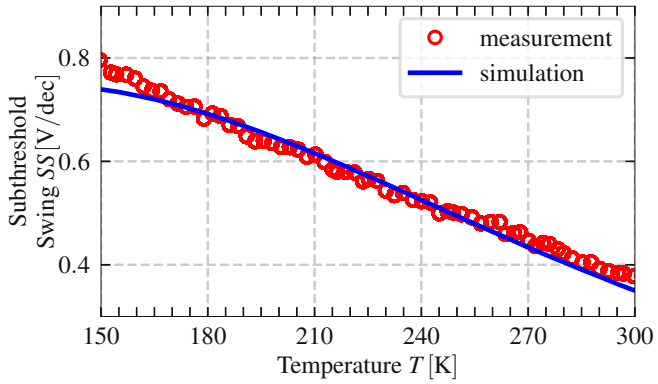


Figure 6.6.: Simulated versus measured subthreshold swing at various temperatures. SS = $\partial V_{\mathrm{gs}}/\partial I_{\mathrm{d}}$, From: [99].

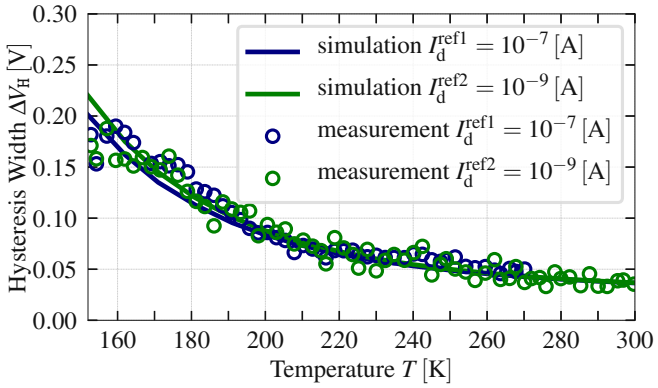


Figure 6.7.: Measured and simulated widths of the hysteresis $\Delta V_{\mathrm{H1,2}}$ in the temperature range from 150 K to 300 K using two different reference drain current levels ($I_{\mathrm{d}}^{\mathrm{ref1}}$, $I_{\mathrm{d}}^{\mathrm{ref2}}$). From: [99].

channel, resulting in predominantly zero-defect occupancy (Fig. 6.8b). This is illustrated in Fig. 5.14a. When $V_{\mathrm{gs}} \geq V_{\mathrm{th}}$, the defect trap levels may energetically align with the Fermi level in the SiC channel, resulting in capture times equal to emission times. This intersection point (IP) is shown in Fig. 6.8a. At the IP, the trap occupancy starts at 50% in the steady state; however, in transient simulations, the trap occupancy depends on the sweep rate and may differ from the steady state IP occupancy, as shown in Fig. 6.8b (horizontal dashed line). Therefore, V_{th} shifts towards positive gate voltages, as shown in Fig. 5.14b.

As illustrated in Fig. 6.8a, both the capture and emission times decrease with increasing T, and their temperature-dependent IP shifts towards elevated V_{gs}. Thus, the trap occupancies, even at raised V_{gs}, decrease significantly at increased T (see Fig. 6.8b). To achieve equivalent occupancy (horizontal dashed line in Fig. 6.8b) at $T = 150\,\mathrm{K}$, a reduced V_{gs} is required. This resulted in a more severe V_{th} shift compared to that observed at $T = 300\,\mathrm{K}$. During the down sweep, electrons are likely to be re-emitted into the channel at elevated temperatures. As a result, the majority of

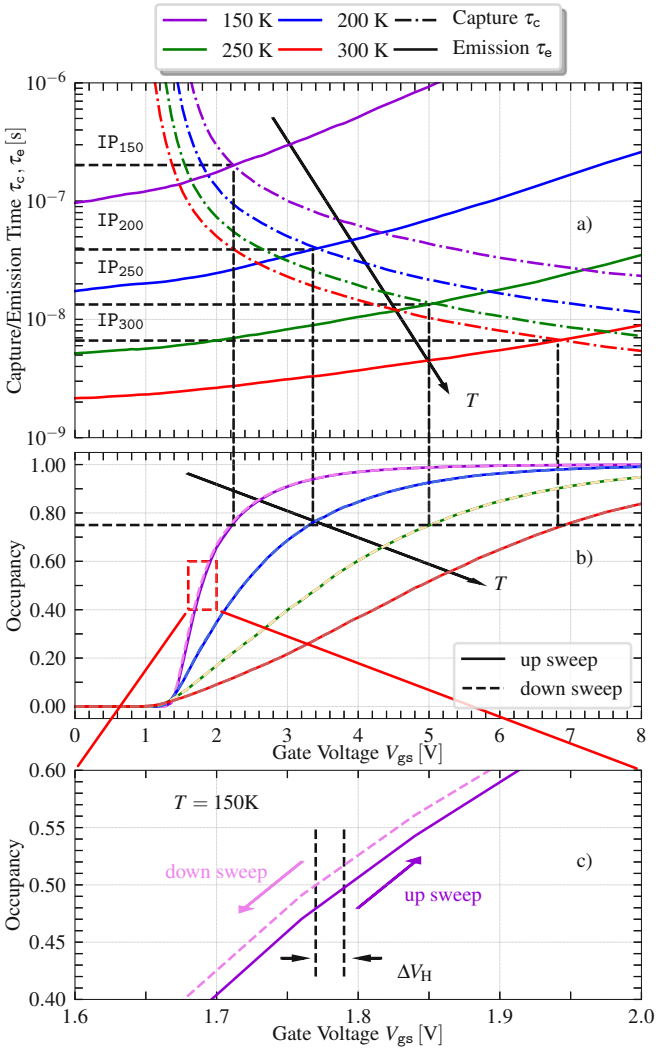


Figure 6.8.: a) Modeling charge capture/emission times as a function of V_{gs} (the median data of all trap ensembles), b) trap occupancy at T=150, 200, 250, and 300 K, c) trap occupancy at T=150 K for up/down V_{gs} sweeps. From: [99].

the traps are neutralized, resulting in minimal $\Delta V_{H1,2}$, as illustrated in Fig. 5.14e. Additionally, we must consider the sweep down time t_{down} (in our example $t_{down} \sim 6$ s), which may affect the hysteresis width. If $\tau_e \gg \tau_c$ and $\tau_e < t_{down}$, a defect eventually captures an electron and quickly releases the captured charge during the down sweep. However, if the relationship is inverted such that $\tau_e > t_{down}$, the defects retain their charge state, as shown in Fig. 5.14f, e. The intersection point indicates the distance between t_{down} and τ_e. Fig. 6.8a illustrates that IP_{150} significantly exceeds IP_{300}. When the temperature decreased, not all traps became neutralized, as illustrated in Fig. 5.14f. These traps remained occupied and retained their contribution to the V_{th} shift (Fig. 6.8c), leading to significant hysteresis, as illustrated in Fig. 6.7 [99].

6.2. Hysteresis of Lateral MOSFETs over an Extended Temperature Range

The hysteresis width over the temperature range of 150 to 300 K was successfully simulated and explained in the previous chapter. Two types of border traps and one type of interface trap distribution were used in the simulation for this purpose Table 6.1. According to Fig. 4.21, the extended measurement data has been used to investigate the hysteresis behavior. In region A, within the temperature range of 100–140 K, the hysteresis width increased. This phenomenon is attributed to the increase in the freeze-out effect, which occurs when the capture and emission rates are insufficiently low, resulting in traps maintaining their states and absence of hysteresis. As the temperature increased, traps began to capture electrons; however, at 150 K, the emission rate was too low to reduce the hysteresis effect for experimentally accessible sweep rates, resulting in the observation of the hysteresis width peak.

To account for the relevant charge trapping kinetics, an acceptor-like NMP defect distribution was introduced in the simulation and termed defect (1), with parameters detailed in Table 6.2. In region B, within the temperature range of 150–400 K, a decrease in the hysteresis width is observed, as detailed in 6.1 for defect (3).

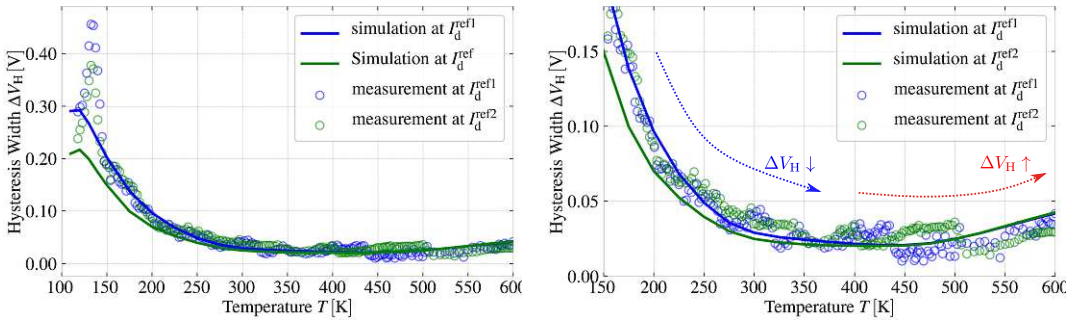


Figure 6.9.: Measured and simulated hysteresis widths of the lateral 4H-SiC MOSFET in the temperature range of (100–600) K. Three different types of border traps were used in the simulations.

The hysteresis width remained mostly constant across the entire temperature range, as illustrated in Fig. 6.9, as indicated by the blue arrow on the left. This may represent a neutral trap that is uniformly distributed throughout the bandgap. In conclusion, anomalous hysteresis increases in the region labeled C, as indicated by the left red arrow in Fig. 6.9. The implementation of an additional border trap (2) explains this behavior. The acceptor-like border traps (1) and (3) exhibit the same energy level but differ in their S values, which can be explained by different phonon coupling regimes resulting from the different structural configuration modes of an amphoteric defect species characterized by distinct temperature behaviors. The post-processing method

and optimization scheme, incorporating new additional trap types, yielded favorable results in explaining the hysteresis width across a broader temperature range than in section 6.1.

Table 6.2: The NMP parameters were used to simulate the $I_d - V_{gs}$ curves of planar 4H-SiC MOSFETs over a wide temperature range.

Symbol	D_{ox1}	D_{ox2}	D_{ox3}	D_{it}	Unit
Trap type	acceptor-like $0/-1$	donor-like $1/0$	acceptor-like $0/-1$	acceptor-like $0/-1$	
N_t	1.1×10^{12}	1.0×10^{11}	5.0×10^{11}	2.6×10^{13}	cm^{-2}
E_t	E_C	$E_g/2$	E_C	E_C	eV
S	0.5 ± 0.2	1.0 ± 0.2	5.0 ± 0.2	–	eV

6.3. Hysteresis in $I_d - V_{gs}$ of Trench MOSFETs over Multiple Cycles

Despite long-term optimized fabrication processes, reliability issues regarding the SiC/SiO_2 interface and oxide remain a major research topic, owing to the high defect density compared to the SiO_2/Si interfaces. At the same time, commonly used lateral MOSFETs have lower mobility because of the high trap concentration located close to the conduction band. The new trend for the next generation of 4H-SiC power MOSFETs is related to trench technologies because of the enhanced channel carrier mobilities at the a-faced SiC/SiO_2 interface, and thus smaller R_{ON}. A difference due to the different interface states between the Si- and a-face SiC/oxide interfaces can also be observed when comparing the hysteresis behaviors of planar and trench MOSFETs. A difference due to the different interface states between Si- and a-face SiC/oxide interfaces can also be observed when comparing the hysteresis behavior of planar and trench architecture MOSFETs. This is likely a result of the different densities of the trap states and their energy levels, which affect charge trap kinetics. To understand the differences between hysteresis, a physical-based modeling approach based on Shockley–Read–Hall (SRH) theory for interface defects and non-radiative multiphonon (NMP) theory for defects in the oxide is developed. To verify the proposed modeling approach and defect parameters used in the simulation, a commercial discrete asymmetric trench 4H-SiC nMOSFET (see Fig. 1.2) was analyzed for hysteresis. Therefore, a measurement method with 21 cycles was used (see Fig. 3.2, right).

Fig. 6.10 shows the comparison between measured (symbols) and simulated (lines) $I_d - V_{gs}$ curves at a temperature of 300 K and different pulses. To obtain this result, the capture and emission times for investigating the effect of the slow border traps on the charging dynamics were calculated. If the emission time at a higher gate bias is slower than the down-sweep and capture times, the charges are stored in the trap, and a hysteresis effect is observed. In addition, the negatively charged interface traps that

led to strong positive voltage shifts were compensated by positive bulk oxide defects to reduce this effect.

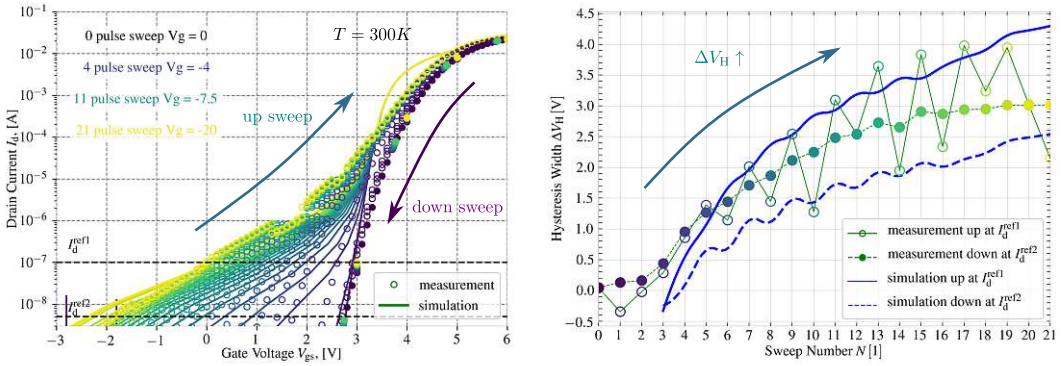


Figure 6.10.: Simulated vs. measured $I_d - V_{gs}$ curve for trench 4H-SiC MOSFET at T =300 K at different starting gate voltage. The V_{th} shift and $\Delta V_{H1,2}$ width were obtained by the non-radiative multiphonon model with the effect of charging traps.

The channel carrier mobility strongly depends on the selected crystal plane. Compared to planar MOSFETs, fast donor-like interface defects are energetically located close to the valence band and have an exponential distribution. The small trap concentrations, which are located close to the conduction band, lead to a higher channel carrier mobility in the trench owing to the reduced Coulomb scattering effect compared with lateral transistors. In addition, slow donor-like border traps were energetically located in the mid-gap and exhibited a Gaussian distribution.

Table 6.3: The NMP parameters of D_{ox2} for simulating the $I_d - V_{gs}$ curves of the trench 4H-SiC MOSFET.

Trap type	N_t	E_t	S	σ_S
donor-like 1/0	1.1×10^{12} $cm^{-2}eV^{-1}$	E_V+ 0.6 eV	2.5 eV	0.2 eV

At zero gate voltage, all the donor-like border traps were initially neutral. During the downward sweep at negative gate voltages, the traps captured holes and became increasingly positively charged, resulting in a negative V_{th} shift. Next, during the up-sweep at positive gate voltages, the positively charged donor-like traps capture electrons and become neutralized. With each cycle, the negative gate voltages increase, resulting in incomplete neutralization of traps by the applied positive gate voltage, thereby increasing the hysteresis during negative voltages in each subsequent cycle.

6.4. Hysteresis in $C-V$ of Lateral MOSFETs Across Varying Frequencies and Temperatures

To extend the energetic range at which charge trapping kinetics can be observed, $C-V$ curves are an attractive alternative to I_d-V_{gs} measurements, and the Fermi level scans over the band gap of the substrate during the bias sweep and defect response can be observed in all MOSFET operation regimes, from accumulation to inversion. Therefore, the modeling approach was extended by adding defects to explain the $C-V$ response. To represent the $C-V$ curves at different frequencies (Fig. 4.16a and c, we used an exponential distribution of fast acceptor-like interface defects located near the conduction band (Fig. 6.11) [100], [104], [165], [166], [167], [168]. The charge capture (τ_c) and emission (τ_e) times across a wide bias range enable charge trapping and detrapping to respond effectively to small-signal modulation. The interface traps that capture electrons become electrically active and are directly incorporated into the mobility degradation model as utilized for $I_d - V_{gs}$. In our study, we utilized the measured and simulated curves to determine parameters such as $\mu_0 = 18\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, $\alpha = 9.2$, and the temperature-dependent interface charge density $D_{it}(T)$ [232]. Variations in the values of $I_d - V_{gs}$ arise from the use of different lateral devices. The capture cross-section for electrons and holes are given by $\sigma = 10^{-15}\,\mathrm{cm^{-2}}$ [232].

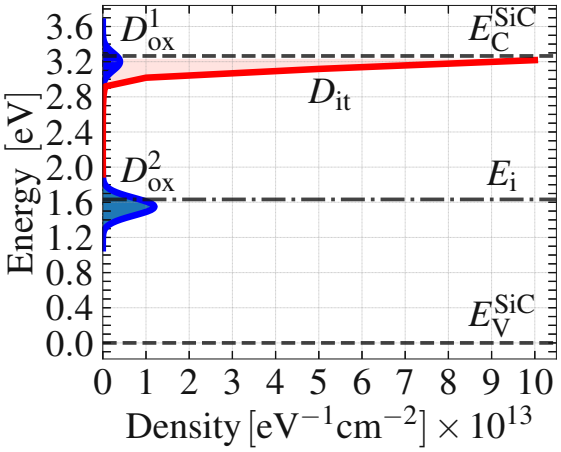


Figure 6.11.: The DOS for the D_{it} (red), D^1_{ox} and D^2_{ox} (blue). From: [100]

The data indicate that donor-like traps that are exponentially distributed from the valence band have minimal impact; therefore, they were excluded from the simulation, as illustrated in Fig. 4.16. In addition, a Gaussian distribution of slower acceptor-like border traps D^2_{ox} near the SiO_2/SiC interface is included. This defect band was found to be located approximately at the center of the 4H-SiC band gap. The capture and emission times of the relevant border traps were computed using the NMP model [18].

The asymmetrical nature of the energetic barriers between the two charge states, as obtained from the potential energy surface (PES) within the NMP model, for both forward and backward processes, results in the dispersion of the charge capture and emission times. The barriers were computed from the relaxation energy $S = 4.0 \pm 0.1$ eV and the parabolic curvature ratio $R = 2.0 \pm 0.1$. The asymmetry of the capture and emission times, which is dependent on the bias, affects the width of the hysteresis as it transitions from the depletion region to the accumulation region. Additionally, another Gaussian distribution of slow acceptor-like border traps, D^1_{ox}, characterized by a reduced concentration and positioned energetically near the conduction band of 4H-SiC, was used. The relaxation energy of D^1_{ox} was calibrated to $S = 0.1 \pm 0.01$ eV, whereas the parabolic curvature ratio was determined to be $R = 1.0 \pm 0.01$ to reproduce the measured data.

Parameter	**Value**
Interface trap concentration D_{it}, $\text{eV}^{-1}\text{cm}^{-2}$	9.6×10^{13}
Exponential energy distribution σ^{it}_E, eV	0.1
Acceptor-like defect density D^1_{ox}, cm^{-2}	0.5×10^{12}
Acceptor-like defect density D^2_{ox}, cm^{-2}	2.0×10^{12}
Positive interface trap concentration $N^{\text{fix}}_{\text{it}}$, cm^{-2}	7.0×10^{11}
Exponential energy distribution $\sigma^{1,2}_{E_{\text{ox}}}$, eV	0.1

Table 6.4.: Parameters for Traps. From: [100].

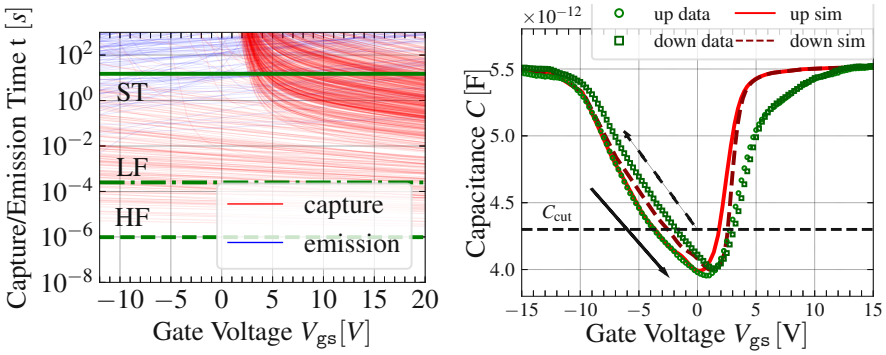


Figure 6.12.: Left: Simulated capture (red) and emission (blue) times of D^2_{ox}. The HF and LF lines refer to high and low frequencies, respectively, and ST is the sweep time. Right: Comparison of the hysteresis width with the measured (green) and simulated C-V (red) at 4 kHz and 300 K. From: [100].

The charge carrier occupation of these defects influences the hysteresis width, transitioning from the depletion to the inversion region [265]. The significant charge stored in the acceptor-like traps leads to a pronounced positive voltage shift, pushing V_{gs} to higher values. Fixed positive traps $N^{\text{fix}}_{\text{it}}$ are required to account for the significant ΔV shift. The defect parameters used in the simulations are listed in Table 6.4 [100].

Figure 6.12, right, illustrates the comparison of the hysteresis width between the measured and simulated capacitance-voltage characteristics at 4 kHz and 300 K. By

sweeping the gate voltage from deep inversion to deep accumulation, we scanned the 4H-SiC band gap and observed the response of the traps to the shifted Fermi level.

A schematic representation of the band diagram and configuration coordinate diagram in various regimes was employed to enhance the understanding of trap kinetics during $C-V$ measurements across varying upward and downward gate voltage sweeps.

When the gate voltage sweeps up in the accumulation region, there are a lot of holes in the channel. However, they cannot be captured by slow acceptor-like traps D^2_{ox} because the barrier E^V_{21} is high. However, the barrier E^V_{12} is low and the traps are empty (see Fig. 6.13A). In the depletion region, electrons start to be captured by the traps but tend to be recombined with minor holes. Traps are charging. In the inversion region, the traps are fully charged because the capture time is shorter than the emission time. During the down-gate voltage in a weak inversion region, traps mostly maintain their charge states and no hysteresis occurs (see Fig. 6.13B and C). This indicates that certain defects maintained their charge states throughout the bias sweep, as illustrated in Fig. 6.12, respectively. These slow defects appear to account for the hysteresis width, $\Delta V_{\text{H}}^{\text{d-a}}$. Nonetheless, an increase in temperature results in a reduction in the hysteresis width, and the value of ΔV_{H} from depletion to accumulation (d-a) is ten times greater than that from depletion to inversion (d-i). Nonetheless, if the emission time continues to exceed the sweep time (ST), we do not observe a significant temperature dependence of $\Delta V_{\text{H}}^{\text{d-i}}$. During the down-gate voltage in a weak accumulation, traps tend to be neutral and shift the curve towards a more positive gate voltage. We can observe hysteresis in the depletion to accumulation region (see Fig. 6.14D and E). At low temperatures, electrons are captured during the up voltage sweep because the emission time is longer than the capture time, specifically $\tau_{\text{e}} \geq \tau_{\text{c}}$.

Therefore, the traps can became negatively charged. Consequently, ΔV is shifted towards positive gate voltages, as illustrated in Fig. 4.16a. As the gate voltage decreases, electrons are likely to be released back into the channel; however, because of the wide distribution of emission times, which extend over many orders of magnitude in time, certain traps retain their charge states. The elevated temperature decreased the capture and emission times, leading to neutralization of most of the traps. Consequently, both $\Delta V_{\text{H}}^{\text{d-a}}$ and $\Delta V_{\text{H}}^{\text{d-i}}$ exhibit small values, as shown in Fig. 4.16a. Fast interface traps exhibit a characteristic time constant τ_{c} ranging from 10^{-10} to 10^{-13} s, which is effective even at frequencies below $1/f_{\text{HF}}$ (high frequency, HF), as illustrated in Fig. 6.12, respectively. This allows them to respond to small signal frequency variations [100].

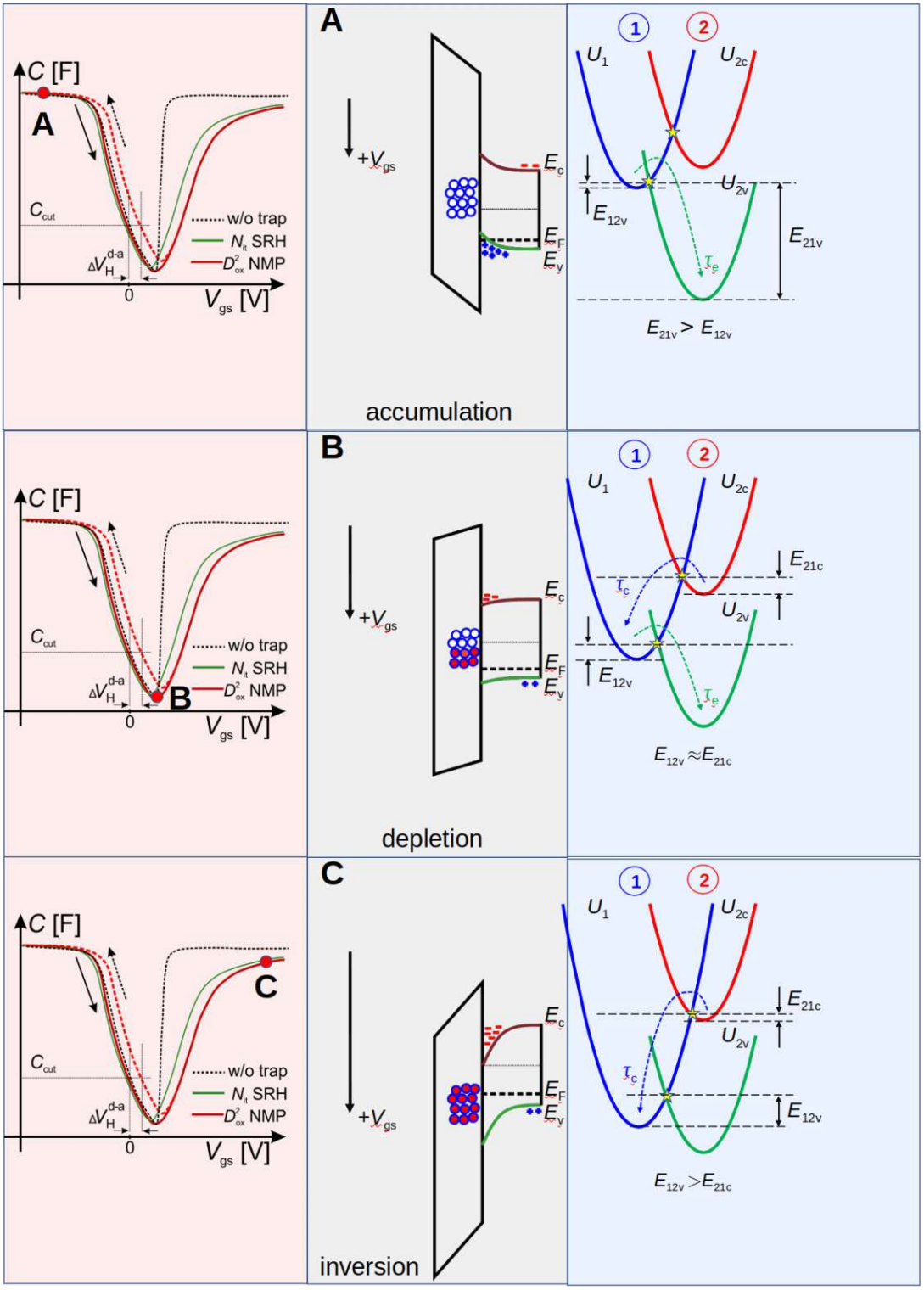


Figure 6.13.: The schematic view of $C-V$ curves and band diagram, and configuration coordinate diagram at the marked point on the $C-V$ curve for up gate voltage sweep.

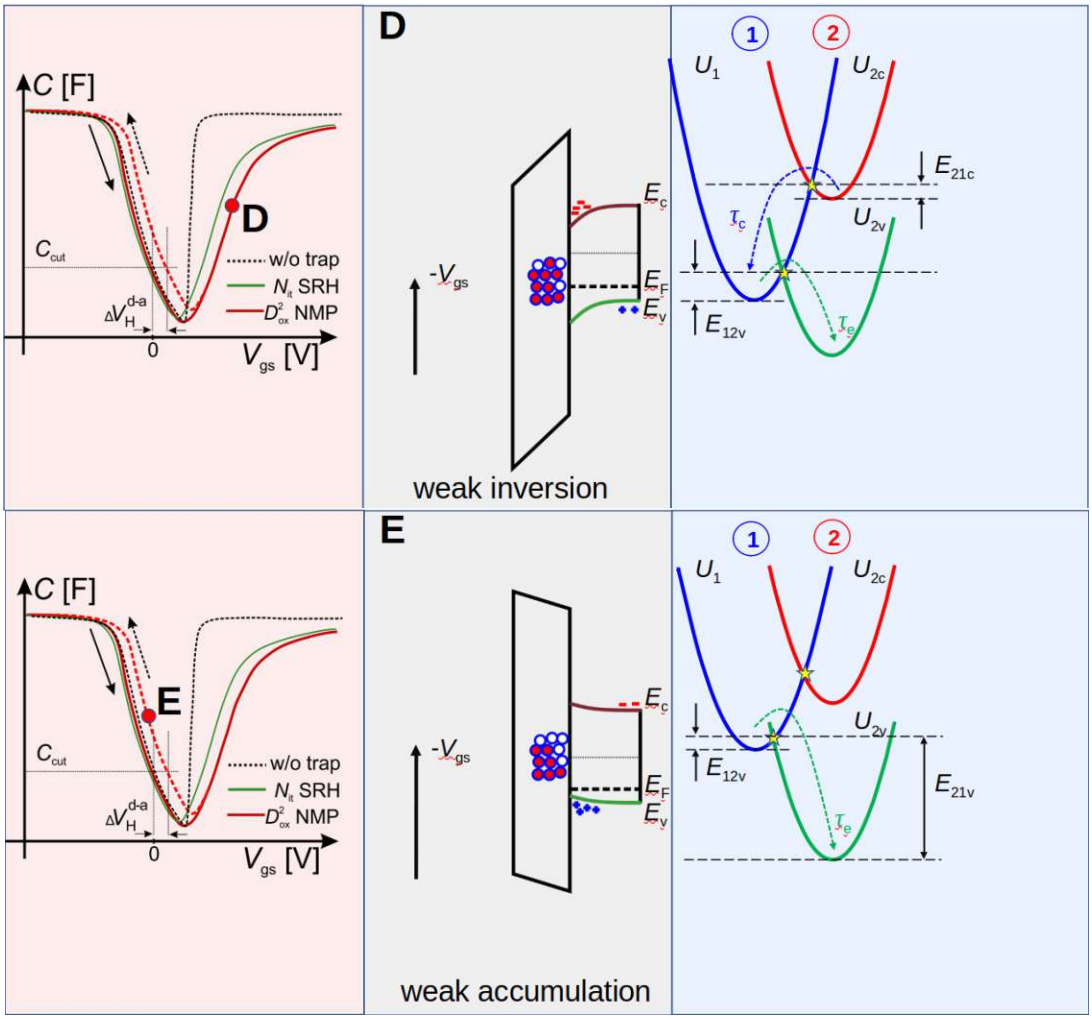
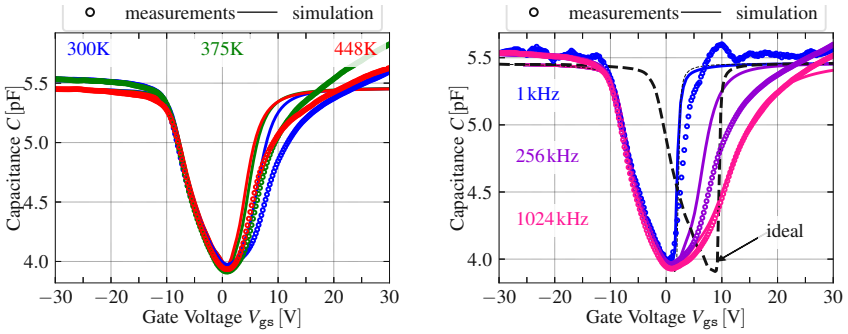


Figure 6.14.: The schematic view of $C-V$ curves and band diagram, and configuration coordinate diagram at the marked point on the $C-V$ curve for down gate voltage sweep.

Fig. 6.15 compares the measured and simulated results. The difference in the capacitance values in the strong inversion regime at high frequencies indicates residual parasitic impedance. The voltage shift ΔV strongly depends on the temperature and frequency, particularly when the gate bias is swept from the depletion to the inversion region (see Fig. 6.15). With increasing temperature, the capture and emission rates increase (or at the same time, τ_e becomes smaller than τ_c), which eventually leads to defect neutralization and thus a decrease in the threshold voltage shift. The frequency dependence of the $C-V$ curve distortion indicates the presence of interface traps. Fig. 6.15, right shows that the fixed positive defects deviate from the ideal and shift them towards lower gate voltages by 6 V at all frequencies (ΔV_{fix}). Simultaneously, the shape of the ideal $C-V$ curve was close to that measured at a low frequency



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and was not affected by the sweep rates and higher frequencies. Fast interface traps D_{it} can follow the small-signal frequency because the capture time is shorter than the emission time.

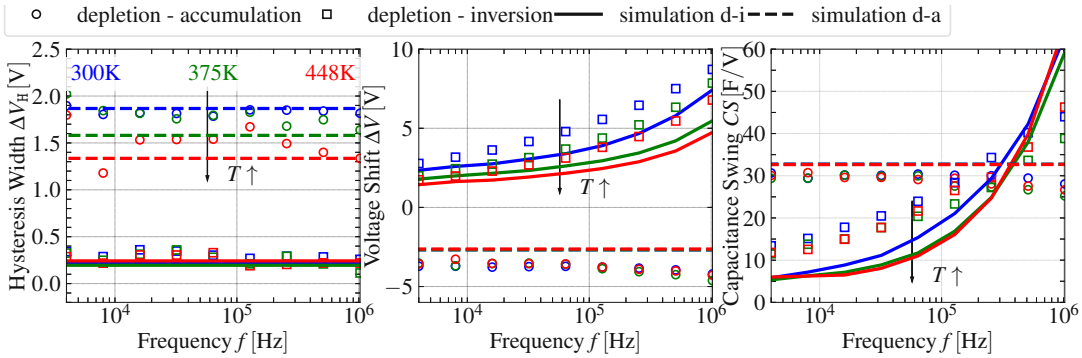

Figure 6.16.: Left: Measured hysteresis width (circles and squares) and simulated C-V (solid and dashed lines) curves. Middle: Voltage shift at C_{cut} for measured and simulated $C-V$. Right: Measured and simulated capacitance swing at C_{cut} in $C-V$ plot From: [100].

A significant fraction of the interface traps become charged, and distortion in the $C-V$ curves can be observed at high frequencies, as illustrated in Fig. 6.15). Furthermore, Fig. 6.16 illustrates the measured and simulated relationships among the hysteresis widths, voltage shifts, and capacitance swings. The significant dependence on the frequency and temperature, transitioning from depletion to inversion, verifies the existence of interface defects, as illustrated in Fig. 6.16, the middle and right panels. The hysteresis width between the depletion and inversion regions was narrow because of the low trap concentration D_{ox}^{1}.

6.5. Hysteresis in $C-V$ of Trench MOSFETs

It has been found [31], [74] that the Si- and a-face types of planar and trench 4H-SiC MOSFETs exhibit different trap densities of states and their spatial distributions from the interface, which affect the $I_{\mathrm{d}}-V_{\mathrm{gs}}$ and $C-V$ curve shifts and shapes. These differences necessitate the application of at least two models (SRH and NMP) with unique trap parameters to accurately calculate system behavior and identify potential defect candidates. The same trap types in the planar devices were demonstrated to affect the hysteresis width and BTI on the $I_{\mathrm{d}}-V_{\mathrm{gs}}$ curves at different temperatures, and their subsequent influence on the hysteresis and stretch-out effect on the $C-V$ characteristics at various frequencies and temperatures. In contrast, within the trench MOSFETs, the change in the hysteresis width strongly depends on the starting gate voltage, and the number of cycles is modeled. The proposed simulation results demonstrate that trap distributions with energy levels below the 4H-SiC mid-gap are the main candidates to explain the hysteresis width. To simulate the hysteresis and stretch-out effect of the $C-V$ curves of this device, the same trap distribution was applied. For measurement and simulation the "up-and-down" $C-V$ scheme was applied, see Fig. 3.3. The black $C-V$ curve in Fig. 6.17, on the left, illustrates an ideal device characterized solely by a fixed positive charge that shifts the entire curve. Before implementing the complete trap system, the quasi-static $C-V$ of the trench device must be adapted and calibrated. This task is not straightforward because we lack precise knowledge about the shape and concentration of commercial devices, necessitating assumptions for our approach. In Fig. 6.17, the left side shows a reduction in capacitance from depletion to inversion, complicating the analysis of traps located near the conduction band. Owing to this fact and the increased mobility in the trench 4H-SiC MOSFETs, the fast interface defect, which was exponentially distributed from the conduction band, became dispensable and was therefore discarded for the simulation of $C-V$ curves (see Fig. 6.17, right). For the simulation of the quasi-static $C-V$ curves, we used the trench MOSFET, as shown in Fig. 1.2c. Because of the p-shield used in the construction, we have a channel on only one side, which potentially increases the overall mobility and consequently reduces the specific resistance of the device. The geometry of this region significantly influences the inversion region of the $C-V$ curves. For calibration, several parameters were used: channel concentration, channel depth (length), p-shield concentration, distance from the channel side trench for the p-shield, drift region thickness, concentration of the drift region, trench depth, and trench width. Upon approximating the ideal characteristics, a major shift from the depletion region to the accumulation region was observed, as shown in Fig. 6.17, left. To simulate this phenomenon, a distribution of donor-like fast traps with high concentrations, extending exponentially from the valence band, was established, as illustrated in Fig. 6.17, right (red lines). In addition to simulating the hysteresis width, the NMP model was employed to incorporate slow donor-like traps with an energy level of 0.6 eV utilizing the valence band. This approach enables the reproduction of the measured $C-V$ curve in the simulation of a trench 4H-SiC MOSFET by exploiting the simulation details, and insights into the charge trapping kinetics of the associated

defects can be gained from the trap behavior. However, to achieve an accurate fit, it is necessary to use precise device parameters and introduce additional traps in the middle of the gap to enhance the hysteresis width in the depletion region.

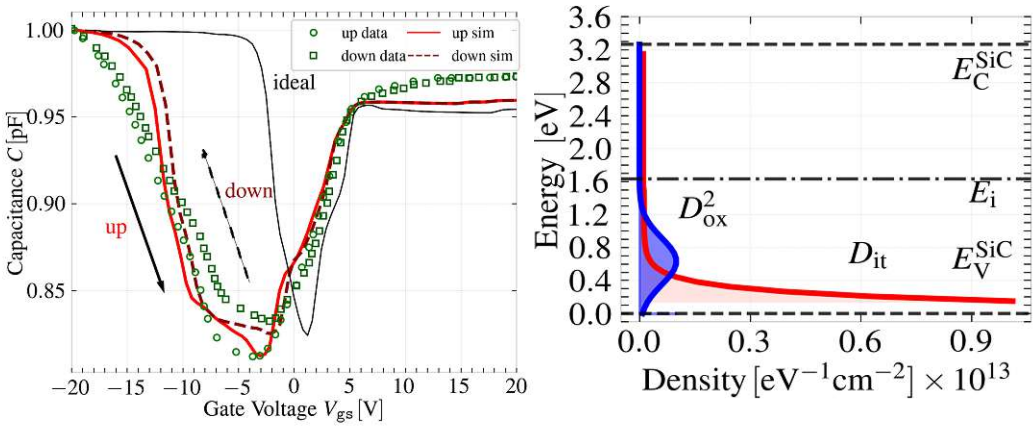

Figure 6.17.: Left: $C-V$ measured and simulated curves of the trench 4H-SiC MOSFETS at room temperature and 100 kHz. The green circles represent the measured data for the up-gate voltage sweep, and the squares represent the down sweep. The solid red line represents the simulated line during the up-gate voltage sweep, and the dashed line represents the down-gate voltage sweep. The black curve represents the ideal quasi-static $C-V$ with positive oxide fixed charges. Right: DOS of the SiC/SiO_2 interface used for simulation of trench devices. Donor-like fast interface traps were exponentially distributed from the valence band with a concentration of $1 \times 10^{13} cm^{-2} eV^{-1}$. Slow border traps with a Gaussian distribution were located at 0.6 eV above the valence band. Note: Fast acceptor-like interface traps are not included in the simulations.

Table 6.5: Example of NMP parameters for simulating the $I_d - V_{gs}$ curves of planar 4H-SiC MOSFETs over a wide temperature range.

Symbol	D_{ox2}	D_{it}	Unit
Trap type	donor-like 1/0	donor-like 1/0	
N_t	1×10^{12}	1.0×10^{13}	cm^{-2}
E_t	E_V+0.6 eV	E_C	eV
S	2.5 ±0.2	–	eV

Note: Fast acceptor-like interface traps with energy levels that are exponentially distributed from the conduction band are not included in the $C-V$ simulations but must be implemented for proper $I_d - V_{gs}$ fit.

7. Outlook and Conclusions

In this chapter, the thesis summary and advancements in the research field are presented. This work concludes with recommendations for future extensions addressing the outstanding issues in characterizing and modeling the dependability of SiC MOSFETs based on the approaches and results achieved.

7.1. Conclusions

A comprehensive dataset describing hysteresis and BTI in various 4H-SiC MOSFETs was produced through device-level simulations. Based on these TCAD simulations and the calibration of the trap parameters from $I_{\mathrm{d}}-V_{\mathrm{gs}}$ and $C-V$ measurements, the following conclusions can be made:

- A two-state NMP framework was employed to calculate the charge trapping kinetics of slow-border traps in lateral and trench 4H-SiC MOSFETs. The slow border traps were modeled to follow a Gaussian distribution in the trap energy.
- SRH theory was used to simulate fast interface traps and needs to be included in the calibration of the channel mobility model. The fast-interface traps were considered to be exponentially distributed in the simulations: acceptor-like traps close to the conduction band and donor-like traps close to the valence band edges.
- Fixed positive traps were used for lateral and trench devices. This may be attributed to ionic charges such as K^+ and Cu^+ [46].
- To simulate the hysteresis width in the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves within the temperature range of 150–300 K for lateral devices, acceptor-like fast interface traps and slow border traps were employed. Both are situated near the conduction band edges.
- Simulating the hysteresis width in the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves over a broader temperature range, from 100 K to 600 K, indicates an anomalous increase in width. An acceptor-like slow-border trap was incorporated with an identical energy level but with a different S parameter to depict this behavior. According to the amphoteric characteristics of P_{b} or P_{bC} centers, they may serve as potential candidates for this behavior rather than mobile ions.
- To replicate the hysteresis width and stretch-out effect in the $C - V$ characteristics of lateral MOSFETs at various frequencies and temperatures, additional slower acceptor-like border traps located in the middle of the 4H-SiC bandgap were incorporated.

- To investigate the hysteresis width in the $I_d - V_{gs}$ curves of the trench MOSFETs over multiple cycles, slow donor-like border traps with energy levels slightly below the mid-gap were applied.
- Fast donor-like interface traps, which are exponentially distributed from the valence band, were employed to reproduce the stretch-out effect from the depletion to the accumulation region in the $C - V$ curves of the trench 4H-SiC MOSFETs.

7.2. Outlook

In summary, to explain the $I_d - V_{gs}$ and $C - V$ characteristics of SIC MOSFETs, a complex set of contributions from traps needs to be considered. Throughout this work, a trap distribution is developed to explain both as well as its temperature dependence. While this work represents a considerable advancement in the modeling of defects in SiC MOSFETs, there are still open issues that need to be tackled towards the establishment of a fully fledged reliability simulation framework for SIC using TCAD tools.

- In this study, we computed the total V_{th} shifts from all traps using a post-processing method. For the most accurate assessment of the reliability simulations, the trap kinetic models must be calculated in a self-consistent manner. However, employing such simulations markedly increases the computing time, resource consumption, and errors, particularly at low temperatures.
- nMOSFETs are extensively utilized for hysteresis width and BTI characterizations. To finalize the inquiry, the pMOSFET has to be evaluated as well. Additionally, the effects of doping concentration, Fermi level, and band gap offsets must be examined.
- The previously demonstrated dependence of BTI and GSI on the switching cycles in SiC trench MOSFETs cannot be accurately represented by a two-state NMP model. The recombination-enhanced defect reaction model was employed to comprehensively characterize the trap kinetics [23], [207]. This model was not used in this study; all traps were simulated independently, indicating no charge exchange between the different trap types.
- Multiple sweep rates at different temperatures must be analyzed and compared with simulation results.
- The addition of SRH fast traps with energy levels close to the conduction band should be used to simulate the trench MOSFETs. Several current references can be used to capture the complicated hysteresis width and shape.
- Recent studies have linked optical emissions occurring after bias switches from the accumulation to the inversion regime with the BTI in trench 4H-SiC MOSFETs [110]. The characterization of radiative transitions for a comprehensive

analysis of the relevant defects must be developed further. Radiative transitions were not utilized in this study.

- By modifying the channel length, one can examine an individual defect to regulate trap kinetics and ultimately produce the defect with controlled parameters.
- The utilization of high-k dielectrics results in a low density of interface traps and may facilitate advancements in future devices [266].
- The influence of the BTI, HCD and hysteresis width at circuit operations [266].
- The NMP approach enables the analysis of BTI, HCD, and hysteresis during circuit operation, allowing it to be used as an enhancement to a standard SPICE model for circuit simulations, or to be utilized self-consistently in mixed-mode simulations [267]. However, this approach was not used in the present study.

  The proposed methodology accounts for multiple trap types, capturing the complete hysteresis behavior across a wide temperature range in both $I_{\mathrm{d}} - V_{\mathrm{gs}}$ and $C - V$ characteristics, as well as in BTI and subthreshold voltage slopes for lateral and trench MOSFETs. The variation between different 4H-SiC crystal faces allows for a detailed evaluation of the influence of the device characteristics on the circuit operation. Therefore, selecting the optimal device configuration for specific applications can enhance efficiency and reduce overall cost and development time.

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Appendix A.

Parameters of Interface Traps

Table A.1: Parameters of Interface Traps.

Parameter	Value	Reference
$D_{it}^{CB_{edge}}$ Si-face	$3 \times 10^{12} - 3 \times 10^{13} cm^{-2} eV^{-1}$	[7], [8], [22], [35], [36], [38], [52], [54], [62], [74], [77], [79], [82], [83], [124], [125], [133], [142], [148], [149], [153], [158], [159], [160], [219], [222], [264], [268], [269], [270], [271], [272], [273], [274], [275], [276], [277], [278], [279], [280], [281], [282], [283], [284]
$D_{it}^{VB_{edge}}$ Si-face	$1 \times 10^{12} cm^{-2} eV^{-1}$	[74]
$D_{it}^{CB_{edge}}$ a-face	$8 \times 10^{11} - 5 \times 10^{12} cm^{-2} eV^{-1}$	[7], [8], [36], [54], [74], [77], [79], [81], [83], [148], [271], [278], [281], [285], [286], [287]
$D_{it}^{VB_{edge}}$ a-face	$5 \times 10^{12} cm^{-2} eV^{-1}$	[74]
$D_{it}^{CB_{edge}}$ C-face	$5 \times 10^{11} - 1 \times 10^{13} cm^{-2} eV^{-1}$	[83], [219], [278]
$D_{it}^{CB_{edge}}$ m-face	$8 \times 10^{12} cm^{-2} eV^{-1}$	[81]
Capture cross section	10^{-21}–$10^{-16}\,cm^{-2}$	[52], [68], [106], [116], [216], [272], [288], [289], [290], [291], [292]

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Table A.1: Parameters of Interface Traps. (Continued)

Parameter	Value	Reference
x_t	<5 nm	[22], [40], [62], [83], [90], [97], [144], [145], [148], [149], [151], [153], [154], [270], [291], [293], [294], [295], [296], [297], [298], [299]
	16 nm for (0001), 14 nm for $(000\bar{1})$, 13 nm for $(11\bar{2}0)$	[79]
Effective fixed charge Q_{eff}	$-1.4 \times 10^{12}cm^{-2}$ for (0001), $-4.2 \times 10^{11}cm^{-2}$ for $(000\bar{1})$, $-1.6 \times 10^{12}cm^{-2}$ for $(11\bar{2}0)$	[79]
N_{ot}, N_{bt}, N_{it}	$2 \times 10^{11} - 4 \times 10^{13}cm^{-2}$	[34], [36], [37], [54], [79], [96], [124], [134], [139], [141], [142], [153], [189], [192], [212], [213], [222], [225], [238], [254], [268], [269], [271], [280], [285], [286], [298], [299], [300], [301], [302], [303], [304], [305], [306]
Type of defects	C positive charged	[22], [40]
	E′ center hole trap positive or neutral	[90]
	Mobile ions Na, K, at >150 °C Mobile positive ions Mo	[90], [121], [123]
	P_b, P_{bC}	[24], [25], [32]
	bonded Si-C-O, carbon clusters, Si-Si bonds	[22]
	E′, O-vacancy, hydrogen bridges (Si–H–Si), C	[11], [23], [26], [41]
Anneal/oxidation shift	NO, N_2O	[67], [79], [89], [96], [101], [116], [155], [276]
	Oxygen, Nitrogen	[37], [38], [77], [141]
	N_2, NO_2, N_2O,	[156], [160], [161], [220]

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Table A.1: Parameters of Interface Traps. (Continued)

Parameter	Value	Reference
	Ar, temperature variation	[33]
	Wet/dry oxidation	[39], [88]
	H,N	[22]
	$POCl_3$	[158], [159]
Modeling type	D_{it}	[117], [145], [151], [183], [212], [214], [220], [222]
	Mobility	[183], [211], [213], [217]
	Occupancy	[216], [217]
	DFT	[217], [230]
	$C-V$	[55], [58], [192], [221], [225], [290], [307], [308], [309], [310], [311], [312], [313], [314]
	$I_d - V_{gs}$	[94], [145], [185], [192], [217], [269], [292], [304], [306], [315], [316], [317]
	V_{th} shift	[106], [254], [292], [314]
Band offsets at SiC/SiO_2	2.7 eV/2.9 eV, 2.6 eV/3.0 eV from $E_C^{SiO_2}/E_V^{SiO_2}$	[8], [26], [36], [57]
	1.09 eV/4.66 eV, 1.24 eV/4.51 eV from $E_C^{SiO_2}/E_V^{SiO_2}$	[296]

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List of Publications

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