

# A standardized approach to characterize hysteresis in 2D-materials-based transistors for stability benchmarking and performance projection

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The hysteresis observed in the transfer characteristics of emerging transistors based on 2D-materials is widely accepted as an important metric related to the device quality. However, the specifics of hysteresis characterization measurements are rarely given, and its mechanistic understanding remains fragmentary. Here, we provide a comprehensive theoretical analysis of the dominant mechanisms contributing to hysteresis: charge trapping by defects from the channel or the gate, the drift of mobile charges, and eventually ferroelectricity. We suggest methods to experimentally distinguish between these phenomena and propose a standardized hysteresis measurement scheme to establish the hysteresis as a comparable metric for the assessment of device stability. Our standardized scheme ensures that hysteresis data can be effectively compared across different technologies and, most importantly, provides a means to extrapolate data obtained on thicker prototypes to subnanometer equivalent oxide thicknesses. This facilitates the systematic benchmarking of insulator/channel combinations in terms of stability, which thereby enables the screening of material systems for more stable and reliable 2D-material-based metal-oxide-semiconductor field-effect transistors (MOSFETs).

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) play the main role in shaping the performance and functionality of integrated circuits. The integration of two-dimensional materials (2D-materials) like transition metal dichalcogenides or one-dimensional materials (1D-materials) like nanowires and nanotubes has emerged as a promising approach to push the performance boundaries of MOSFETs, as their atomically thin nature offers a considerable advantage

for device scaling. However, these next-generation MOSFETs often exhibit pronounced hysteresis in their transfer characteristics<sup>1–8</sup>, a behavior that may be exploited as a useful device feature for future applications:

- Nonvolatile memory: Charge trapping in the gate stack of 2D- and 1D-material MOSFETs could create discrete, retained states suitable for embedded flash-style memory cells<sup>9–14</sup>.

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- Neuromorphic computing: Controlled hysteresis might emulate synaptic plasticity, enabling compact, low-power artificial neural networks in prototype devices<sup>15–17</sup>.
- Tunable sensors and actuators: Hysteretic transfer curves could be harnessed for sensing applications in chemical, biological, and mechanical platforms<sup>18–20</sup>.

Despite these possible applications, hysteresis is usually regarded as a problematic instability that undermines conventional transistor operation. While widely recognized as a critical metric for device stability, many studies still claim hysteresis-free operation without specifying how the hysteresis was measured. We will demonstrate here that an accurate interpretation of hysteresis measurements is anything but trivial, since the observed hysteresis can vary dramatically depending on how it is measured. First, we provide a comprehensive theoretical analysis of the dominant mechanisms that potentially contribute to hysteresis. We examine charge trapping due to defects, the drift and diffusion of mobile charges, as well as ferroelectricity, with a focus on how these mechanisms can be experimentally differentiated. This analysis aims to identify the sources of instabilities in emerging 2D-MOSFETs, facilitating the development of effective countermeasures.

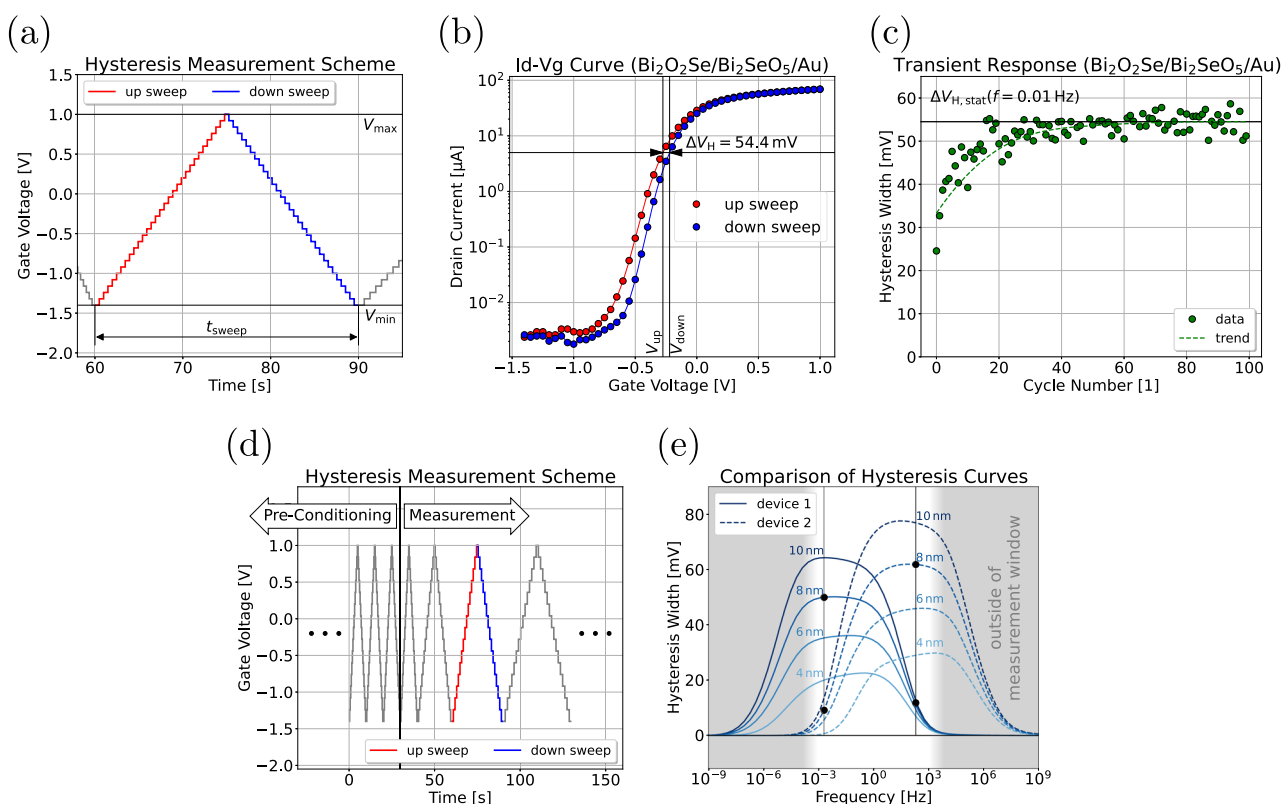
Based on the observation that the measured hysteresis is very sensitive to the sweep frequency and sweep voltage range<sup>21,22</sup>, temperature<sup>13,23</sup>, ambient pressure<sup>20,24,25</sup>, as well as insulator

thickness<sup>26</sup>, we highlight the need to standardize hysteresis measurements to establish the hysteresis as a comparable metric for device stability. This is critical because current literature often reports hysteresis values measured under arbitrary conditions, making the reported values unsuitable for comparison. To address this issue, we propose a unified approach to hysteresis measurements, enabling meaningful comparisons across different technologies and allowing for the extrapolation of data obtained from thicker prototypes to sub-nanometer equivalent oxide thicknesses (EOTs).

## Results and discussion

### The necessity for standardization

Figure 1 a and b present a typical hysteresis measurement performed on a 2D-MOSFET with a  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  gate stack, as reported in<sup>27</sup>. During the measurement, a triangular staircase signal is applied to the gate, defined by its minimum voltage  $V_{\min}$ , maximum voltage  $V_{\max}$ , and frequency  $f = 1/t_{\text{sweep}}$ . Moreover, a small drain voltage ( $qV_d \lesssim k_B T$ ) is applied during the sweep to generate a drain current while keeping the electric field along the channel direction small. Although not strictly necessary, this restriction enables us to approximate quantities along the channel, such as the quasi Fermi level  $E_F^{\text{ch}}$ , as position-independent, thereby simplifying the analysis. The corresponding drain current is recorded throughout the sweep and then plotted against the gate voltage, as shown in Fig. 1b. Due to non-ideal effects, the curves



**Fig. 1 | Hysteresis in the transfer characteristics of metal-oxide-semiconductor field-effect transistors (MOSFETs).** **a** Single gate sweep defined by the minimum voltage  $V_{\min}$ , maximum voltage  $V_{\max}$ , and frequency  $f = 1/t_{\text{sweep}}$ . **b** Drain current  $I_d$  as a function of gate voltage  $V_g$  for a device with a  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  gate stack. Circles represent measured data, and lines serve as a guide to the eye.  $V_{\text{up}}$  and  $V_{\text{down}}$  denote the gate voltages at which the threshold current criterion is reached during the up- and down-sweep, respectively, revealing a positive hysteresis of  $\Delta V_H = V_{\text{down}} - V_{\text{up}} = 54.4$  mV. **c** Transient evolution of the hysteresis over 100 sweep cycles on the same device. The dashed line is a spline fit to highlight the trend, and the solid line marks the quasi-stationary hysteresis value obtained from the average of the last ten measurements. **d** Hysteresis measurement scheme consisting of a

pre-conditioning phase followed by a measurement phase where the sweep frequency is gradually reduced. **e** Simulated hysteresis curves for two  $\text{MoS}_2/\text{HfO}_2/\text{Au}$  devices with different defect distributions. Defect positions  $x_T$  are uniformly distributed across the oxide, while charge-transition levels  $E_T$  and relaxation energies  $E_R$  follow Gaussian distributions (device 1:  $E_T = (-4.4 \pm 0.2)$  eV,  $E_R = (2.5 \pm 0.2)$  eV; device 2:  $E_T = (-4.6 \pm 0.2)$  eV,  $E_R = (1.5 \pm 0.2)$  eV<sup>28</sup>). The gray-shaded area indicates the frequency range inaccessible in typical hysteresis measurements due to instrumental limitations. The vertical lines at 2 mHz and 200 Hz demonstrate that single-frequency device comparisons can lead to opposite conclusions: device 2 appears more stable at 2 mHz, whereas device 1 is more stable at 200 Hz.

for the up- and down-sweep differ, which can be quantified by the hysteresis width:

$$\Delta V_H = V_{\text{down}} - V_{\text{up}}, \quad (1)$$

i.e. the shift of the threshold voltage evaluated at a suitable current criterion. Note that, like with all other phenomena, the same physical mechanism will lead to a different sign of  $\Delta V_H$  in a pMOS as compared to an nMOS. For example, charge trapping from the channel will result in a positive  $\Delta V_H$  for an nMOS and a negative  $\Delta V_H$  for a pMOS. The following discussion will focus on the nMOS case and all signs have to be flipped for pMOS transistors.

The hysteresis width is a key indicator of stability in 2D-MOSFETs, yet it is influenced by many external and internal factors and requires careful experimental control to ensure meaningful comparisons. Most importantly, the choice of insulator material has a critical influence on the density and distribution of defects, as well as on the band alignment at the interface, all of which strongly affect hysteresis. Consequently, hysteresis is not an intrinsic property of the 2D-material alone but rather a characteristic of the entire gate stack. It is therefore essential to always report hysteresis together with the exact gate stack configuration, for example, MoS<sub>2</sub>/HfO<sub>2</sub>/Au.

In addition, environmental conditions play a particularly crucial role, especially for prototype devices that are not encapsulated but directly exposed to the atmosphere. Factors such as ambient pressure and gas composition significantly affect adsorption and desorption processes as well as the stability of electronic states in the hetero-structure, thereby strongly impacting hysteresis. For example, some authors have suggested that air pressure may modulate hysteresis by altering the adsorption of water and oxygen molecules on the MOSFET surface<sup>20,24,25</sup>. To ensure maximum comparability of our hysteresis measurements, we therefore employ a standardized vacuum level of  $5.0 \times 10^{-6}$  and anneal the device at 100°C for 12 hours prior to each measurement to effectively remove adsorbed water and oxygen molecules.

Furthermore, since defects begin in an unknown initial state, the hysteresis in the transfer characteristic is inherently time-dependent and typically requires several sweep cycles to reach a stable cyclo-stationary response at a given frequency. Figure 1c shows the evolution of the hysteresis over 100 cycles measured at 0.01 Hz. Experimentally, the cyclo-stationary hysteresis value is most relevant, as it is independent of the device's prior history and reflects its stability at a given frequency. Comprehensive characterization thus requires measuring this cyclo-stationary hysteresis across a broad frequency range. In practice, the accessible frequency range is constrained at the upper end by the limitations of the experimental setup and at the lower end by the time one is willing to dedicate to the measurement. A realistic measurement window that can be covered with commercially available source measure units (SMUs) is given by  $f \in [1 \text{ mHz} \dots 1 \text{ kHz}]$ . A suitable measurement procedure is sketched in Fig. 1d, starting with a preconditioning phase allowing the device to stabilize at the maximum frequency  $f_{\text{max}}$ . During the subsequent measurement phase, the frequency is gradually decreased between successive sweeps until the minimum frequency  $f_{\text{min}}$  is reached. The frequency change between successive sweeps is chosen to be as small as possible to ensure that the measured hysteresis is a good approximation to the cyclo-stationary hysteresis.

The cyclo-stationary hysteresis  $\Delta V_H$  is best presented as a function of the sweep frequency  $f$ , as shown in Fig. 1e, which displays simulated hysteresis curves for hypothetical devices with a similar MoS<sub>2</sub>/HfO<sub>2</sub>/Au gate stack but different defect distributions in the insulator. Simulations were performed by solving the time dependent master equation for trap occupation, with transition rates given by the nonradiative multi-phonon (NMP) model (Supplementary Note 2). We assumed the defect positions  $x_T$  to be uniformly distributed throughout the oxide, while charge-transition levels  $E_T$  and relaxation energies  $E_R$  were drawn from Gaussian distributions, using known defect parameters for

HfO<sub>2</sub><sup>28</sup>. By sweeping the gate voltage at various frequencies and tracking the time-dependent defect populations, we extracted the effective shift of the threshold voltage and calculated the cyclo-stationary hysteresis for each ensemble.

This figure highlights several challenges in defining a metric for device stability. Real-world measurements are blind to the hysteresis occurring at very low ( $\ll \text{mHz}$ ) or very high ( $\gg \text{kHz}$ ) sweep frequencies due to the limitations of the experimental setup. As such, any metric we define only quantifies device stability over the finite frequency window accessible in the lab. Moreover hysteresis is a strongly frequency-dependent phenomenon: a device that appears perfectly stable at one sweep frequency (see device 1 at 200 Hz) can become completely unstable when driven at a different frequency (see device 1 at 2 mHz). This demonstrates that single-frequency measurements are inadequate for assessing device stability. Therefore, the common practice of reporting hysteresis at a single frequency is misleading. To overcome this problem, one might be tempted to specify the maximum hysteresis  $\Delta V_H^{\text{max}}$  within the measurement window to quantify the worst case. However, Fig. 1e shows that the magnitude of the hysteresis peaks increases with the thickness of the insulator. Consequently, the naive use of this metric would lead to devices with thinner dielectrics being systematically classified as more stable than those with thicker dielectrics. This highlights the necessity of normalizing  $\Delta V_H^{\text{max}}$  to enable meaningful comparisons of devices with varying insulator thicknesses. Therefore, after exploring the underlying physical mechanisms of hysteresis, we suggest to normalize  $\Delta V_H^{\text{max}}$  by the insulator thickness in our standardized hysteresis measurement protocol.

### Physical mechanisms contributing to hysteresis

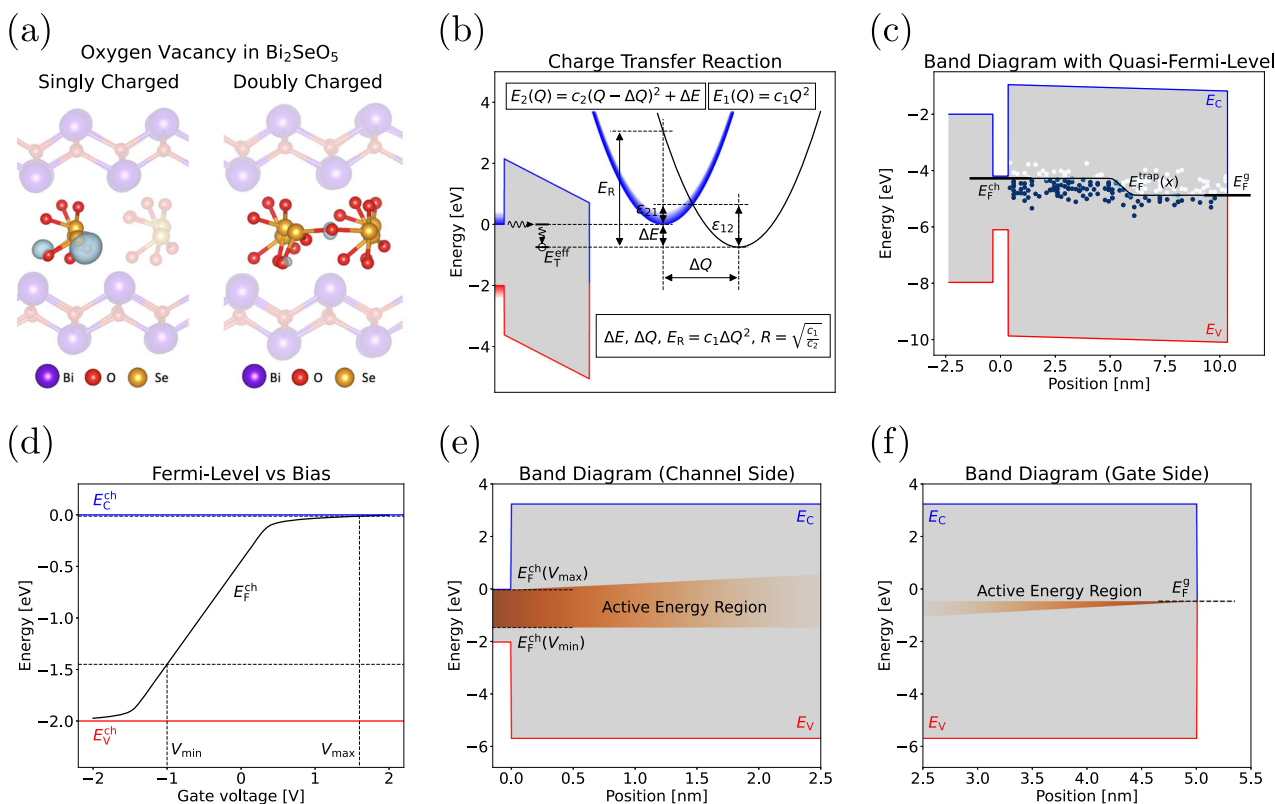
Next, the most frequently encountered physical mechanisms of hysteresis are explained using the example of an n-channel 2D-MOSFET. To accurately describe the device behavior, we extend the model proposed by Marin et al.<sup>29</sup> to account for contact resistances and residual charges in the gate insulator (see Supplementary Note 1). In the following,  $d_{\text{ins}}$  denotes the thickness of the gate insulator and  $C_{\text{ins}} = \epsilon_{\text{ins}}/d_{\text{ins}}$  its capacitance per area. The spatial coordinate  $x$  is defined such that  $x = 0$  corresponds to the channel/insulator interface and  $x = d_{\text{ins}}$  to the gate/insulator interface. In the proposed model, the effective threshold voltage is given by:

$$V_{\text{th}} = V_{\text{th0}} - q(N_d^+ - N_a^-)/C_{\text{ins}} + \Delta V_{\text{ins}}, \quad (2)$$

and consists of three contributions: the threshold voltage  $V_{\text{th0}}$  of the ideal device, the impact of ionized channel defects  $q(N_d^+ - N_a^-)/C_{\text{ins}}$  and the voltage shift  $\Delta V_{\text{ins}}$  caused by the residual charges in the gate insulator. This voltage shift  $\Delta V_{\text{ins}}$  is determined by the total charge  $Q_{\text{ins}}$  and the charge centroid  $x_{\text{ins}}$  of the residual charges:

$$\Delta V_{\text{ins}} = -\frac{Q_{\text{ins}}}{C_{\text{ins}}} \left(1 - \frac{x_{\text{ins}}}{d_{\text{ins}}}\right), \quad Q_{\text{ins}} = \int_0^{d_{\text{ins}}} \rho_{\text{ins}}(x) dx, \quad x_{\text{ins}} = \frac{1}{Q_{\text{ins}}} \int_0^{d_{\text{ins}}} \rho_{\text{ins}}(x)x dx. \quad (3)$$

Hysteresis in the transfer characteristics corresponds to a  $V_{\text{th}}$ -shift between successive up- and down-sweeps<sup>30</sup>. Consequently, the hysteresis width is given by  $\Delta V_H = V_{\text{th}}(t_{\text{down}}) - V_{\text{th}}(t_{\text{up}})$ , where  $t_{\text{up}}$  denotes the time at which the threshold-current criterion is first reached during the up-sweep and  $t_{\text{down}}$  marks the corresponding time during the down-sweep. In this study, we focus specifically on the gate insulator and examine three time-dependent processes whose contributions to reliability problems have been repeatedly suggested in the literature: charge trapping by defects in the insulator<sup>31</sup>, the drift of mobile charges within the insulator<sup>32</sup>, and capacitance variations due to ferroelectricity<sup>33</sup>. Note that, at room temperature, defects in the 2D-material or defects at the hetero-structure interface typically possess very small time constants in the picosecond to nanosecond



**Fig. 2 | Charge capture and emission by defects in the insulator.** **a** Single and double positively charged oxygen vacancies in Bi<sub>2</sub>SeO<sub>5</sub>. **b** Configuration-coordinate diagram illustrating electron capture within the non-radiative multi-phonon (NMP) framework. The potential energy in the two charge states is approximated by  $E_1(Q) = c_1 Q^2$  and  $E_2(Q) = c_2(Q - \Delta Q)^2 + \Delta E$ , where  $Q$  is the configuration coordinate. The capture and emission barriers  $\epsilon_{12}$  and  $\epsilon_{21}$  are governed by the coordinate shift  $\Delta Q$ , the energy shift  $\Delta E$ , the relaxation energy  $E_R = c_1 \Delta Q^2$  and the curvature ratio  $R = \sqrt{c_1/c_2}$ . While  $\Delta Q$ ,  $E_R$ , and  $R$  are defect specific,  $\Delta E$  depends on the field-dependent alignment between the channel conduction band  $E_C^{\text{ch}}$  and the effective charge-transition level  $E_T^{\text{eff}}$  (see Supplementary Note 3). **c** Band diagram showing

the conduction band  $E_C$ , valence band  $E_V$ , and the quasi-Fermi level  $E_F^{\text{trap}}$ , which transitions from the channel Fermi level  $E_F^{\text{ch}}$  to the gate Fermi level  $E_F^{\text{g}}$ . In thermal equilibrium defects below  $E_F^{\text{trap}}$  are predominantly occupied (blue circles), while those above are predominantly empty (white circles). **d** Conduction band  $E_C^{\text{ch}}$ , valence band  $E_V^{\text{ch}}$  and Fermi level  $E_F^{\text{ch}}(V_g)$  of the channel. The Fermi level shifts from deep in the band gap at  $V_g = V_{\text{min}}$  toward the conduction band at  $V_g = V_{\text{max}}$ . **e** Band diagram with the channel-sided active energy region highlighted in orange. The two horizontal dashed lines indicate  $E_F^{\text{ch}}(V_{\text{min}})$  and  $E_F^{\text{ch}}(V_{\text{max}})$ . **f** Band diagram with the gate-sided active energy region highlighted in orange. The horizontal dashed line indicates  $E_F^{\text{g}}$ .

range. Since hysteresis measurements sweep the gate bias over timescales of milliseconds to seconds, these fast defects equilibrate essentially instantaneously at any given bias point. Consequently, although these fast traps still influence the form of the  $I_d$ - $V_g$  curve, most notably by degrading the subthreshold slope, they are too rapid to generate any observable hysteresis in the accessible frequency range. For this reason, room-temperature hysteresis measurements predominantly probe defects in the gate insulator (several Angstrom away from the interface) and the insulator defect density  $D_{\text{ins}}$  extracted from hysteresis measurements can differ substantially from the interface defect density  $D_{\text{it}}$  inferred from the subthreshold slope analysis<sup>34</sup>. Finally, we remark that fast defects in the 2D-material or fast defects at the hetero-structure interface could dominate the hysteresis at operating frequencies in the GHz regime.

### Hysteresis due to charge trapping

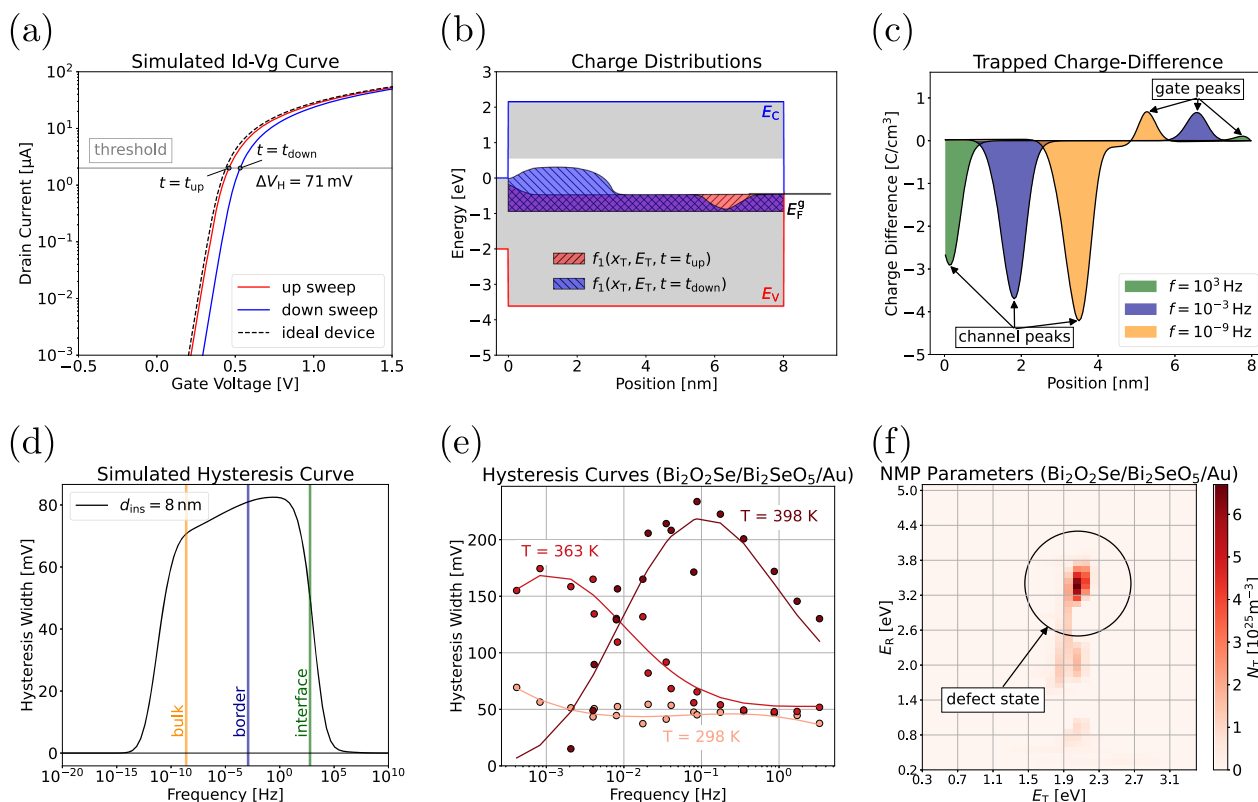
Charge trapping results in a time-dependent charge density  $\rho_{\text{ins}}(x, t)$  within the insulator, which produces an observable hysteresis (Eq. (2) and Eq. (3)). Notably, only charge differences contribute to hysteresis, while the effect of time-independent charge distributions (fixed charges) cancels out. The capture of an electron by an insulator defect conceptually occurs in two steps: First, the electron tunnels to the defect, changing its charge state and disturbing the equilibrium of the original atomic configuration. Consequently, in the second step, the atoms relax towards their new equilibrium positions. Figure 2a

illustrates an example of this process with an oxygen vacancy in Bi<sub>2</sub>SeO<sub>5</sub> deforming due to the capture of an electron. The configuration coordinate diagram shown in Fig. 2b illustrates the capture of an electron from the conduction band of the channel by an insulator defect. The dynamics of this process are governed by the capture rate  $k_{21}^{\text{CB}}$  and the emission rate  $k_{12}^{\text{CB}}$ . These rates are calculated using non-radiative multiphonon (NMP) theory<sup>35–38</sup>, as summarized in Supplementary Note 2, and depend sensitively on three key defect parameters: (i) the spatial position  $x_T$ , since the tunneling probability entering the transition rates decreases exponentially with tunneling distance; (ii) the effective charge-transition level  $E_T^{\text{eff}}$  which shifts with the electric field in the insulator and thus introduces a strong gate voltage dependence of the rates, and (iii) the relaxation energy  $E_R$ , which governs the temperature dependence of the transition rates.

In general, every defect interacts not only with the conduction band but also with the valence band and gate. Accordingly, the total capture rate and emission rate are given by  $k_{21} = k_{21}^{\text{CB}} + k_{21}^{\text{VB}} + k_{21}^{\text{G}}$  and  $k_{12} = k_{12}^{\text{CB}} + k_{12}^{\text{VB}} + k_{12}^{\text{G}}$  respectively, where  $k_{21}^{\text{VB}}$  and  $k_{12}^{\text{VB}}$  denote the capture and emission rates associated with the valence band, and where  $k_{21}^{\text{G}}$  and  $k_{12}^{\text{G}}$  represent the corresponding rates for the gate. The occupation probability  $f_1$  of the defects evolves according to the Pauli master equation:

$$\frac{df_1}{dt} = -f_1 k_{12}(V_g) + (1 - f_1) k_{21}(V_g) \quad (4)$$





**Fig. 3 | Hysteresis due to defects in the insulator.** **a** Exemplary  $I_d$ - $V_g$  curve for a device with a  $\text{MoS}_2/\text{HfO}_2/\text{Au}$  gate stack, simulated with a Gaussian defect band ( $E_T = (-4.4 \pm 0.2)$  eV,  $E_R = (2.25 \pm 0.2)$  eV,  $R = 1$ ) placed across the gate insulator. The points in time at which the current criterion is reached are marked by  $t_{\text{up}}$  and  $t_{\text{down}}$ . **b** Corresponding band diagram of the device showing contour plots of the defect occupancy  $f_1(x_T, E_T, t_{\text{up}})$  in red and  $f_1(x_T, E_T, t_{\text{down}})$  in blue. **c** Charge difference  $\rho_{\text{ins}}(x_T, t_{\text{down}}) - \rho_{\text{ins}}(x_T, t_{\text{up}})$  plotted as a function of position for various sweep frequencies. The channel interaction leads to a negative charge difference near the channel, while the gate interaction leads to a positive charge difference in the

proximity of the gate. If the frequency is reduced, defects with larger capture and emission time constants ( $\tau_c$  and  $\tau_e$ ) situated deeper within the insulator are probed, resulting in a shift of the peaks further into the center of the insulator.

**d** Corresponding hysteresis curve of the device with an insulator thickness of  $d_{\text{ins}} = 8$  nm. The colored vertical lines correspond to the frequencies already shown in (c). **e** Measured (circles) and simulated (lines) hysteresis curves for a device with a planar  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  gate stack as reported in ref. 27, showing a good agreement for varying temperatures. **f** Extracted defect concentration  $N_T(E_T, E_R)$  for the device with the planar  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  gate stack.

where the gate-voltage dependence of the rates is explicitly indicated. As  $t \rightarrow \infty$ , each trap approaches its equilibrium occupancy given by the stationary solution of the master equation, which can be rewritten in Fermi-Dirac form by introducing a position dependent quasi-Fermi level  $E_F^{\text{trap}}(x)$ . Since the transition rates to the channel and gate decay exponentially with the distances  $x_T$  and  $d_{\text{ins}} - x_T$ , respectively, the quasi-Fermi level approaches  $E_F^{\text{ch}}$  at the channel interface and  $E_F^{\text{g}}$  at the gate interface, as illustrated in Fig. 2c. In a sufficiently thick insulator, the equilibrium occupancy of channel-sided defects is therefore governed primarily by  $E_F^{\text{ch}}$ , whereas the equilibrium occupancy of gate-sided defects is determined by  $E_F^{\text{g}}$ .

Therefore, a channel-sided defect may change its charge state when its effective defect level  $E_T^{\text{eff}}$  is crossed by the channel Fermi level  $E_F^{\text{ch}}$ . As illustrated in Fig. 2d, increasing the gate voltage from  $V_{\text{min}}$  to  $V_{\text{max}}$  causes  $E_F^{\text{ch}}$  to sweep across the band gap, thereby defining a region of the band diagram referred to as the channel-sided active energy region (AER), shown in Fig. 2e. Within this energy window, channel-sided defects can undergo charge transitions. Similarly, a gate-sided defect may change its charge state when its effective defect level  $E_T^{\text{eff}}$  is crossed by the gate Fermi level  $E_F^{\text{g}}$ . When the transistor is turned on,  $E_F^{\text{g}}$  covers a portion of the band diagram referred to as the gate-sided AER, shown in Fig. 2f, where gate-sided defects can likewise undergo charge transitions. Note that the gate-sided AER is narrower than its channel-side counterpart because the gate Fermi level is pinned relative to the insulator (assuming a metal gate without a depletion layer). Finally, it should be emphasized that not all defects within the

channel-sided or gate-sided AER actually contribute to hysteresis, since the mean time for charge capture or emission is given by  $\tau_c = 1/k_{21}$  or  $\tau_e = 1/k_{12}$ , respectively. Consequently, defects with  $\tau_c, \tau_e \gg 1/f$  remain effectively frozen during the sweep, whereas those with  $\tau_c, \tau_e \ll 1/f$  equilibrate almost instantaneously at each bias point. Since both groups retain the same charge state during the up-sweep and down-sweep, they do not contribute to hysteresis.

Figure 3a–d illustrate the general physics of charge trapping and the interplay between channel and gate interaction for a representative  $\text{MoS}_2/\text{HfO}_2/\text{Au}$  gate stack. For the simulation a very broad Gaussian acceptor-like defect band was placed across the insulator. Although the figures correspond to a  $\text{MoS}_2/\text{HfO}_2/\text{Au}$  stack, the qualitative conclusions are not material-specific; the same behavior would be expected for other semiconductor-dielectric combinations. Figure 3a shows a single  $I_d$ - $V_g$  for the device where the two time points at which the threshold current is reached are marked by  $t_{\text{up}}$  and  $t_{\text{down}}$ . Figure 3b shows the corresponding band diagram under flat-band conditions and overlays two contour plots of the trap occupation  $f_1(x_T, E_T)$ , where  $x_T$  and  $E_T$  denote the position and the charge transition level respectively. The red contour encloses all defects whose occupancy exceeded 0.5 at  $t = t_{\text{up}}$ , while the blue contour encloses those whose occupancy exceeded 0.5 at  $t = t_{\text{down}}$ . The common region (shaded purple) corresponds to traps that do not contribute to hysteresis in this sweep (as they have approximately the same charge state at both  $t = t_{\text{up}}$  and  $t = t_{\text{down}}$ ). Although the detailed distribution  $f_1(x_T, E_T)$  is complex due to the nontrivial dependence of the time constants

$\tau_c(x_T, E_T)$  and  $\tau_e(x_T, E_T)$  on both position and energy, a clear trend emerges. When the device is turned on, the channel Fermi level rises relative to the insulator, favoring electron capture, while the gate Fermi level simultaneously decreases relative to the insulator, promoting electron emission. Consequently, a net negative charge builds up in the channel-sided AER ( $f_1(x_T, E_T, t_{\text{down}}) > f_1(x_T, E_T, t_{\text{up}})$ ), whereas a net positive charge accumulates in the gate-sided AER ( $f_1(x_T, E_T, t_{\text{down}}) < f_1(x_T, E_T, t_{\text{up}})$ ) during a hysteresis sweep.

This behavior is highlighted in Fig. 3c, which plots the total charge difference  $\rho_{\text{ins}}(x_T, t_{\text{down}}) - \rho_{\text{ins}}(x_T, t_{\text{up}})$  as a function of position for various sweep frequencies. At each frequency, a negative peak (channel interaction) and a positive peak (gate interaction) emerge. Since the threshold-voltage shift has the opposite sign to the trapped charge (Eq. (3)), we conclude that the channel interaction produces positive hysteresis while the gate interaction produces negative hysteresis. Because tunneling probability decays exponentially with distance, the capture and emission time constants  $\tau_c(x_T, E_T)$  and  $\tau_e(x_T, E_T)$  increase sharply for deeper traps. As a result, lower sweep frequencies probe progressively deeper traps, which can also be seen in Fig. 3c where the peaks shift progressively deeper in the insulator center as the frequency decreases. This depth-sensitivity gives rise to the plateau-shaped hysteresis curve in Fig. 3d, with the right (green) edge set by the fastest, interface-proximal traps and the left (yellow) edge by the slowest, bulk traps. Note that in this example the overall hysteresis remains positive because the channel interaction dominates.

Finally, Fig. 3e overlays measured and simulated hysteresis data for a planar  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_3/\text{Au}$  MOSFET ( $L \approx 4.9 \mu\text{m}$ ,  $W \approx 7.9 \mu\text{m}$ ,  $d_{\text{ins}} \approx 6 \text{ nm}$ ) reported by Zhang et al.<sup>27</sup>. Microwave impedance microscopy of  $\text{Bi}_2\text{SeO}_5$  on a Mica substrate yielded an dielectric constant  $\epsilon_r \approx 22$ , corresponding to an equivalent oxide thickness of  $\approx 1.1 \text{ nm}$ . In the simulation, the positive hysteresis was attributed to defects located within the first 2 nm of the insulator near the channel interface. Both the simulation and experimental results consistently show that the hysteresis peak shifts to higher frequencies as the temperature increases, which can be explained by the exponential temperature dependence of the rates (see Supplementary Note 2). In addition, Fig. 3f presents the corresponding defect parameter distribution extracted with the ESI algorithm<sup>39</sup>. The strongly localized distribution with a pronounced maximum at  $(E_T, E_a) = (2.0 \text{ eV}, 3.3 \text{ eV})$  suggests that a single defect species dominates the hysteresis in this device.

### Hysteresis due to mobile insulator charges

Similar to charge trapping, mobile charges (extrinsic contaminants such as  $\text{Na}^+$  and  $\text{K}^+$  or charged intrinsic defects such as oxygen vacancies  $V_{\text{O}}^{\bullet}$ ) result in a time-dependent charge density  $\rho_{\text{ins}}(x, t)$  in the insulator. Notably, such contaminants were a serious issue in early silicon-based devices, as their presence adversely affected device reliability and performance<sup>40,41</sup>.

From a microscopic viewpoint, diffusion occurs as the charges hop between stable lattice sites, requiring them to overcome a specific migration barrier  $E_a$  (Fig. 4a). Macroscopically, the charge movement in the insulator is assumed to be governed by the drift-diffusion (DD) equation<sup>42</sup>, with a spatial independent diffusion constant  $D = D_0 \exp(E_a/k_B T)$  (Supplementary Note 3). In the off state of the device, the electric field in the insulator is negligible and diffusion dominates. In this regime the mobile charges strive for a uniform distribution within the insulator. In contrast, in the on state, the electric field becomes significant and positive charges drift toward the channel while negative charges drift toward the gate.

Figure 4c clearly demonstrates the effect of positively charged mobile ions by overlaying the measured and simulated  $I_d$ - $V_g$  curves of a planar  $\text{MoS}_2/\text{SiO}_2/\text{Au}$  MOSFET ( $L \approx 6.5 \mu\text{m}$ ,  $W \approx 11.7 \mu\text{m}$ ,  $d_{\text{ins}} \approx 30.0 \text{ nm}$ ) as reported in<sup>43</sup>. During the up-sweep, when  $V_g \ll V_{\text{th}}$ , the electric field in the insulator is negligible and the mobile ions remain uniformly distributed. However, once  $V_g \gg V_{\text{th}}$ , the growing

electric field drives these ions toward the channel, shifting the effective threshold voltage. This behavior is most strikingly illustrated in the inset of Fig. 4c, showing a characteristic peak in the subthreshold slope due to ion migration. The peak spans from the point where the electric field becomes significant to the point at which the ions accumulate fully at the channel interface. In the subsequent down-sweep, most mobile charges are still located close to the channel interface, resulting in an effective positive charge difference and thus a pronounced negative hysteresis in the  $I_d$ - $V_g$  curve. Only when the applied voltage drops well below the threshold, rendering the electric field negligible, do the mobile charges redistribute uniformly again. Note that, both positive and negative mobile charges within the insulator contribute to negative hysteresis: positive mobile charges drift toward the channel while negative charges drift away from the channel, resulting in an effective positive charge difference in both cases.

Figure 4d presents the corresponding measured and simulated hysteresis curves of the device, with an excellent agreement between measurement and simulation. In the simulation, the positive hysteresis was attributed to defects in the first 2 nm of the insulator near the channel interface, using electron trap parameters from literature<sup>39</sup>. The negative hysteresis was attributed to mobile  $\text{K}^+$  ions in the  $\text{SiO}_2$  insulator, with parameters  $E_a = 0.98 \text{ eV}$  and  $D_0 = 1.87 \times 10^{-7} \text{ m}^2 \text{ s}^{-1}$ , which align well with experimental values reported in literature<sup>40</sup>. The hysteresis of this device changes from negative to positive when its cooled down, which can be explained by the simulation: The mobility of the ions is suppressed exponentially with decreasing temperature. Consequently, when the temperature decreases from 470 K to 295 K, the ions become immobile and cease to contribute to hysteresis within the measurement window, making charge trapping the dominant mechanism and resulting in a reversal of the hysteresis sign.

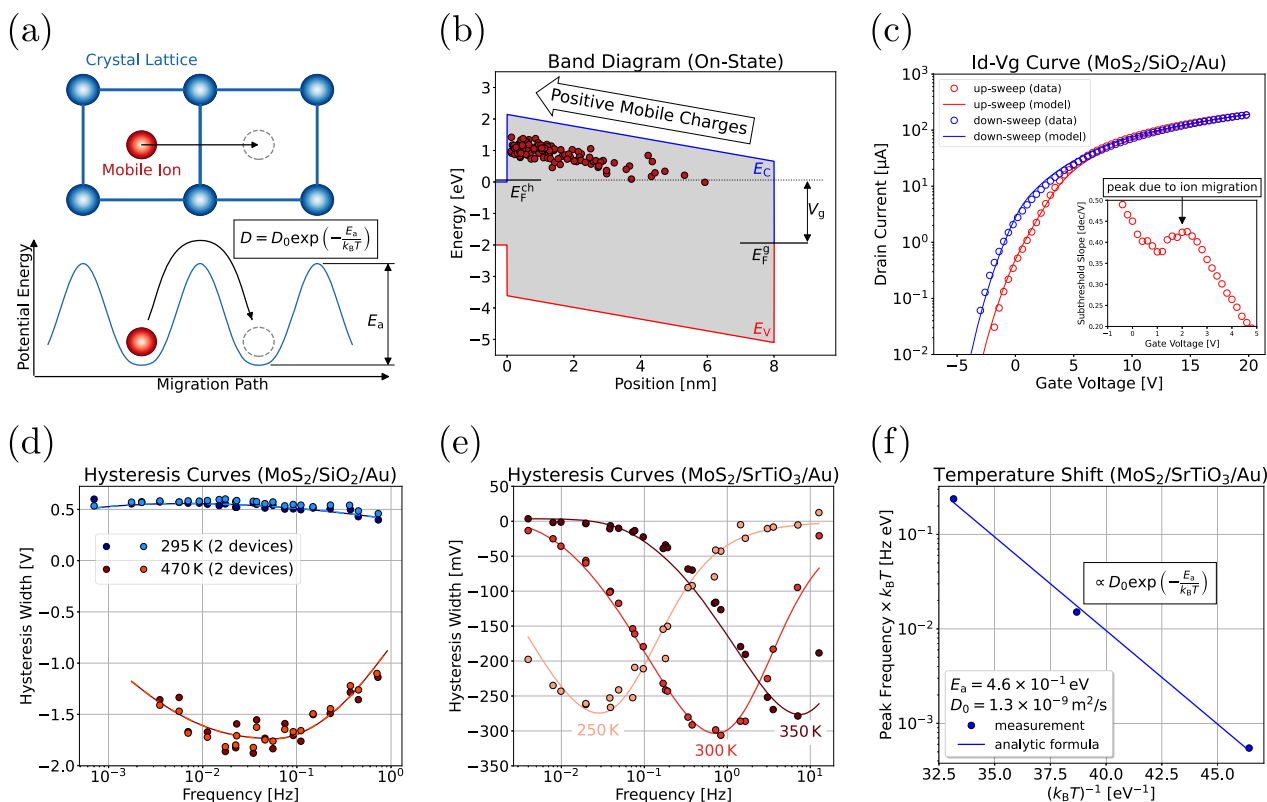
Furthermore, Fig. 4e presents another example of hysteresis curves for a planar  $\text{MoS}_2/\text{SrTiO}_3/\text{Au}$  MOSFET ( $L \approx 2.5 \mu\text{m}$ ,  $W \approx 5.0 \mu\text{m}$ ,  $d_{\text{ins}} \approx 32.0 \text{ nm}$ ) as reported in ref. 44, where the measured and simulated traces are overlaid with remarkable agreement. Capacitance-voltage characterization of identical fabricated  $\text{Au}/\text{SrTiO}_3/\text{Au}$  capacitors yielded a dielectric constant of  $\epsilon_r \approx 26$ , corresponding to an equivalent oxide thickness of approximately 4.8 nm.

At all temperatures, these  $\text{MoS}_2/\text{SrTiO}_3/\text{Au}$  MOSFETs exhibited a pronounced negative hysteresis peak at a characteristic frequency  $f_{\text{peak}}$ . As the temperature rises,  $f_{\text{peak}}$  shifts to higher frequencies, while the peak height  $\Delta V_H(f_{\text{peak}})$  remains essentially unchanged (see Fig. 4e). The negative hysteresis was attributed to mobile charges with a migration barrier of  $E_a = 0.49 \text{ eV}$  in the simulation, consistent with the predicted migration barrier of charged oxygen vacancies in  $\text{SrTiO}_3$ <sup>45</sup>. Based on the simulation, the frequency  $f_{\text{peak}}$  can be approximated by the inverse time required for a single ion to traverse the entire insulator, resulting in

$$f_{\text{peak}} \approx \frac{D_0 E_{\text{eff}} |q|}{d_{\text{ins}} k_B T} \exp\left(-\frac{E_a}{k_B T}\right), \quad (5)$$

where  $E_{\text{eff}}$  represents the time-averaged electric field during the sweep. Figure 4f presents the experimentally extracted values of  $f_{\text{peak}} \times k_B T$  on an Arrhenius plot, resulting in a straight line in perfect agreement with Eq. (5). Since the slope of this line directly corresponds to the migration barrier of the mobile charges, the Arrhenius plot serves as a powerful, simulation-free method for extracting  $E_a$  and thus facilitates the identification of mobile species within the gate stack.

Finally, Fig. 4f demonstrates that mobile species with higher migration barriers freeze out more rapidly upon cooling (i.e. their characteristic hysteresis peaks shift more quickly out of the measurement window) than those with lower barriers. This explains why oxygen vacancies in  $\text{SrTiO}_3$  ( $E_a = 0.49 \text{ eV}$ ) remain active at room temperature (see Fig. 4e), whereas  $\text{K}^+$  ions in  $\text{SiO}_2$  ( $E_a = 0.98 \text{ eV}$ ) are effectively immobilized under the same conditions (see Fig. 4d).



**Fig. 4 | Hysteresis due to mobile charges in the insulator.** **a** Microscopic illustration of mobile-charge migration in a solid. Mobile ions hop between stable lattice sites by overcoming a migration barrier. The diffusion coefficient follows an Arrhenius law,  $D = D_0 \exp(-E_a/k_B T)$ , with pre-factor  $D_0$ , migration barrier  $E_a$ , Boltzmann constant  $k_B$ , and temperature  $T$ . **b** Band diagram showing the drift of positive mobile charges toward the channel. **c** Comparison of measured (circles) and simulated (lines)  $I_d$ - $V_g$  curves for a device with a planar  $\text{MoS}_2/\text{SiO}_2/\text{Au}$  gate stack as reported in<sup>43</sup>. The inset shows the subthreshold slope  $d(\log_{10}(I_d))/dV_g$  of the device with a characteristic peak due to ion migration. **d** Comparison of measured (circles) and simulated (lines) hysteresis curves of the device with the planar

$\text{MoS}_2/\text{SiO}_2/\text{Au}$  gate stack, showing a temperature induced inversion of the hysteresis sign. The negative hysteresis was attributed to mobile  $\text{K}^+$  ions in the  $\text{SiO}_2$  insulator, with parameters  $E_a = 0.98$  eV and  $D_0 = 1.87 \times 10^{-6} \text{ m}^2 \text{ s}^{-1}$ . The positive hysteresis was attributed to defects in the first 2 nm of the insulator, using parameters reported in literature<sup>39</sup>. **e** Comparison of measured (circles) and simulated (lines) hysteresis curves of a device with a planar  $\text{MoS}_2/\text{SrTiO}_3/\text{Au}$  gate stack as reported in ref. 44. The negative hysteresis was attributed to mobile charges with a migration barrier of  $E_a = 0.49$  eV. **f** Arrhenius plot of the temperature induced shift of the hysteresis peak.

### Hysteresis due to ferroelectricity

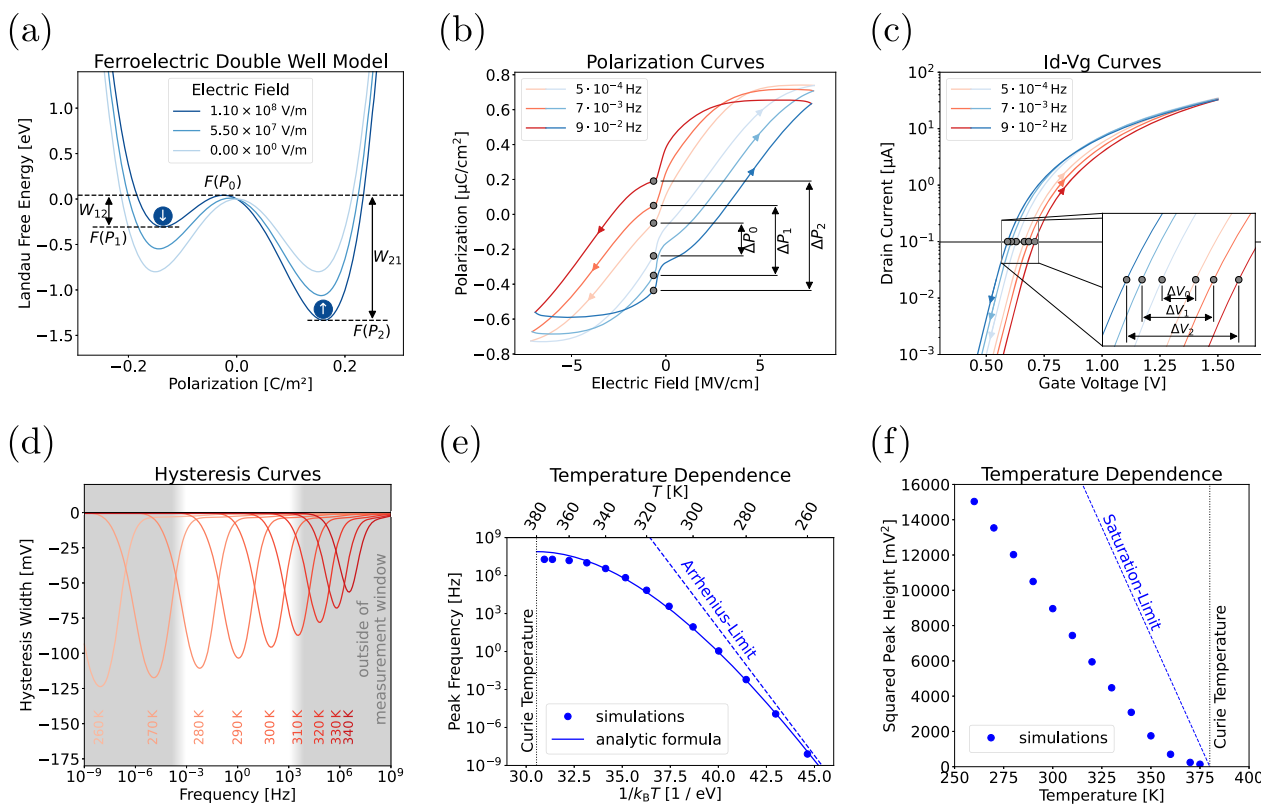
In commercial silicon technology, dielectric materials are used as gate insulators because their properties are ideally independent of the device's history, ensuring stable performance. In contrast, ferroelectric materials (such as some phases of  $\text{SrTiO}_3$  and  $\text{BaTiO}_3$ ) can retain their polarization and thus exhibit a complex, time-dependent polarization response to electric fields<sup>46</sup>. While ferroelectric materials can be deliberately used for neuromorphic<sup>47</sup> or memory devices<sup>48</sup>, their unintended use in conventional MOSFETs introduces instabilities in the transfer characteristics. This risk is significant as experimental devices often use novel gate insulators that may exhibit ferroelectric phases. For instance, the commonly used material  $\text{SrTiO}_3$  can exist in either its paraelectric or ferroelectric phase within a device, depending on factors such as thickness, strain, and temperature<sup>49</sup>.

Figure 5a illustrates the Landau free energy landscape for a material in its ferroelectric phase with its two polarization states  $P_1$  and  $P_2$ . When an electric field is applied, one of the states is lowered in energy, while the other is raised, thereby facilitating the transition between the two polarization states. We follow the approach of Vopsariou et al.<sup>50</sup> and describe the transition as a thermally activated process, which has been effective in replicating experimental data for thin films<sup>51–53</sup> (for further details, see Supplementary Note 4). Figure 5b illustrates the polarization of a ferroelectric gate insulator in a MOSFET as a function of the MOSFET's surface field. Under the effect of a positive field, the ferroelectric layer polarizes in the positive direction until saturation is reached.

Likewise, when a negative field is applied, the ferroelectric layer is polarized in the negative direction, eventually saturating as well. However, the up-sweep (shown in red) and down-sweep (shown in blue) follow different paths, which results in a clearly visible hysteresis loop, characterized by the polarization difference  $\Delta P = P(t_{\text{down}}) - P(t_{\text{up}})$ . As shown in Fig. 5c, the hysteresis in the polarization of the ferroelectric gate insulators translates to a negative hysteresis in the transfer characteristic, given by  $\Delta V_H = \Delta P d_{\text{ferro}}/\epsilon_{\text{ferro}}$ , where  $d_{\text{ferro}}$  and  $\epsilon_{\text{ferro}}$  represent the ferroelectric layer's thickness and background permittivity.

Figure 5d illustrates simulated hysteresis curves for a hypothetical device with a ferroelectric gate insulator. While hysteresis curves of real systems may deviate from those depicted due to the impact of additional terms in the Landau free energy, two general trends can be observed with increasing temperature: First, the hysteresis peak shifts to higher frequencies, which results from the temperature activation of the transition rates. Second, the height of the hysteresis peak decreases due to the reduction of the spontaneous polarization. As shown previously for mobile charges, the temperature-dependent shift of the hysteresis peak provides valuable insight into the underlying processes. When the applied electric fields are moderate, we can approximate the peak frequency by the rate at zero field and obtain

$$f_{\text{peak}} \approx \nu_0 \exp\left(\frac{1}{4} \frac{a_0^2 V (T_C - T)^2}{b k_B T}\right). \quad (6)$$



**Fig. 5 | Hysteresis due to ferroelectric grains in the insulator.** **a** Landau free-energy landscape in the ferroelectric phase with a characteristic double-well structure. The polarization states  $P_1$  and  $P_2$  are separated by the energy barriers  $W_{12} = (W_B - P_S E) V$  and  $W_{21} = (W_B + P_S E) V$ , where  $W_B$  is the zero-field barrier,  $P_S$  the spontaneous polarization,  $V$  the ferroelectric grain volume, and  $E$  the local electric field. **b** Simulated polarization curves for a device with a slightly ferroelectric gate insulator using  $P_S = 0.75 \mu\text{C cm}^{-2}$ ,  $W_B = 8 \times 10^{20} \text{ eV cm}^{-3}$ , and  $V = 0.5 \times 10^{-20} \text{ cm}^3$  (see Supplementary Note 4 for model details). **c** Corresponding  $I_d$ - $V_g$  curves plotted for

various frequencies. The polarization change  $\Delta P$  produces a negative hysteresis shift  $\Delta V_H = \Delta P d_{\text{ferro}} / \epsilon_{\text{ferro}}$ , where  $d_{\text{ferro}}$  is the ferroelectric thickness and  $\epsilon_{\text{ferro}}$  the background permittivity. **d** Corresponding hysteresis curves as a function of temperature. **e** Arrhenius plot of the peak frequency  $f_{\text{peak}}$ .  $f_{\text{peak}}$  reaches its maximum near the Curie temperature and follows Arrhenius-like behavior at lower temperatures, consistent with Eq. (6). **f** Squared peak height as a function of temperature. The peak height saturates once the spontaneous polarization is reached, giving an upper limit  $\Delta V \lesssim (2P_S) d_{\text{ferro}} / \epsilon_{\text{ferro}}$ .

Figure 5e shows the simulated peak frequencies in an Arrhenius plot, demonstrating that the analytical formula given by Eq. (6) effectively captures the temperature dependence observed in the simulation. The peak frequency reaches its maximum near the Curie temperature and exhibits Arrhenius-like behavior at lower temperatures. In practice, this analytical formula can be fitted to experimental data to determine both the ratio  $a_0^2 V / b$  and the Curie temperature  $T_C$ . In addition, Fig. 5f displays the squared peak height as a function of temperature. Unfortunately, there is no straightforward analytical expression for the peak height, as it depends on whether the applied voltage drives the ferroelectric layer into saturation or not.

### Experimental identification of individual mechanisms

While, in real devices, several mechanisms can contribute to hysteresis simultaneously, in many cases a single mechanism dominates the hysteresis process. Identifying this dominant mechanism is essential for improving device stability by implementing appropriate countermeasures. Therefore, we quickly summarize the means to distinguish the studied mechanisms:

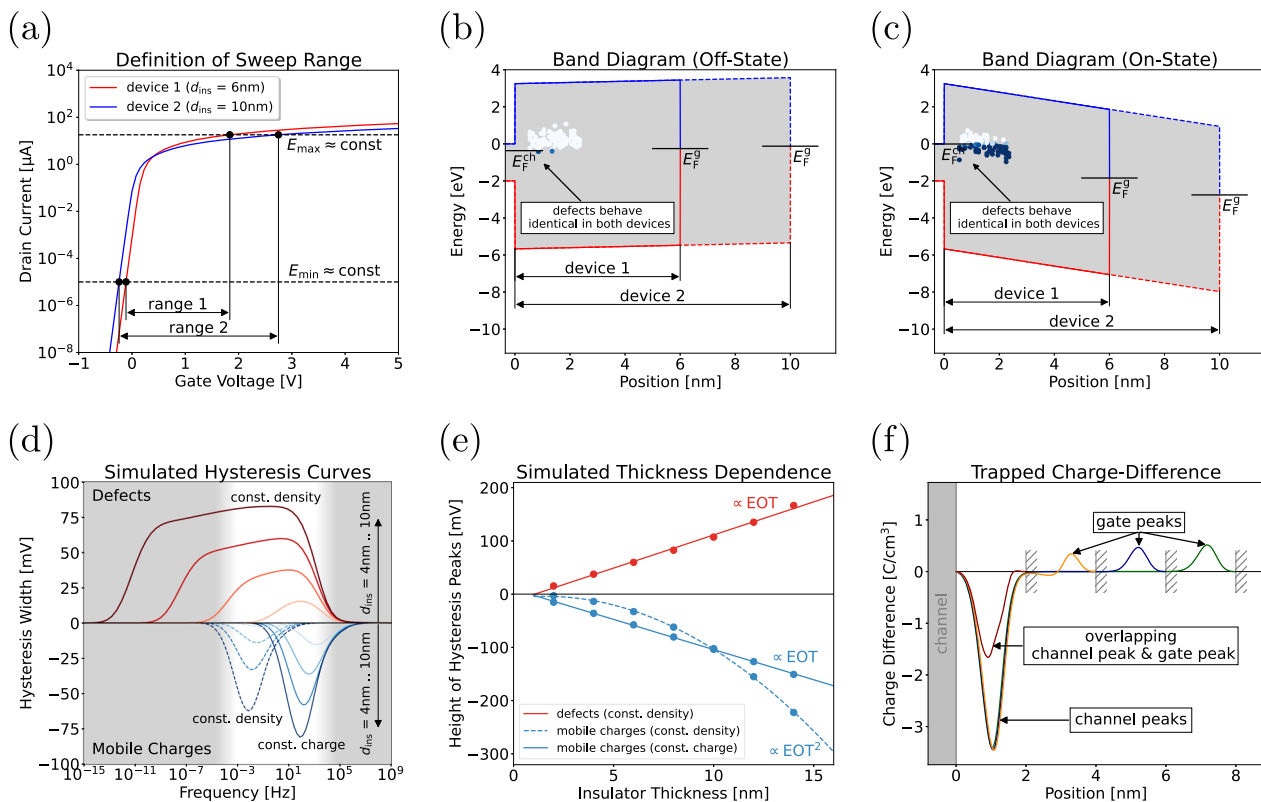
Positive hysteresis is typically associated with charge trapping by defects near the channel, as other mechanisms presented cannot account for the positive sign of the hysteresis. In general, as shown in Fig. 3e, the observed hysteresis peak shifts to higher frequencies due to the temperature activation of the rates. As only defects within the AER can contribute to hysteresis, density functional theory (DFT) calculations can be used to verify whether a particular defect type falls within the AER. Conversely, the NMP parameters extracted from

experiments can be compared with DFT predictions to identify the most likely defect type.

One contribution to negative hysteresis may originate from charge trapping due to defects near the gate. However, the contribution of defects to the hysteresis decreases linearly the closer the defects are to the gate (see Eq. (3)). As a result, in many practical cases, the defect density required to account for the observed negative hysteresis is unreasonably high, i.e.  $\geq 10^{21} \text{ cm}^{-3}$ , which rules out charge trapping by gate-sided defects as the primary mechanism (a possible exception where such a high defect density might still occur is if the insulator is damaged during the deposition of the metal gate). In practice, the required defect density can be estimated by the expression  $\rho_{\text{ins}} \gtrsim -C_{\text{ins}} \Delta V_H 2d_{\text{ins}} / \Delta x^2$ , which is derived from Eq. (3) under the assumption that charges are uniformly distributed within the region  $[d_{\text{ins}} - \Delta x, d_{\text{ins}}]$  near the gate.

A more likely mechanism resulting in negative hysteresis is the drift of mobile charges within the insulator. We demonstrated that mobile charges in the insulator can lead to a characteristic peak in the subthreshold slope (see Fig. 4c), which can be used as a reliable indicator. Furthermore, the height of the hysteresis peaks is temperature independent and the temperature-induced shift of the hysteresis peaks follows an Arrhenius law if the transport obeys the conventional drift diffusion equation with a constant migration barrier. This behavior has been confirmed experimentally (see Fig. 4e and f) and could also be used as an indication for the presence of mobile charges in the insulator. Note that in the case of dispersive transport (e.g. distributed migration barriers) a different behavior is to be expected<sup>54</sup>.





**Fig. 6 | Standardized hysteresis measurement scheme for devices with varying insulator thicknesses.** **a** Standardized sweep ranges to ensure identical minimum and maximum electric fields  $E_{\min}$  and  $E_{\max}$  across devices, enabling a comparable evolution of the electric field during switching. Superimposed band diagrams of two devices in their off-state (**b**) and in their on-state (**c**), showing that defects behave similarly in both devices. **d** Simulated hysteresis curves for devices with insulator thicknesses  $d_{\text{ins}} = \{4 \text{ nm}, 6 \text{ nm}, 8 \text{ nm}, 10 \text{ nm}\}$ . Scenario 1 (red solid): hysteresis due to charge trapping in defects ( $E_T = (-4.5 \pm 0.2) \text{ eV}$ ,  $E_R = (2.5 \pm 0.2) \text{ eV}$ ,  $R = 1$ ). Scenario 2 (blue solid): hysteresis due to mobile charges with constant total

charge ( $E_a = 0.55 \text{ eV}$ ,  $D_0 = 1.0 \times 10^{-10} \text{ m}^2/\text{s}$ ). Scenario 3 (blue dashed): hysteresis due to mobile charges with constant average density ( $E_a = 0.30 \text{ eV}$ ,  $D_0 = 1.0 \times 10^{-10} \text{ m}^2/\text{s}$ ). **e** Corresponding height of the hysteresis peaks as a function of thickness. The points represent the simulated data, while the lines indicate the trend. **f** Charge difference due to charge trapping during quasi-stationary hysteresis sweeps at 1 Hz for devices of varying  $d_{\text{ins}}$ . When the sweep range is adapted to  $d_{\text{ins}}$ , the same defects are probed near the channel (or gate), independent of the insulator thickness.

Finally, ferroelectric materials in the gate stack can also lead to negative hysteresis. Based on our theoretical investigation, we expect that the corresponding height of the hysteresis peak decreases when  $T_C$  is approached. Moreover, we predict that the temperature-induced shift of the hysteresis peaks deviates from an Arrhenius law when  $T_C$  is approached (see Fig. 5d–f). Another indication of ferroelectricity is the ferroelectric phase transition itself, which could be detected experimentally by the characteristic discontinuity in the electric susceptibility, as described by the Curie-Weiss law<sup>46</sup>. Therefore, the phase transition can be specifically explored by measuring the capacitance of the gate stack over an extended temperature range.

**Standardization and normalization of hysteresis measurements**  
After identifying the main mechanisms contributing to hysteresis, we now address the standardization of hysteresis measurements to define a consistent metric for device stability. The maximum hysteresis width  $\Delta V_H^{\text{max}}$  has been shown to scale with insulator thickness<sup>26</sup>. Since different research groups often use samples with varying insulator thicknesses,  $\Delta V_H^{\text{max}}$  must be normalized to allow meaningful comparison across studies.

Critically, this normalization is only valid if the dominant instability mechanism (defects, mobile charges, or ferroelectric grains, ...) evolves with similar dynamics across all devices under test. Accordingly, the sweep range  $[V_{\min}, V_{\max}]$  must be adjusted individually for each device, as illustrated in Fig. 6a–c, ensuring that all devices

undergo a comparable evolution of the electric field in the insulator during switching. This constraint is discussed in more detail in Supplementary Note 5 and can be approximately enforced by keeping both the normalized voltage overdrive  $(V_{\max} - V'_{\text{th}})/\text{EOT}$  and the on-off ratio  $I_d(V_{\max})/I_d(V_{\min})$  constant across hysteresis measurements. These two conditions uniquely define the sweep range for each device and result in a relatively simple measurement rule. We recommend using a normalized voltage overdrive of  $3.5 \text{ MV cm}^{-1}$  and an on-off ratio of  $10^6$  for standardized hysteresis measurements:

$$\frac{V_{\max} - V'_{\text{th}}}{\text{EOT}} = 3.5 \text{ MV cm}^{-1} \quad \frac{I_d(V_{\max})}{I_d(V_{\min})} = 10^6 \quad (7)$$

This range reflects realistic operating conditions for 2D-MOSFETs and is derived from the 2.0 nm technology node specified in the IRDS roadmap<sup>55</sup>, assuming a threshold voltage equal to half of the supply voltage  $V_{\text{dd}}$ . Although also expressed in  $\text{MV cm}^{-1}$ , the normalized voltage overdrive should not be confused with the actual electric field in the insulator. Because the overdrive is normalized by the EOT, an identical normalized value corresponds to a weaker field in high- $\kappa$  dielectrics and a stronger field in low- $\kappa$  dielectrics. We recommend determining the sweep range for each device based on an initial  $I_D$ - $V_G$  measurement performed prior to the hysteresis measurement as illustrated in Fig. 6a. If  $I_d(V_{\min})$  cannot be measured due to the SMU's current resolution,  $V_{\min}$  can be obtained by extrapolating the subthreshold slope.

Figure 6d displays simulated hysteresis curves for devices with varying insulator thicknesses, where the sweep range was adjusted as described above. The figure displays three distinct scenarios: In the first scenario (red), defects with a constant density were placed in the insulator of each device. In the second scenario (blue, solid), mobile charges with a constant total charge  $Q_{\text{ins}}$  were placed in the insulator of each device to simulate the external surface contamination by mobile ions. In the third scenario (blue, dashed), mobile charges with a constant average density  $Q_{\text{ins}}/d_{\text{ins}}$  were placed in the insulator of each device, to simulate intrinsic mobile charges like charged oxygen vacancies. Figure 6e shows the corresponding height of the hysteresis peaks as a function of the insulator thickness  $d_{\text{ins}}$ . The figure reveals that the hysteresis caused by defects scales linearly with  $d_{\text{ins}}$ . Moreover, the hysteresis due to mobile charges scales linearly with  $d_{\text{ins}}$  when the total charge is constant and quadratically with  $d_{\text{ins}}$  when the average charge density is constant. These scaling laws are a direct consequence of the adaptive sweep range and can be understood by the following considerations:

Mobile charges strive for a mostly uniform distribution in the off-state and a distribution that is strongly localized at the channel or gate interface in the on-state. Consequently, the associated shift  $\Delta x_{\text{ins}} = x_{\text{ins}}(t_{\text{down}}) - x_{\text{ins}}(t_{\text{up}})$  of the charge centroid between up- and down-sweep is given in good approximation by  $d_{\text{ins}}/2$  if the insulator is sufficiently thick. As a result, the maximum hysteresis exhibits the following thickness dependence (see Eq. (3)):

$$\Delta V_{\text{H}}^{\text{max}} = \max \left| \frac{Q_{\text{ins}}}{C_{\text{ins}}} \frac{\Delta x_{\text{ins}}}{d_{\text{ins}}} \right| \propto \begin{cases} d_{\text{ins}}, & \text{if } Q_{\text{ins}} = \text{const} \\ d_{\text{ins}}^2, & \text{if } Q_{\text{ins}}/d_{\text{ins}} = \text{const} \end{cases} \quad (8)$$

Moreover, Fig. 6f illustrates the charge difference caused by charge trapping within the devices of varying insulator thicknesses. For sufficiently thick insulators, defects primarily interact with either the channel or the gate, giving rise to two distinct peaks: a channel peak located a fixed distance  $x_{\text{peak}}^{\text{channel}}$  from the channel interface, and a gate peak situated a fixed distance  $x_{\text{peak}}^{\text{gate}}$  from the gate interface. Assuming that either the channel or gate interaction clearly dominates, the maximum hysteresis in devices with sufficiently thick insulators thus scales as follows:

$$\Delta V_{\text{H}}^{\text{max}} = \max \left| \frac{\Delta Q_{\text{ins}}}{C_{\text{ins}}} \left( 1 - \frac{x_{\text{peak}}}{d_{\text{ins}}} \right) \right| \propto \begin{cases} d_{\text{ins}}, & \text{if channel peak dominates,} \\ \text{const,} & \text{if gate peak dominates,} \end{cases} \quad (9)$$

Please note that this scaling law breaks down in ultrathin films, where defects interact simultaneously with the channel and the gate. As such, it should be understood as an idealized trend that applies primarily to thicker films.

Finally, we consider the theoretical scaling of ferroelectric materials. Under the assumption of constant spontaneous polarization, the voltage shift increases linearly with film thickness of the ferroelectric

layer<sup>56</sup>, leading to:

$$\Delta V_{\text{H}}^{\text{max}} = \max \left| d_{\text{ins}} \frac{2P_{\text{S}}}{\epsilon_{\text{ins}}} \right| \propto d_{\text{ins}}, \quad \text{if } P_{\text{S}} = \text{const} \quad (10)$$

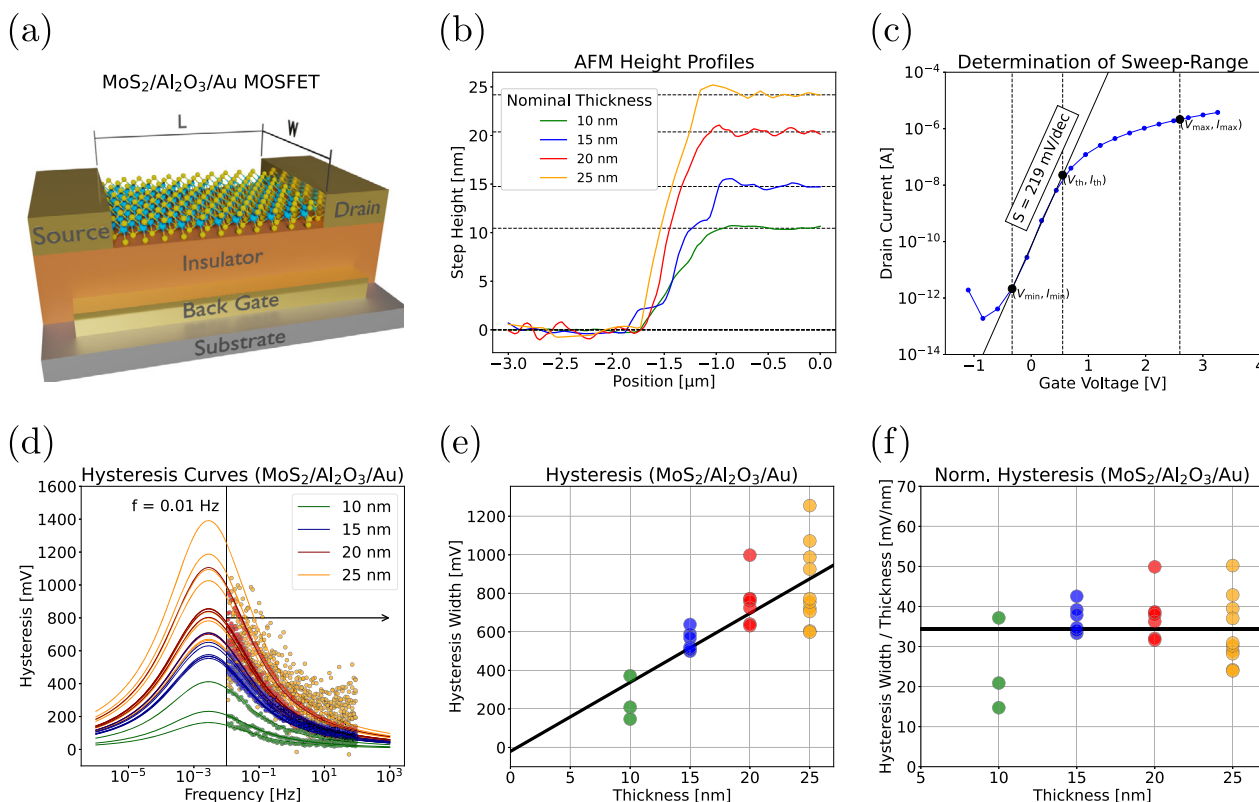
Here too, the idealized relation breaks down in ultrathin films, where surface and interface effects markedly alter the ferroelectric behavior compared to the bulk. In many real systems, depolarizing fields, imperfect screening, and chemical boundary layers reduce or modify  $P_{\text{S}}$  as thickness decreases, leading to substantial deviations from the ideal linear trend<sup>57–59</sup>. As such, the scaling law should be understood as an idealized trend that applies primarily to thicker films.

Table 1 summarizes the hysteresis mechanisms examined in this study along with their respective scaling laws. While the established scaling laws provide an excellent approximation for thick insulators, they begin to break down for ultra thin insulators. Nevertheless, we propose to normalize the hysteresis measurements based on these idealized scaling laws to achieve largely thickness-independent hysteresis results for comparison. To this end, each hysteresis curve is normalized according to its dominant mechanism. For example, we propose to normalize the hysteresis curve by insulator thickness when defects near the channel interface dominate the hysteresis.

To verify our standardized approach to hysteresis measurements, we fabricated planar  $\text{MoS}_2/\text{Al}_2\text{O}_3/\text{Au}$  MOSFETs (see Fig. 7a) with the same lateral dimensions ( $L \approx 2 \mu\text{m}$ ,  $W \approx 20 \mu\text{m}$ ) but varying insulator thicknesses. Device fabrication followed a sequence of process steps as reported in ref. 60 and is summarized in the Methods section for completeness. We characterized the oxide thickness on a representative subset of devices using atomic force microscopy (AFM, see Fig. 7b) and found the nominal and measured thicknesses to agree within a few percent. The nominal  $\text{Al}_2\text{O}_3$  thicknesses were 10 nm, 15 nm, 20 nm, and 25 nm, which, assuming a relative permittivity of  $\epsilon_r \approx 10$ <sup>61</sup>, correspond to equivalent oxide thicknesses of approximately 3.9 nm, 5.85 nm, 7.8 nm, and 9.75 nm, respectively. Before the hysteresis measurements, the sweep range of each device was determined according to Eq. (7). For this purpose, an initial  $I_{\text{D}}-V_{\text{G}}$  curve was recorded in the SMU's autorange mode, as shown in Fig. 7c. The subthreshold region was fitted with a straight line (black solid), yielding a subthreshold slope of  $S = 219 \text{ mV/dec}$ . The effective threshold voltage  $V_{\text{th}}$  and current  $I_{\text{th}}$ , used to define the sweep range according to Eq. (7), are obtained as the point where the drain current deviates by more than 5% from the ideal subthreshold behavior. The resulting hysteresis curves for devices with increasing  $\text{Al}_2\text{O}_3$  thickness are presented in Fig. 7d, where circles denote raw data and lines serve as visual guides. The systematic grouping by insulator thickness confirms that the hysteresis width scales with insulator thickness. Indeed plotting the maximum hysteresis as a function of insulator thickness as shown in Fig. 7e reveals an approximately linear trend, consistent with charge traps near the channel. Finally, normalizing the hysteresis curves by  $\text{Al}_2\text{O}_3$  thickness, as shown in Fig. 7f, makes it nearly independent of thickness,

**Table 1 | Physical Mechanisms Contributing to Hysteresis**

| Contributions to Hysteresis    |          |                                                                                                                                                                  |                            |
|--------------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|
| Physical Origin                | Sign     | Comment on Identification                                                                                                                                        | Thickness Scaling          |
| defects (channel side)         | positive | can be identified by sign                                                                                                                                        | $\propto d_{\text{ins}}$   |
| defects (gate side)            | negative | can often be excluded by required high defect density                                                                                                            | $\propto \text{Const}$     |
| mobile charges (fixed charge)  | negative | can be identified by a characteristic peak in the inverse subthreshold slope; temperature shift follows an Arrhenius law; peak height is temperature independent | $\propto d_{\text{ins}}$   |
| mobile charges (fixed density) | negative | can be identified by a characteristic peak in the inverse subthreshold slope; temperature shift follows an Arrhenius law; peak height is temperature independent | $\propto d_{\text{ins}}^2$ |
| ferroelectricity               | negative | can be identified by a phase transition; temperature shift deviates from Arrhenius behavior; hysteresis height decreases with temperature                        | $\propto d_{\text{ins}}$   |



**Fig. 7 | Standardized hysteresis measurements performed on planar MoS<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/Au MOSFETs.** **a** Device geometry of the fabricated planar MoS<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/Au MOSFETs, with channel length  $L \approx 2 \mu\text{m}$ , channel width  $W \approx 20 \mu\text{m}$ , and oxide thicknesses of 10 nm, 15 nm, 20 nm, and 25 nm. **b** Atomic force microscopy (AFM) line scans for four devices with different oxide thicknesses. **c** Determination of the standardized sweep range based on an  $I_d$ - $V_g$  curve measured prior to the hysteresis measurements. The subthreshold region is fitted with a straight line (black solid), yielding a subthreshold slope of  $S = 219 \text{ mV/dec}$ . The effective threshold voltage  $V_{th}$

and current  $I_{th}$ , used to define the sweep range according to Eq. (7), are obtained as the point where the drain current deviates by more than 5 % from the ideal subthreshold behavior. **d** Hysteresis curves measured on devices with different insulator thicknesses. Circles represent measurement data, and lines are Lorentzian lineshape fits that serve as a guide to the eye. **e** Bare hysteresis width and **(f)** normalized hysteresis width plotted as a function of Al<sub>2</sub>O<sub>3</sub> thickness. The bare hysteresis shows a linear increase with thickness, while the normalized hysteresis remains approximately independent of thickness.

yielding a consistent maximum hysteresis value of approximately  $35 \text{ mV nm}^{-1}$  for this prototype device series.

To demonstrate the applicability of our standardization and normalization scheme to more complex device geometries, we fabricated gate-all-around Bi<sub>2</sub>O<sub>2</sub>Se/Bi<sub>2</sub>SeO<sub>5</sub>/Au MOSFETs (Fig. 8a) with identical lateral dimensions ( $L \approx 2 \mu\text{m}$ ,  $W \approx 20 \mu\text{m}$ ) but varying insulator thicknesses. Device fabrication followed the process described in<sup>62</sup> and is summarized in the Methods section for completeness. During process development, the oxidation step was calibrated by measuring the oxide thickness from transmission electron microscopy (TEM) images (Fig. 8c) as a function of oxidation time (for calibration details, see ref. 27). Using this calibration, we fabricated devices with 7, 12, and 14 oxide layers. Assuming a dielectric constant of  $\epsilon_r \approx 22$  and an interlayer spacing of  $\approx 0.8 \text{ nm}$ , these correspond to equivalent oxide thicknesses of approximately 1.0 nm, 1.7 nm, and 2.0 nm, respectively. Before acquiring hysteresis data, we determined each device's sweep range according to Eq. (7), based on an initial  $I_d$ - $V_g$  curve as exemplified in Fig. 8c. Figure 8d presents the hysteresis curves for the devices with increasing Bi<sub>2</sub>SeO<sub>5</sub> thickness. Plotting the maximum hysteresis width as a function of Bi<sub>2</sub>SeO<sub>5</sub> thickness as shown in Fig. 8e again reveals an approximately linear trend, consistent with charge traps near the channel. Finally, as shown in Fig. 8f, normalizing the hysteresis curves by Bi<sub>2</sub>SeO<sub>5</sub> thickness collapses all curves onto a similar trend, giving a consistent maximum hysteresis width of approximately  $5 \text{ mV nm}^{-1}$  for this prototype device series.

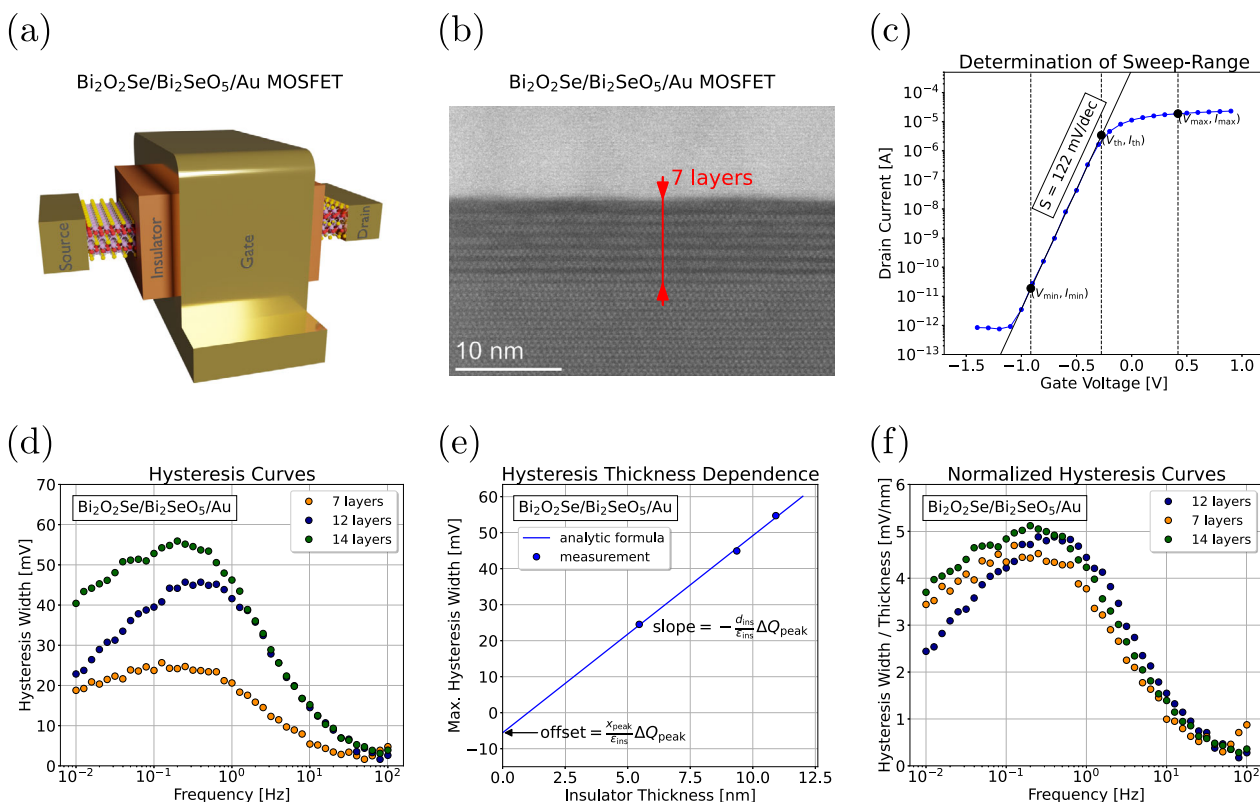
In summary, we successfully applied our standardized hysteresis measurement scheme to two very different device architectures,

planar MoS<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/Au MOSFETs and gate-all-around Bi<sub>2</sub>O<sub>2</sub>Se/Bi<sub>2</sub>SeO<sub>5</sub>/Au MOSFETs. Both device types showed a positive hysteresis that increases linearly with insulator thickness, consistent with charge trapping by defects close to the channel side. Crucially, we demonstrated that the dependence on insulator thickness vanishes when hysteresis curves are normalized by the insulator thickness or equivalent oxide thickness (EOT): all planar devices collapse onto a uniform value of  $\Delta V_H^{\text{max}}/d_{\text{ins}} \approx 35 \text{ mV nm}^{-1}$ , and all GAA devices onto  $\Delta V_H^{\text{max}}/d_{\text{ins}} \approx 5 \text{ mV nm}^{-1}$ . This normalization ensures that the height of the hysteresis curves becomes independent of insulator thickness, ensuring comparability across devices with varying insulator thicknesses. Finally, and most importantly, our approach facilitates the extrapolation of hysteresis data from large EOT prototype devices fabricated during early development stages to scaled devices with small EOT. For instance, if the normalized hysteresis width is  $\Delta V_H^{\text{max}}/d_{\text{ins}} = 10 \text{ mV nm}^{-1}$ , a device with an  $d_{\text{ins}}$  of 2 nm will show a maximum hysteresis of  $\Delta V_H^{\text{max}} \approx 20 \text{ mV}$ , while a device with an  $d_{\text{ins}}$  of 0.5 nm will exhibit a maximum hysteresis of  $\Delta V_H^{\text{max}} \approx 5 \text{ mV}$  within the measurement window.

## Methods

### Fabrication of MoS<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/Au MOSFETs

Prior to device fabrication, few-layer MoS<sub>2</sub> was synthesized on a c-plane sapphire substrate using a two-zone horizontal split tube furnace. After the sample and the precursors were loaded, the tube was pumped down to a pressure of a few mbar and subsequently flushed with argon. This procedure was repeated twice to ensure a clean



**Fig. 8 | Standardized hysteresis measurements performed on gate-all-around  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  MOSFETs.** **a** Geometry of the gate-all-around  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  MOSFETs studied in this work<sup>62</sup>. **b** Transmission electron microscopy (TEM) image of the  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  gate stack, used to determine the oxide thickness as a function of oxidation time. **c** Determination of the standardized sweep range based on an  $I_d$ - $V_g$  curve measured prior to the hysteresis measurements. The subthreshold region is fitted with a straight line (black solid), yielding a subthreshold slope of  $S = 122$  mV/dec. The effective threshold voltage  $V_{th}$  and

current  $I_{th}$ , used to define the sweep range according to Eq. (7), are obtained as the point where the drain current deviates by more than 5 % from the ideal subthreshold behavior. **d** Bare hysteresis curves for devices with different  $\text{Bi}_2\text{SeO}_5$  thicknesses. **e** Maximum hysteresis width as a function of  $\text{Bi}_2\text{SeO}_5$  thickness, showing a linear increase with thickness. **f** Normalized hysteresis curves for devices with different  $\text{Bi}_2\text{SeO}_5$  thicknesses. The collapse of all curves onto a single characteristic profile confirms that, when adopting the standardized measurement scheme, the hysteresis becomes approximately independent of insulator thickness.

environment in the growth chamber. Sulfur powder (Sigma-Aldrich) served as the precursor and was heated to approximately 140 °C under atmospheric pressure with a continuous argon flow as the carrier gas. Positioned downstream, the sapphire substrate was placed face-down above molybdenum trioxide ( $\text{MoO}_3$ ) powder (Sigma-Aldrich), which was heated to -750 °C to enable its evaporation. The growth process was maintained for 10 minutes with an argon flow rate of 10 sccm. Afterwards, the split tube furnace was opened to accelerate the cooling process before the samples were retrieved.

Device fabrication was carried out using a sequence of lithography, dielectric deposition, layer transfer, metal deposition, and etching steps following the approach reported in<sup>60</sup>. Electron-beam lithography was employed for all patterning processes, using a Raith Voyager system in combination with positive PMMA-based electron-beam resist from Allresist. Metal deposition was performed via electron-beam evaporation in a Leybold system (Plassys MEB 550 SL) at a base pressure  $<3.0 \times 10^{-8}$  mbar. The first metallization step defined the gate electrodes and pads, consisting of a bilayer stack of 5 nm titanium and 100 nm gold (Ti/Au). The sample with the pre-patterned back gate was afterwards fully covered by an aluminum oxide ( $\text{Al}_2\text{O}_3$ ) layer grown at 200 °C in a Cambridge Nanotech Savannah atomic layer deposition (ALD), which serves as the gate dielectric. Then the  $\text{MoS}_2$  film was transferred from its original sapphire growth substrate using polystyrene (PS) as a support layer. Thereby, a thick PS layer was spin-coated onto the as-grown  $\text{MoS}_2$ , followed by annealing for one hour at 150 °C. The resulting PS/ $\text{MoS}_2$  stack was then immersed in 30% potassium hydroxide (KOH) in order to release the  $\text{MoS}_2$  from the

sapphire substrate. The detached PS/ $\text{MoS}_2$  film was thoroughly rinsed in deionized water and dried in ambient conditions. Transfer to the target substrate was conducted in a vacuum chamber. The PS/ $\text{MoS}_2$  film was placed on the prefabricated sample, with the  $\text{MoS}_2$  facing the substrate. The chamber was then evacuated, and the sample was left overnight at an elevated temperature of 70 °C and a pressure of  $<1.0 \times 10^{-5}$  mbar to remove adsorbed water and promote clean contact. Subsequently, the temperature was gradually increased to 150 °C during the transfer, after which the sample was left for one hour to allow the PS to soften and to ensure conformal contact between the  $\text{MoS}_2$  and the target substrate. Following a cooling phase, the sample was brought back to atmospheric pressure, and the PS film was subsequently removed by dissolution in toluene. The transistor channels were then patterned using anisotropic plasma etching with an  $\text{Ar}/\text{SF}_6$  gas mixture in an Oxford Cobra reactive ion etching (RIE) system. The fabrication process was completed by defining the source and drain electrodes, formed by depositing a 2 nm Ti and 100 nm Au layer by electron-beam evaporation.

To determine the oxide thickness of the fabricated devices, we performed spectroscopic ellipsometry measurements on the samples with a J.A. Woollam alpha-SE ellipsometer (see Supplementary Fig. 5). The amplitude ratio and phase difference were then fitted using the Cauchy dispersion relation as described in ref. 63 treating the thickness of the samples as free parameters. The values extracted in this way turned out to be 9.9 nm, 15.1 nm, and 19.5 nm and 25.3 nm, which closely match the nominal values. Furthermore, the oxide thickness was also measured by atomic force microscopy (AFM) as shown in



Fig. 7b. The thickness was measured on top of the back gate contact, where the excess  $\text{Al}_2\text{O}_3$  on top of the metal pad was removed by selective wet etching in a KOH solution.

### Fabrication of $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$ MOSFETs

The devices were fabricated following the protocol reported by Tang et al.<sup>62</sup>  $\text{Bi}_2\text{O}_2\text{Se}$  nanoplates were grown on freshly cleaved mica substrates by chemical vapor deposition (CVD) using  $\text{Bi}_2\text{O}_3$  and  $\text{Bi}_2\text{Se}_3$  powders as precursors. Controlled oxidation into  $\text{Bi}_2\text{SeO}_5$  was achieved via UV-assisted intercalative oxidation in a UV- $\text{O}_3$  environment at 110 °C. The oxidation time was used to tune the oxide thickness: durations of 60 s, 90 s, and 120 s yielded approximately 7, 12, and 14  $\text{Bi}_2\text{SeO}_5$  layers, respectively. During this process, the  $\text{Bi}_2\text{O}_2\text{Se}$  nanoplates became fully encapsulated by the epitaxial  $\text{Bi}_2\text{SeO}_5$  layer, forming atomically smooth and conformal core-shell pillars.

These core-shell  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5$  heterostructures were then transferred onto silicon-on-insulator (SOI) substrates prepatterned with Ti/Au (3 nm/8 nm) gate electrodes. Pillars aligned to the buried gate were selected for further processing. Subsequently, an additional 30 nm Au gate-all-around electrode was deposited by electron-beam evaporation, forming a complete GAA configuration.

To define low-resistance contacts, the  $\text{Bi}_2\text{SeO}_5$  dielectric was selectively removed in the source/drain regions using Ar-plasma etching, exposing pristine  $\text{Bi}_2\text{O}_2\text{Se}$ . Finally, Ti/Au (5 nm/45 nm) source/drain electrodes were deposited by electron-beam evaporation, resulting in a low contact resistance of approximately 140  $\Omega\mu\text{m}$  at carrier densities around  $2 \times 10^{13} \text{ cm}^{-2}$ .

The epitaxial  $\text{Bi}_2\text{SeO}_5$  dielectric exhibits a high dielectric constant ( $\kappa \approx 21$ ), while maintaining an atomically smooth and lattice-matched interface with  $\text{Bi}_2\text{O}_2\text{Se}$ . This high-quality interface minimizes trap densities ( $D_{\text{it}} \approx 2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ) and enables near-ideal subthreshold swings ( $S \approx 62 \text{ mV dec}^{-1}$ ). The resulting GAAFETs show enhancement-mode  $n$ -type operation.

### Hysteresis measurements

All electrical measurements on the devices were carried out in a Lakeshore TTPX probe station. To ensure maximum comparability of our hysteresis measurements, we employ a standardized vacuum level of  $5.0 \times 10^{-6}$  and anneal the device at 100 °C for 12 h prior to each measurement to effectively remove adsorbed water and oxygen molecules. Gate and drain voltages/currents were sourced and measured with a Keithley 2636B source measure unit (SMU). The devices were contacted with spring-loaded tungsten needles to prevent the needles from slipping when the temperature changes.

### Hysteresis simulations

The simulations presented in this work, including transfer characteristics, hysteresis curves caused by charge trapping, mobile charge drift, and ferroelectric gate insulators, were conducted using the Python-based framework Comphy (Compact Physics)<sup>28,64</sup>, jointly developed by TU Wien and imec. Comphy is a one-dimensional simulation tool that treats the electric field in the channel direction as a small perturbation compared to the field in the direction perpendicular to the channel. This approximation is valid for most experimental prototype devices, where the dimensions  $W$  and  $L$  are typically on the scale of micrometers, while the gate dielectric thickness measures only a few nanometers. As a result, the electrostatics of the device can be effectively modeled along a one-dimensional cross-section in the direction perpendicular to the channel (see Supplementary Note 1). The framework allows the simulation of various dynamic processes along this direction, such as charge trapping at insulator defects (see Supplementary Note 2), mobile charge drift (see Supplementary Note 3), and the switching behavior of ferroelectric gate insulators (see Supplementary Note 4).

### Data availability

The Source Data underlying the figures of this study are available with the paper. All raw data generated during the current study are available from the corresponding authors upon request. Source data are provided with this paper.

### Code availability

The source code of the Python framework Comphy used in this study is accessible at <https://comphy.eu/> after free registration.

### References

1. Late, D. J., Liu, B., Matte, H. S. S. R., Dravid, V. P. & Rao, C. N. R. Hysteresis in single-layer  $\text{MoS}_2$  field effect transistors. *ACS Nano* **6**, 5635–5641 (2012).
2. Jin, L. et al. High-performance  $\text{WS}_2$  MOSFETs with bilayer  $\text{WS}_2$  contacts. *ACS Omega* **9**, 32159–32166 (2024).
3. Lee, C. et al. Comparison of trapped charges and hysteresis behavior in hBN encapsulated single  $\text{MoS}_2$  flake based field effect transistors on  $\text{SiO}_2$  and hBN substrates. *Nanotechnology* **29**, 335202 (2018).
4. Sheng, C. et al. Synergistic engineering of top gate stack for low hysteresis 2D  $\text{MoS}_2$  transistors. *Adv. Funct. Mater.* **34**, <https://doi.org/10.1002/adfm.202400008> (2024).
5. Kato, R. et al. p-type conversion of  $\text{WS}_2$  and  $\text{WSe}_2$  by position-selective oxidation doping and its application in top gate transistors. *ACS Appl. Mater. Interfaces* **15**, 26977–26984 (2023).
6. Si, M. et al. Steep-slope hysteresis-free negative capacitance  $\text{MoS}_2$  transistors. *Nat. Nanotechnol.* **13**, 24–28 (2017).
7. Roh, J., Lee, J.-H., Jin, S. H. & Lee, C. Negligible hysteresis of molybdenum disulfide field-effect transistors through thermal annealing. *J. Inf. Disp.* **17**, 103–108 (2016).
8. Datye, I. M. et al. Reduction of hysteresis in  $\text{MoS}_2$  transistors using pulsed voltage measurements. *2D Mater.* **6**, 011004 (2018).
9. Zhang, E. et al. Tunable charge-trap memory based on few-layer  $\text{MoS}_2$ . *ACS Nano* **9**, 612–619 (2014).
10. Lipatov, A., Sharma, P., Gruverman, A. & Sinitskii, A. Optoelectrical molybdenum disulfide ( $\text{MoS}_2$ )—ferroelectric memories. *ACS Nano* **9**, 8089–8098 (2015).
11. He, G. et al. Thermally assisted nonvolatile memory in monolayer  $\text{MoS}_2$  transistors. *Nano Lett.* **16**, 6445–6451 (2016).
12. Bertolazzi, S., Krasnozhan, D. & Kis, A. Nonvolatile memory cells based on  $\text{MoS}_2$ /graphene heterostructures. *ACS Nano* **7**, 3246–3252 (2013).
13. Kaushik, N. et al. Reversible hysteresis inversion in  $\text{MoS}_2$  field effect transistors. *npj 2D Mater. Appl.* **1**, <https://doi.org/10.1038/s41699-017-0038-y> (2017).
14. Lim, D., Kim, M., Kim, Y. & Kim, S. Memory characteristics of silicon nanowire transistors generated by weak impact ionization. *Sci. Rep.* **7**, <https://doi.org/10.1038/s41598-017-12347-x> (2017).
15. Jadwiszczak, J. et al.  $\text{MoS}_2$  memtransistors fabricated by localized helium ion beam irradiation. *ACS Nano* **13**, 14262–14273 (2019).
16. Paul, T., Ahmed, T., Kanhaiya Tiwari, K., Singh Thakur, C. & Ghosh, A. A high-performance  $\text{MoS}_2$  synaptic device with floating gate engineering for neuromorphic computing. *2D Mater.* **6**, 045008 (2019).
17. Ko, T.-J. et al. Two-dimensional near-atom-thickness materials for emerging neuromorphic devices and applications. *iScience* **23**, 101676 (2020).
18. Marquez, C. et al. Hysteresis in as-synthesized  $\text{MoS}_2$  transistors: origin and sensing perspectives. *Micromachines* **12**, 646 (2021).
19. Nam, H. et al. Multiple  $\text{MoS}_2$  transistors for sensing molecule interaction kinetics. *Sci. Rep.* **5**, <https://doi.org/10.1038/srep10546> (2015).
20. Urban, F. et al. Gas dependent hysteresis in  $\text{MoS}_2$  field effect transistors. *2D Mater.* **6**, 045049 (2019).

21. Knobloch, T. et al. A physical model for the hysteresis in MoS<sub>2</sub> transistors. *IEEE J. Electron Devices Soc.* **6**, 972–978 (2018).
22. Knobloch, T. et al. Improving stability in two-dimensional transistors with amorphous gate oxides by Fermi-level tuning. *Nat. Electron.* **5**, 356–366 (2022).
23. Al Mamun, M. S., Sainoo, Y., Takaoka, T., Ando, A. & Komeda, T. Hysteresis in the transfer characteristics of MoS<sub>2</sub> field effect transistors: gas, temperature and photo-irradiation effect. *RSC Adv.* **14**, 36517–36526 (2024).
24. Di Bartolomeo, A., Pelella, A., Grillo, A., Urban, F. & Giubileo, F. Air pressure, gas exposure and electron beam irradiation of 2d transition metal dichalcogenides. *Appl. Sci.* **10**, 5840 (2020).
25. Shimazu, Y., Tashiro, M., Sonobe, S. & Takahashi, M. Environmental effects on hysteresis of transfer characteristics in molybdenum disulfide field-effect transistors. *Sci. Rep.* **6**, <https://doi.org/10.1038/srep30084> (2016).
26. Park, R. S. et al. Hysteresis-free carbon nanotube field-effect transistors. *ACS Nano* **11**, 4785–4791 (2017).
27. Zhang, Y. et al. A single-crystalline native dielectric for two-dimensional semiconductors with an equivalent oxide thickness below 0.5 nm. *Nat. Electron.* **5**, 643–649 (2022).
28. Rzepa, G. et al. Comphy—a compact-physics framework for unified modeling of BTI. *Microelectron. Reliab.* **85**, 49–65 (2018).
29. Marin, E. G., Bader, S. J. & Jena, D. A new holistic model of 2-D semiconductor FETs. *IEEE Trans. Electron Devices* **65**, 1239–1245 (2018).
30. Egginger, M., Bauer, S., Schwödau, R., Neugebauer, H. & Sariciftci, N. S. Current versus gate voltage hysteresis in organic field effect transistors. *Monatshefte f.ür. Chem. Chem. Monthly* **140**, 735–750 (2009).
31. Ravichandran, H. et al. Observation of rich defect dynamics in monolayer MoS<sub>2</sub>. *ACS Nano* **17**, 14449–14460 (2023).
32. Shirakawa, H., Kamiya, K., Araidai, M., Watanabe, H. & Shiraishi, K. Origin of the unidentified positive mobile ions causing the bias temperature instability in SiC MOSFETs and their diffusion process. *Appl. Phys. Express* **9**, 064301 (2016).
33. Lin, C.-I., Khan, A. I., Salahuddin, S. & Hu, C. Effects of the variation of ferroelectric properties on negative capacitance FET characteristics. *IEEE Trans. Electron Devices* **63**, 2197–2199 (2016).
34. Ghosh, R. et al. Theoretical insights into the impact of border and interface traps on hysteresis in monolayer MoS<sub>2</sub> FETs. *Microelectron. Eng.* **299**, 112333 (2025).
35. Alkauskas, A., Yan, Q. & Van de Walle, C. G. First-principles theory of nonradiative carrier capture via multiphonon emission. *Phys. Rev. B* **90**, 075202 (2014).
36. Turiansky, M. E. et al. Nonrad: Computing nonradiative capture coefficients from first principles. *Comput. Phys. Commun.* **267**, 108056 (2021).
37. Goes, W. et al. Identification of oxide defects in semiconductor devices: a systematic approach linking DFT to rate equations and experimental evidence. *Microelectron. Reliab.* **87**, 286–320 (2018).
38. Grasser, T. Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities. *Microelectron. Reliab.* **52**, 39–70 (2012).
39. Waldhoer, D. et al. Toward automated defect extraction from bias temperature instability measurements. *IEEE Trans. Electron Devices* **68**, 4057–4063 (2021).
40. Hillen, M. W., Greeuw, G. & Verweij, J. F. On the mobility of potassium ions in SiO<sub>2</sub>. *J. Appl. Phys.* **50**, 4834–4837 (1979).
41. Greeuw, G. & Verweij, J. F. The mobility of Na<sup>+</sup>, Li<sup>+</sup>, and K<sup>+</sup> ions in thermally grown SiO<sub>2</sub> films. *J. Appl. Phys.* **56**, 2218–2224 (1984).
42. Heitjans, P. & Kärger, J. (eds.) *Diffusion in Condensed Matter: Methods, Materials, Models* (Springer, 2005).
43. Smithe, K. K. H., Suryavanshi, S. V., Muñoz Rojo, M., Tedjarati, A. D. & Pop, E. Low variability in synthetic monolayer MoS<sub>2</sub> devices. *ACS Nano* **11**, 8456–8463 (2017).
44. Sattari-Esfahlan, S. M. et al. Stability and reliability of van der Waals high-κ SrTiO<sub>3</sub> field-effect transistors with small hysteresis. *ACS Nano* **19**, 12288–12297 (2025).
45. Walsh, A., Catlow, C. R. A., Smith, A. G. H., Sokol, A. A. & Woodley, S. M. Strontium migration assisted by oxygen vacancies in SrTiO<sub>3</sub> from classical and quantum mechanical simulations. *Phys. Rev. B* **83**, 220301 (2011).
46. Kittel, C. & McEuen, P. *Introduction to Solid State Physics, Global Edition* (Wiley, 2018).
47. Xi, F. et al. Ferroelectric Schottky barrier MOSFET as analog synapses for neuromorphic computing. In *Proc. ESSCIRC 2022-IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, 121–124 (IEEE, 2022).
48. Ali, T. et al. A multilevel FeFET memory device based on laminated HSO and HZO ferroelectric layers for high-density storage. in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 28.7.1–28.7.4 (IEEE, 2019).
49. Haeni, J. H. et al. Room-temperature ferroelectricity in strained SrTiO<sub>3</sub>. *Nature* **430**, 758–761 (2004).
50. Vopsaroiu, M., Blackburn, J., Cain, M. G. & Weaver, P. M. Thermally activated switching kinetics in second-order phase transition ferroelectrics. *Phys. Rev. B* **82**, 024109 (2010).
51. Chen, H. et al. Temperature dependent polarization-switching behavior in Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> ferroelectric film. *Materialia* **14**, 100919 (2020).
52. Zhu, X. L. & Chen, X. M. Ferroelectric properties and polarization dynamics in Ba<sub>4</sub>Sm<sub>2</sub>Ti<sub>4</sub>Ta<sub>6</sub>O<sub>30</sub> tungsten bronze ceramics. *Appl. Phys. Lett.* **108**, <https://doi.org/10.1063/1.4945742> (2016).
53. Nomura, Y., Tachi, T., Kawae, T. & Morimoto, A. Temperature dependence of ferroelectric properties and the activation energy of polarization reversal in (Pr, Mn)-codoped BiFeO<sub>3</sub> thin films. *Phys. status solidi (b)* **252**, 833–838 (2015).
54. Grasser, T., Gos, W. & Kaczer, B. Modeling of dispersive transport in the context of negative bias temperature instability. In *Proc. IEEE International Integrated Reliability Workshop Final Report*, 5–10 (IEEE, 2006).
55. Doe, J. International roadmap for devices and systems (IRDS™) 2023 edition. <https://irds.ieee.org/editions/2023/20-roadmap-2023-edition/130-irds%E2%84%A2-2023-more-moore> (2025).
56. Toprasertpong, K., Takenaka, M. & Takagi, S. Memory window in ferroelectric field-effect transistors: Analytical approach. *IEEE Trans. Electron Devices* **69**, 7113–7119 (2022).
57. Sawabe, Y. et al. On the thickness dependence of the polarization switching kinetics in HfO<sub>2</sub>-based ferroelectric. *Appl. Phys. Lett.* **121**, <https://doi.org/10.1063/5.0098436> (2022).
58. Wang, X. et al. Thickness dependence of PbZrO · 52TiO · 48O3 thin film ferroelectric parameters. *Nano Energy* **107**, 108161 (2023).
59. Junquera, J. & Ghosez, P. Critical thickness for ferroelectricity in perovskite ultrathin films. *Nature* **422**, 506–509 (2003).
60. Polyushkin, D. K. et al. Analogue two-dimensional semiconductor electronics. *Nat. Electron.* **3**, 486–491 (2020).
61. Rajab, K. Z. et al. Broadband dielectric characterization of aluminum oxide (Al<sub>2</sub>O<sub>3</sub>). *J. Microelectron. Electron. Packag.* **5**, 2–7 (2008).
62. Tang, J. et al. Low-power 2d gate-all-around logics via epitaxial monolithic 3d integration. *Nat. Mater.* **24**, 519–526 (2025).
63. Woollam, J. A., Bungay, C. L., Yan, L., Thompson, D. W. & Hilfiker, J. N. Application of spectroscopic ellipsometry to characterization of optical thin films. *Soc. Photo-Opt. Instrum. Eng. (SPIE)* **4932**, 393 (2003).
64. Waldhoer, D. et al. Comphy v3.0—a compact-physics framework for modeling charge trapping related reliability phenomena in MOS devices. *Microelectron. Reliab.* **146**, 115004 (2023).

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## Author contributions

A.K. performed the data analysis of the electrical characterization, carried out the device modeling and simulations, and wrote the manuscript with input from all authors. A.V. fabricated and characterized the  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  and  $\text{MoS}_2/\text{Al}_2\text{O}_3/\text{Au}$  devices. D.W., T.K., and J.K. contributed to model development, implementation of the Comphy framework, and the design of the hysteresis experiments. M.B. calculated material parameters for the  $\text{MoS}_2/\text{SrTiO}_3/\text{Au}$  devices required for modeling. M.R.D. contributed to the implementation of the Comphy framework. P.K. calculated material parameters for the  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  devices required for modeling. B.S., S.M.S.-E., and Y.I. contributed to the electrical characterization of the  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  devices. A.N., C.L., and Y.Z. provided input on experimental design and simulation consistency. L.P., D.P., and T.M. contributed to the fabrication of the  $\text{MoS}_2/\text{Al}_2\text{O}_3/\text{Au}$  transistor devices. S.D. contributed to the fabrication of the  $\text{MoS}_2/\text{SiO}_2/\text{Au}$  transistor devices. X.R.W. contributed to the fabrication of the  $\text{MoS}_2/\text{SrTiO}_3/\text{Au}$  transistor devices. J.T., Y.Z., C.T., Y.L., and H.P. contributed to the fabrication of the  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5/\text{Au}$  devices. M.W. and T.G. supervised and directed the research. All authors discussed the results and contributed to the final version of the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

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