Simulation of Vertically Stacked 2-D Nanosheet FETs

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***Abstract*— We present a simulation study of vertically stacked 2-D nanosheet field-effect transistors (NSFETs). The aim of this investigation is to assess the performance and potential of FinFET alternatives, i.e., gate-all-around (GAA) nanosheet FET at the ultimate nanosheet thickness, using 2-D materials (2DMs). In particular, our numerical study specifically explores the potential of multilayer vertically stacked GAA MoS_2 FETs, considering different geometries and device parameters (e.g., number of stacked nanosheets, spacer dimensions, doping, and so on) with the aim of providing guidelines for obtaining high-performance devices. Sources of nonideality that have been considered are the effects of contact resistance and line-edge roughness (LER), which significantly affect the overall performance of NSFETs. Finally, circuit performance has been benchmarked by calculating the energy per switching and worst case delay of a 32-bit full adder circuit.**

***Index Terms*— 2-D gate-all-around (GAA) nanosheet FET, 2-D materials (2DMs), vertical stacked MoS_2 FETs.**

I. Introduction

As MOORE'S law approaches its scaling limits, researchers are extensively exploring new materials and device structures for future technology nodes. The scaling of silicon FinFET technology beyond the 5-nm technology node leads to short-channel effects (SCEs), which significantly degrade device performance [1], [2]. This challenge has led to a shift from tri-gate FinFETs to a gate-all-around (GAA) Si nanosheet architecture [1], [2], [3], [4], which has demonstrated superior electrostatic control compared to FinFETs [5]. However, reducing the silicon channel thickness below 5 nm, which is the key element to further improve SCE reduction, leads to quantum confinement effects and mobility degradation [6], [7]. To address this issue, 2-D materials (2DMs) seem to be the natural choice to further sustain Moore's law, as they offer a distinct advantage over conventional silicon channel transistors in terms of scalability due to their atomic thinness [8] and do not suffer from mobility degradation and quantum confinement effects unlike silicon nanosheets [8], [9], [10]. In addition, recent advances in the growth of large-area 2-D TMD films [10], [11], [12] have led to considerable improvement in terms of fab-compatible integrability, paving the way for their exploitation as a channel material in advanced technology node transistors at the ultimate scaling [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19].

In recent years, a limited but growing number of experimental demonstrations of vertically stacked 2-D nanosheet FETs have been successfully realized [14], [15], [20], [21], [22], [24], showing that the ON-current (I_{ON}) in vertically stacked multi-MoS_2-channel FETs can be improved for the same footprint area [23]. On the other hand, comprehensive and predictive theoretical models of these devices are still lacking, as well as a thorough investigation of the device performance throughout the parameter space. In [23], a compact model based on drift-diffusion (DD) transport has been used to evaluate the performance of multichannel 2-D nanosheet FETs, while in [14] a semiclassical DD simulation approach has been used to study the performance of vertically stacked 2-D nanosheet transistors. However, the simulation of ultrashort 2DM-based FETs requires a full quantum treatment, to fully capture the mechanisms at play at the nanoscale.

In this article, we present a simulation study of vertically stacked 2-D nanosheet FETs by self-consistently solving the 3-D Poisson and the Schrödinger equations through the nonequilibrium green's function (NEGF) formalism within the ballistic approximation, thus providing a full quantum treatment and an upper bound for the device performance, while considering different geometries and configurations. In particular, we have focused our attention on three device structures: 1) monolayer MoS_2 double-gate FET (DG FET) [Fig. 1(a)]; 2) gate-all-around (GAA) vertically stacked multilayer MoS_2 FETs (GAA-FET) [Fig. 1(b)]; and 3) multilayer MoS_2 FETs with a gate placed all around the stacking perimeter, but not in between the layers (GAP-FET) [Fig. 1(c)], which, if functional, could greatly reduce the fabrication complexity of 2DM-based nanosheet FETs. In fact, this GAP structure is the intermediate step in the fabrication of 2-D GAA-FETs, as described in a recent paper by TSMC, see [24]. Avoiding

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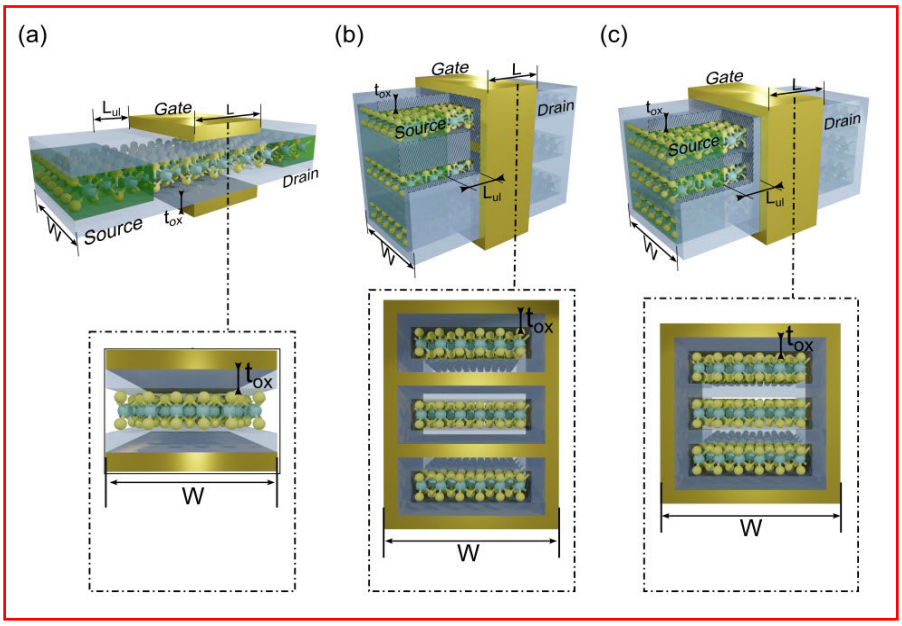

Fig. 1. Schematic of (a) DG-FET, (b) GAA 3L-FET, and (c) GAP 3L-FET with cross-sectional view in the middle of the device. The regions in green indicate the doped source and drain regions. (b) and (c) (Top) Also show a cutaway corresponding to the source region (highlighted by black dashed lines).

the inclusion of the metal gate between the MoS_2 layers would reduce processing complexity, lower cost, and increase yield. Indeed, the performance of GAP-FET has recently been studied by INTEL [22], but the potential of this technological solution is still unknown. First, we have compared the performance of these devices in terms of I_{ON} (for fixed OFF-current) and subthreshold swing (*SS*) in the ideal situation. In addition, we have investigated the effect of: 1) spacer length and doping between source/drain and gate; 2) the contact resistance; and 3) the line-edge roughness (LER) on the performance of the devices.

We show that vertical stacking of 2-D channels can be a viable solution to meet the performance requirements of the IRDS at a 1-nm technology node [26] even in the presence of nonidealities. Finally, we have benchmarked the circuit performance of a nanosheet field-effect transistor (NSFET) by calculating the power and delay of a 32-bit full adder circuit.

This article is organized as follows. In Section II, we present in detail the device structures and the simulation approach adopted. In Section III, we present the results, covering the device space parameter. In Section IV, we discuss important nonideality effects. In Section V, we compare the circuit performance of GAA-FETs, and Section VI summarizes the main results of this article.

II. Device Structure and Simulation Approach

This section presents the device structures investigated and the simulation approach adopted. A sketch of the device geometries is shown in Fig. 1. In Fig. 1(a), we show a schematic representation of the DG-FET structure (and transversal cross sections), which consists of a monolayer MoS_2 channel of 10 nm length (L), 13 nm width (W), and a dielectric oxide with dielectric constant of 3.9 and thickness of 1 nm. The length of both the source and drain region is 10 nm with a doping of 3.2×10^{13} cm^{-2}. Open boundary conditions have been considered at the channel ends. The GAA-FET is shown in Fig. 1(b), i.e., multiple monolayer MoS_2 channels (of the same length and width as the DG FET) stacked vertically, each separated by a dielectric oxide layer of $t_{ox} = 1$ nm of SiO_2 and each is surrounded by a metal gate all around to eliminate interaction and tunneling between adjacent channel layers. The GAP-FET structure is shown in Fig. 1(c), which is similar to the one in Fig. 1(b), but without the metal gates embedded between the stacked layers.

We have solved the 3-D Poisson and the Schrödinger equations self-consistently within the NEGF framework as implemented in our in-house open-source simulator NanoTCAD ViDES [27], [28]. A two-band tight-binding Hamiltonian [29] is used to describe the channel material considering an energy gap of $E_g = 1.8$ eV and an effective mass of $m_e^* = 0.572\ m_e$, where m_e is the free electron mass [29]. We have assumed independent channel layers and no interaction and tunneling between the layers. For all the considered devices, we have set the source-to-drain voltage (V_{DS}) equal to 0.6 V.

The effect of the contact resistance has been included by postprocessing the transfer characteristics considering resistances in series to the source and the drain terminal of the device as described in Appendix. The effect of LER is investigated by considering atomistic defects at the edge of the MoS_2 flakes [30], by breaking the nearest neighbor bonds in the Hamiltonian (i.e., setting the hopping parameter equal to zero and considering a very large onsite energy as in [30]).

III. Results and Discussion

The comparison of the transfer characteristics of the DG FET, the three-layer GAA-FET, and the three-layer GAP-FET is shown in Fig. 2. The GAA-FET has the highest ON-current, followed by the GAP-FET and the DG FET. This is due to

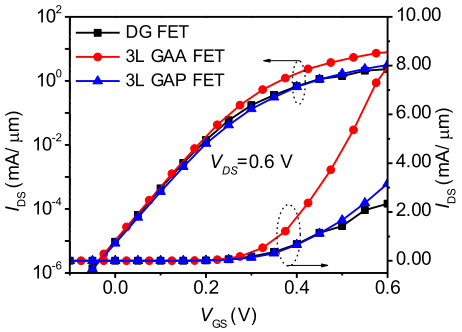

Fig. 2. Transfer characteristics of DG FET, GAA 3L-FET, and GAP 3L-FET on a linear and semi-log scale.

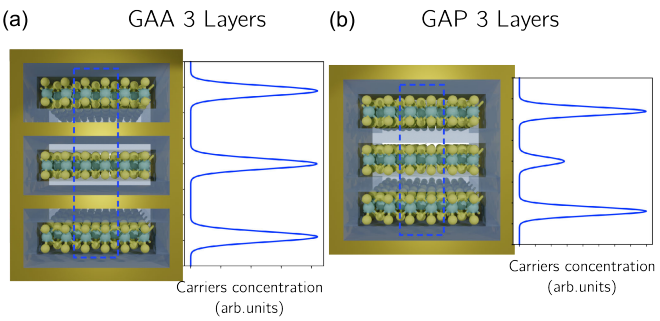

Fig. 3. Average electron concentration in the ON-state of the device at the middle of channel width over a range of 4 nm in width direction of (a) GAA-FET and (b) GAP FET.

TABLE I
COMPARISON OF PERFORMANCE PARAMETERS OF DG FET, GAA-FET, AND GAP-FET. WE HAVE CONSIDERED $V_{DD} = 0.6$ V AND $I_{OFF} = 10^{-5}$ MA/μM

Parameters	DG FET	GAP 3L-FET	GAA 3L-FET	IRDS (1 nm node)
SS (mV/decade)	60	62	60	< 70
I_{ON} (mA/μm)	2.34	3.2	8.0	> 0.753

the superior electrostatic control of the GAA-FET compared to the GAP-FET and the larger number of conductive channels compared to the DG-FET. In particular, the GAP-FET has the same number of conductive channels (i.e., three) as the GAA-FET, but poorer electrostatic control, especially in the middle layer. We observe that the ON-current of the GAA-FET is almost three times higher than that of the DG-FET. This suggests that the GAA-FET maintains the same level of electrostatic control as the DG-FET for each individual layer, resulting in a cumulative amplification of the current.

The situation is quite different in the GAP-FET structure. In this case, the electrostatic control of the gate is weaker than in the DG-FET and the GAA-FET. As a result, the current in the GAP 3L FET is not amplified by the number of channels. This is because the gate is less effective in controlling the potential in particular for the middle channel compared to the top and bottom channels, resulting in reduced current flow, as shown in the three-layer average carrier density plot for both the GAA-FET and the GAP-FET in Fig. 3(a) and (b), respectively. Nevertheless, the GAP-FET shows overall excellent electrostatic control as indicated by the near ideal *SS* (i.e., 62 mV/dec as shown in Table I). Fig. 2 demonstrates that the three-layer GAP FETs show a significant improvement in ON-current compared to the single-layer DG FET.

The comparison of the performance parameters *SS* and I_{ON} of DG FET, GAA-FET, and GAP-FET together with the IRDS [26] requirement for the 1-nm node is shown in Table I, considering an OFF-current $I_{OFF} = 10^{-5}$ mA/μm and supply voltage $V_{DD} = 0.6$ V. Under ideal conditions, all three devices meet the IRDS requirement. In Fig. 4(a) and (b), we present the comparison of one-layer (1L), two-layer (2L), and three-layer (3L) MoS_2 stacked GAP-FET and GAA-FET, respectively.

As expected, the ON-current of the GAA device increases linearly with the number of MoS_2 layers and shows a sublinear behavior for the GAP-FET case. Again, this effect can be attributed to the weak electrostatic control of the gates with respect to the MoS_2 middle layers.

These results indicate that the vertical stacking of the channels is a viable technique to improve the drive current of the 2-D channel material-based devices without increasing the device footprint as long as the gates are included between the channel layers.

IV. PERFORMANCE ANALYSIS OF NSFETS: EXPLORING DEVICE PARAMETER SPACE AND NONIDEALITIES

We now investigate the performance of NSFETs while scanning the device parameter space (i.e., considering several underlap lengths and doping) and considering the influence of nonidealities on the device characteristics such as contact resistance and line-edge roughness.

In Fig. 5, we show the transfer characteristics considering different spacer underlap lengths (L_{ul}) and doping (N_{ul}) for the single-channel layer GAA-FET case. It can be observed from Fig. 5(a) that I_{ON} of the device decreases with increasing spacer length (intrinsic spacer region). The degradation of I_{ON} is attributed to the potential barrier in the spacer/underlap region as shown in the inset of Fig. 5(a). The potential barrier in the underlap region (of 6 nm length) can be reduced by doping this region as shown in Fig. 5(b).

Another important effect to consider is the contact resistance (R_{SD}). In the simulations shown in the previous section, we have considered an ideal ohmic contact between the metal and the MoS_2, which represents the upper limit of the device performance. In real devices, however, the source and drain contacts present an intrinsic resistance (e.g., due to an accumulation layer, sheet resistance, metal/semiconductor interface, and so on), which we have modeled by a lump resistance corresponding to the source and drain contact, i.e., R_S and R_D. According to IRDS, their sum $R_{SD} = R_S + R_D$ should be $R_{SD} < 232\ \Omega \cdot$ m. To investigate the effect of the contact resistance, we performed postprocessing of the current–voltage data and included a resistor at both the source (R_S) and drain (R_D) terminals while fitting the simulation results with

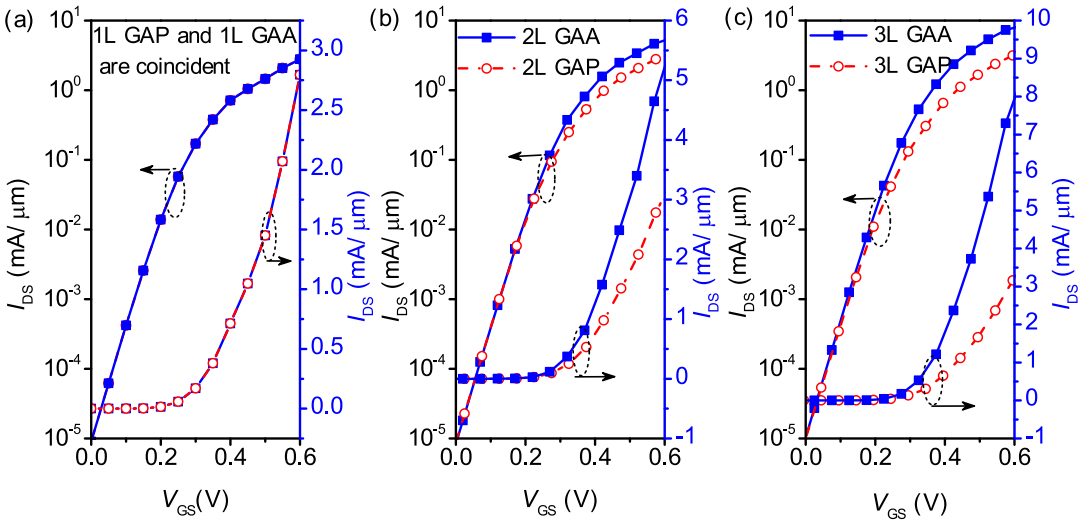

Fig. 4. Comparison of transfer characteristics of (a) 1L, (b) 2L, and (c) 3L GAA and GAP FETs.

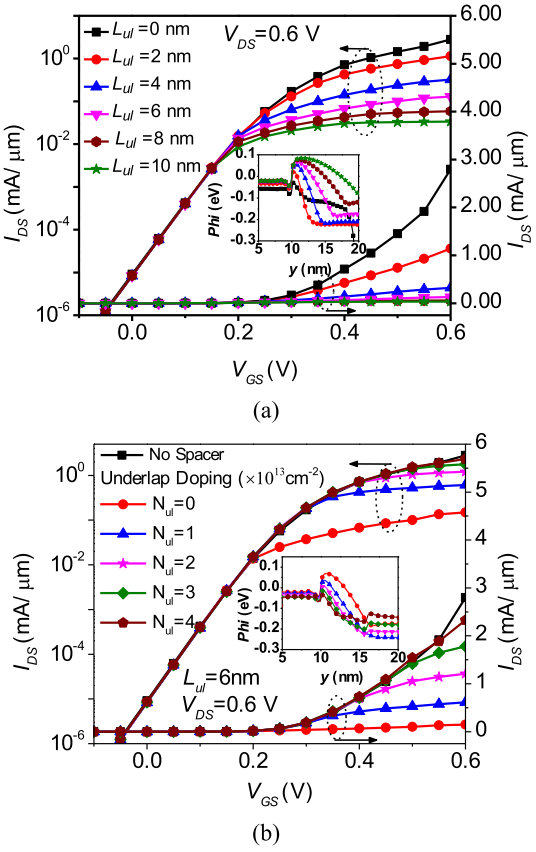

Fig. 5. Impact of (a) spacer length and (b) spacer doping on GAA-FET transfer characteristics.

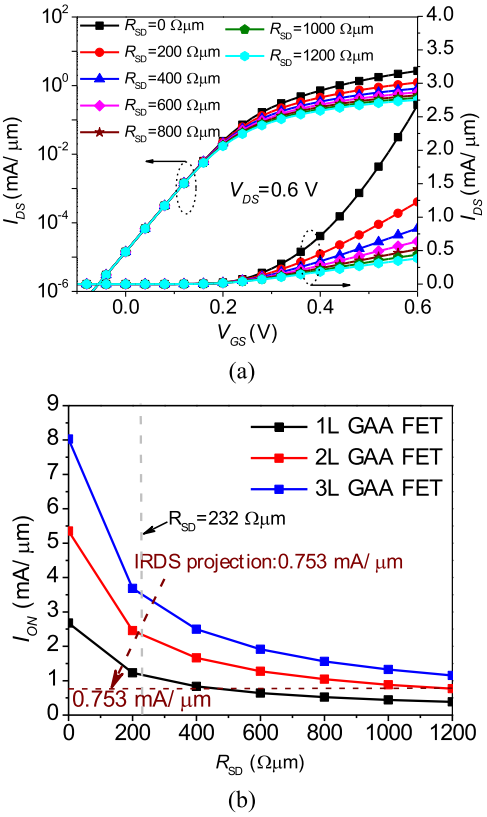

Fig. 6. (a) Impact of source and drain contact resistance on the transfer characteristics of the monolayer GAA-FET. (b) Impact of source and drain contact resistance on I_{ON} of the GAA 1L-FET, GAA 2L-FET, and GAA 3L-FET.

a Verilog-A (VA) model we developed previously [32] (see Appendix).

The effect of source and drain resistances on the transfer characteristics of the device is shown in Fig. 6(a), considering a GAA 1L FET with several R_{SD} (from 0 to 1200 $\Omega \cdot \mu$m, which includes IRDS requirement of $<232\ \Omega \cdot \mu$m at 1-nm node). It can be observed that the contact resistance significantly degrades I_{ON} of the device, which is consistent with the low I_{ON} for monolayer MoS_2 FET devices observed in experimental measurements. The adoption of multilayer 2-D nanosheet structures GAA-FET as shown in Fig. 6(b) can mitigate this problem. Indeed, we observe that also if we consider the scenario where the total contact resistance of the 3L structure is three times the one required by IRDS ($R_{DS} = 232\ \Omega \cdot \mu\text{m} \times 3$), the I_{ON} current ($\sim$1.8 mA/μm) is always 2.3 times higher than that projected by IRDS (0.753 mA/μm) and 1.5 times the one expected for 1L with $R_{DS} = 232\ \Omega \cdot \mu$m ($\sim$1.2 mA/$\mu$m).

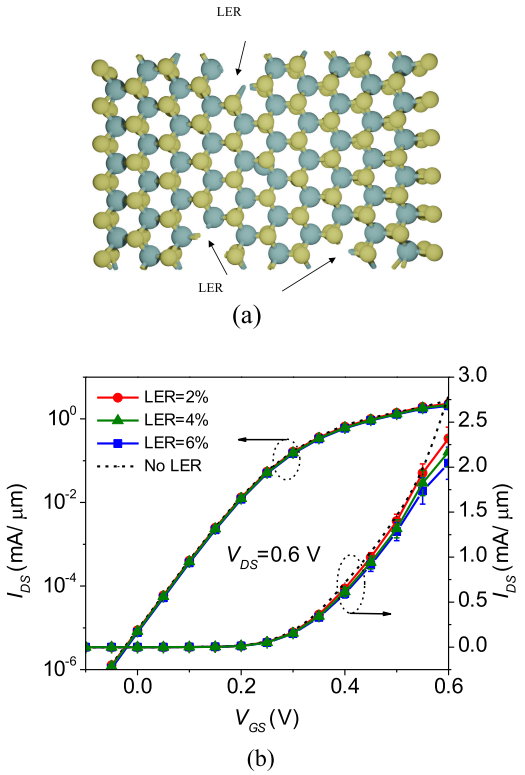

Fig. 7. (a) LER in MoS_2 channel. (b) Impact of LER on GAA-FET transfer characteristics.

TABLE II
COMPARISON OF PERFORMANCE PARAMETERS OF A 1L GAA-FET AND A 3L GAA-FET AFTER CONSIDERING NONIDEALITIES (CONTACT RESISTANCE $R_S = R_D = 500\ \Omega\ \mu$M AND LER 2%) AGAINST IRDS REQUIREMENT FOR THE 1-NM NODE IN 2031. WE HAVE CONSIDERED $V_{DD} = 0.6$ V AND $I_{OFF} = 10^{-5}$ mA/μM

Parameters	GAA 1L-FET	GAA 3L-FET	IRDS (1 nm node)
SS (mV/dec)	60	60	70
I_{ON} (mA/μm)	0.47	1.41	0.753

Line-edge roughness is another nonideal effect that leads to device variability and performance degradation. In the simulations, we have considered LER as an atomic defect as shown in Fig. 7(a). Fig. 7(b) compares the transfer characteristics of the GAA-FET with no LER and with LER of 2%, 4%, and 6%. To consider the variability of the devices, we have performed 20 sets of Monte Carlo simulations corresponding to 20 different channels with LER of 2%, 4%, and 6%. It can be observed that the LER reduces the ON-current of the device due to the reduction of the carriers contributing to the transport.

As a final analysis, we report in Table II, a comparison of the performance parameters *SS* and I_{ON} of GAA 1L-FET, GAA 3L-FET, after considering nonideal effects, with the IRDS requirement for high-performance devices at the 1-nm technology node [25]. In particular, for the GAA 1L-FET and GAA 3L-FET, we have considered a typical contact resistance of 500 $\Omega \cdot \mu$m, LER of 2%, and zero spacer length between source/drain and gate. It can be observed that the nonideal

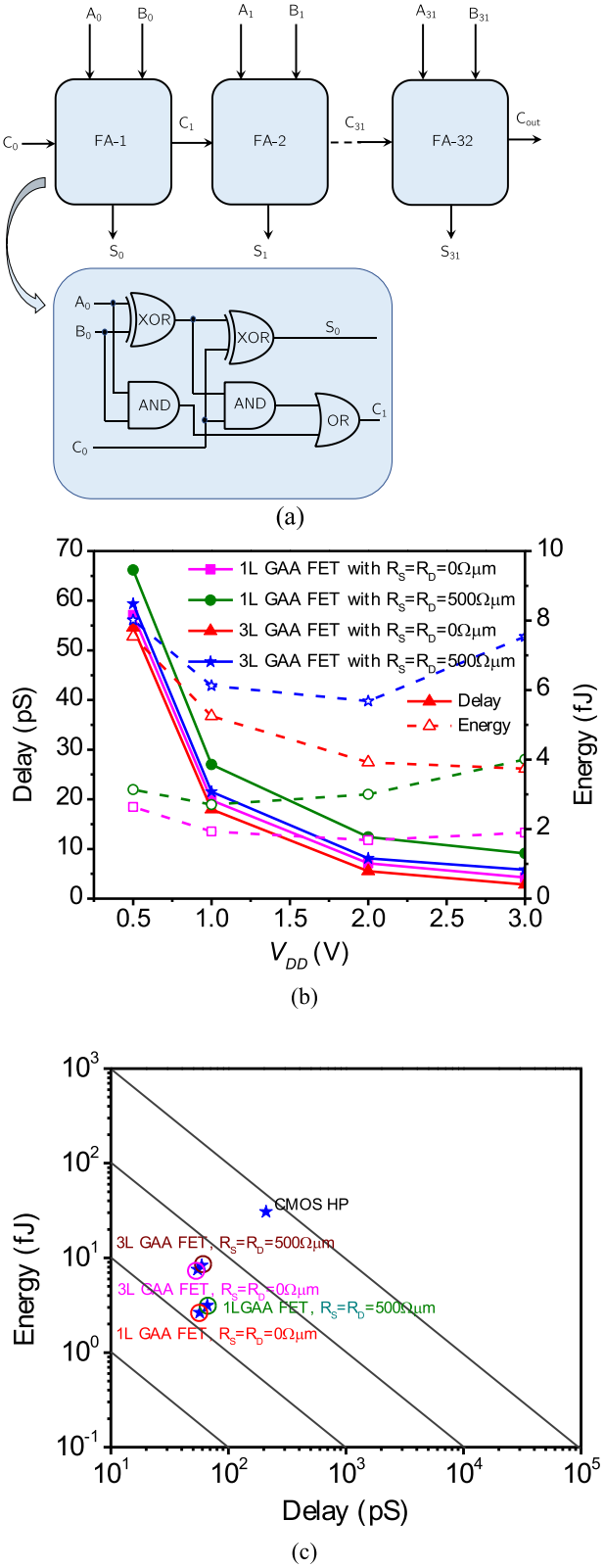

Fig. 8. (a) Schematic of 32-bit full adder circuit. (b) Energy per switching operation and delay of an NSFET-based 32-bit full adder circuit. (c) Comparison of energy and delay of the three NSFETs for $V_{DD} = 0.5$ V with state-of-the-art technologies presented in [32].

effects degrade the performance of the device and GAA 1L-FET, with the I_{ON} current of 0.47 mA/μm does not meet the IRDS requirement for the 1-nm technology node expected

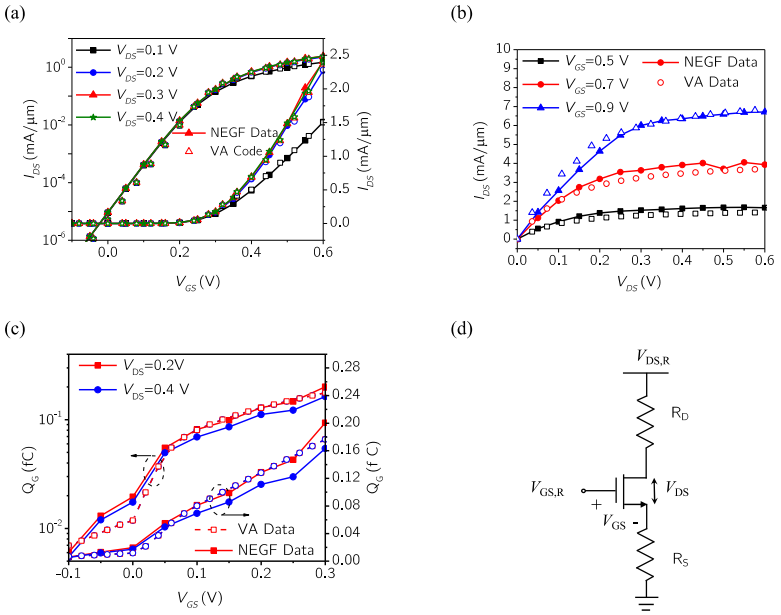

Fig. 9. Fitting of VA data with GAA 1L-NSFET characteristics. (a) Transfer characteristics. (b) Output characteristics. (c) Gate charge. (d) Schematic of GAA-FET with contact resistance.

in 2031 ($I_{\mathrm{ON}} = 0.753$ mA/μm). However, the vertical stacking of the channels improves the performance of the device, and the GAA 3L-FET, taking into account nonideal effects, shows the potential to meet and exceed the performance parameters as predicted by the IRDS [25]. In addition, it is worth noting that after accounting for nonideal effects, I_{ON} of 470 μA/μm using our ballistic transport approach is very close to the experimentally reported I_{ON} of 460 μA/μm, corresponding to a contact resistance of 500 $\Omega \cdot \mu$m in [31].

V. Circuit Performance Benchmarking

To demonstrate the potential of GAA-FET devices, we have evaluated the circuit performance of GAA-FETs by performing 32-bit full adder circuit simulations. For accurate transient simulations, we fit current–voltage and gate charge–voltage curves extracted from NEGF simulations with our in-house VA model [32], as shown in Appendix. In particular, we have calculated the energy and delay of a 32-bit full adder (FA) circuit shown in Fig. 8(a), considering symmetric p-GAA-FET and n-GAA-FET devices. Fig. 8(b) shows the worst case delay, t_d (i.e., the delay between the carry of the first stage and the sum of 32nd stage FA) measured at $0.5V_{\mathrm{DD}}$ with rising pulse and the energy consumption per switching [energy = average power $\times$ t_d/number of switching transitions at the S_{31} node in Fig. 8(a)] of a 32-bit FA circuit based on GAA-FETs, both without considering the source and drain contact resistances and with a source and drain contact resistance of 500 $\Omega \cdot \mu$m. It can be observed that the contact resistance increases the delay and thus the energy consumption per switching operation. In addition, the delay increases as the supply voltage decreases due to a decrease in the ON-current. The energy per switch first decreases with supply voltage and then begins to increase due to the large increase in delay at lower supply voltages.

The 3L GAA-FET has a higher power consumption compared to 1L GAA-FET devices due to an increase in the device ON-current. It should be noted that the contact resistance has a dominating effect on the ON-current and a negligible effect on the OFF-current [Fig. 6(a)]. The power consumption of the 3L GAA-FET with a contact resistance of 500 $\Omega \cdot \mu$m is the highest due to higher power consumption (higher I_{ON}) compared to 1L-GAA-FET and higher delay compared to 3L-GAA-FET with $R_{\mathrm{DS}} = 0\ \Omega \cdot \mu$m. Fig. 8(c) compares the energy and delay of the GAA-FET for $V_{\mathrm{DD}} = 0.6$ V with the IRDS [26] CMOS HP technology requirement at the 1-nm technology node. The energy and delay of a 32-bit full adder circuit based on an IRDS CMOS HP technology is calculated using the method presented in [33]. It can be observed that the performance of the investigated GAA-FETs meets the CMOS HP technology requirements in the energy–delay space projected by the IRDS at the 1-nm technology node.

VI. Conclusion

We have presented a full quantum simulation study of vertically stacked 2-D nanosheet FETs. The proposed method has allowed us to outline the device performance while considering different geometries in both ideal and nonideal cases. We have studied two different geometries for vertically stacked 2-D nanosheets, i.e., GAP and GAA, and have shown that the latter can improve the drive current without increasing the device footprint, while GAP, which is simpler from a fabrication point of view, does not. The results show that 2-D multilayer GAA-FETs can overcome the ON-current limitation typically encountered in 2-D monolayer-based devices when nonidealities such as contact resistance and LER are also taken into account. The results presented here indicate that 2D-based vertical nanosheet FETs can be a valuable alternative to Si-based nanosheet architectures, as 2DMs do not suffer from mobility degradation and quantum confinement effect, as typically happens in thin Si channels, and by themselves provide the best electrostatic control due to their (almost) atomic thickness. Finally, we benchmarked the circuit performance of

the device by calculating the energy per switching operation and the worst case delay of a 32-bit full adder circuit. The circuit performance shows that the GAA-FETs outperform CMOS high-performance technology in energy–delay space for a supply voltage of 0.6 V.

Appendix
Method to Study the Contact Resistance on the GAA-FET

The impact of contact resistance in GAA 1L-FET is studied by using a postprocessing methodology on GAA 1L-FET characteristics. First, we calculated the transfer and output characteristics of the device using numerical NEGF simulations. We fitted a Verilog-A model for 2D material FETs [31] with the numerically calculated transfer and output characteristics and gate charge as presented in Fig. 9(a)–(c), respectively. Furthermore, we used the Verilog-A model with extracted parameters to study the impact of contact resistance in the Cadence Virtuoso environment by connecting ohmic resistance at the source and drain terminal as presented in Fig. 9(d). The calculated results show that the contact resistance degrades the ON-current and speed of the circuit significantly as presented in Figs. 6 and 8.

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