On-Current Degradation in Ultra-Scaled Nanosheet FETs With S/D Underlap Doping

Lee-Chi Hung, *Student Member, IEEE*, Zlatan Stanojević, *Senior Member, IEEE*, Franz Schanovsky, *Member, IEEE*, Hans Kosina, *Member, IEEE*, and Markus Karner, *Member, IEEE*

***Abstract*— Aggressive gate pitch scaling makes it increasingly challenging to control the doping gradient at the source/drain (S/D) extensions. To address this, S/D underlap doping has been proposed as a solution. However, anomalous $I_{D,lin}$ saturation has been experimentally observed in such devices, raising questions about its physical origin. In this work, we investigate the transport physics in ultra-scaled nanosheet FETs by solving the Subband Boltzmann Transport Equation. The simulation results reveal that secondary barriers formed in underdoped S/D extensions enhance quasi-ballistic transport even in the linear regime, providing a consistent explanation for the observed $I_{D,lin}$ saturation in underlap devices. These insights offer guidance for optimizing S/D underlap doping profiles, highlighting the need to avoid excessive Gate-S/D overlap capacitance while preventing on-current degradation.**

***Index Terms*— TCAD, subband Boltzmann transport, S/D underlap doping, nanosheet, ultra-scaled CMOS devices.**

I. Introduction

DUE to their superior electrostatic control, nanosheet FETs (NSFETs) have been demonstrated to meet the scaling demands of advanced technology nodes [1], [2], [3]. However, as gate pitch scales aggressively, the physical spacer length is reduced, making it increasingly difficult to engineer the source/drain (S/D) extension doping gradient with high precision. This limitation results in excessive S/D overlap, which can significantly degrade the subthreshold swing (SS) due to enhanced short-channel effects (SCEs). To address these challenges, a S/D underlap doping profile combined with an undoped channel has been proposed [4], [5], [6], [7]. This configuration offers several benefits: it suppresses leakage current by relaxing S/D electrostatic coupling, preserves channel mobility by minimizing impurity scattering, and reduces process-induced variability such as random dopant fluctuations.

While previous simulation studies [4], [5], [6], [7], [8], [9] have already evaluated the role of S/D doping profiles on device performance, they relied on drift-diffusion (DD) based solvers, which assume carriers are in local equilibrium. This assumption breaks down in ultra-scaled devices, where non-equilibrium effects such as ballistic transport and velocity overshoot become increasingly significant [10]. Moreover, in DD-based simulations, the extensions are effectively represented as lumped series resistances determined by doping concentration, neglecting the carrier injection mechanisms that govern transport in these regions. Notably, measurements on underlap devices [11], [12] have shown an anomalous saturation in $I_{D,lin}$, which a constant parasitic resistance model cannot fully explain.

In this letter, we investigate the ultra-scaled underlap NSFETs by solving the Subband Boltzmann Transport Equation (SBTE). Our results reveal that the observed current degradation arises from an amplification of ballistic effect by the peculiar electrostatics of these underlap devices. These findings offer new physical insights for optimizing the design of S/D underlap doping profile in future technology nodes.

II. Methodology

Fig. 1(a) illustrates the 3D n-NSFET structure analyzed in this study. The gate is separated from the S/D epitaxial regions by extensions, which are enclosed by nitride spacers. The different S/D doping profiles along the channel direction are modeled using an error function, characterized by a proximity parameter z_0 and an abruptness parameter σ. Here, $z_0 = 0$ nm marks the extension/epitaxy interface and increases toward the S/D epitaxial regions, while σ corresponds to the standard deviation of the underlying Gaussian distribution before integration, as shown in Fig. 1(c). Although the inclusion of contact resistance slightly alters the charge balance, its impact has been experimentally minimized as reported in [11] and [12]. Therefore, in this work we assume ideal Ohmic contacts to isolate the intrinsic transport effects in ultra-scaled devices. Device simulations are performed globally in 3D using the GTS Nano Device Simulator (NDS) [13], with the entire nanosheet treated as SBTE domain. All relevant scattering processes, including Coulomb scattering, acoustic phonon

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Lee-Chi Hung is with Global TCAD Solutions GmbH, 1010 Vienna, Austria, and also with the Institute for Microelectronics, TU Wien, 1040 Vienna, Austria (e-mail: r.hung@globaltcad.com).

Zlatan Stanojević, Franz Schanovsky, and Markus Karner are with Global TCAD Solutions GmbH, 1010 Vienna, Austria.

Hans Kosina is with the Institute for Microelectronics, Vienna University of Technology, 1040 Vienna, Austria.

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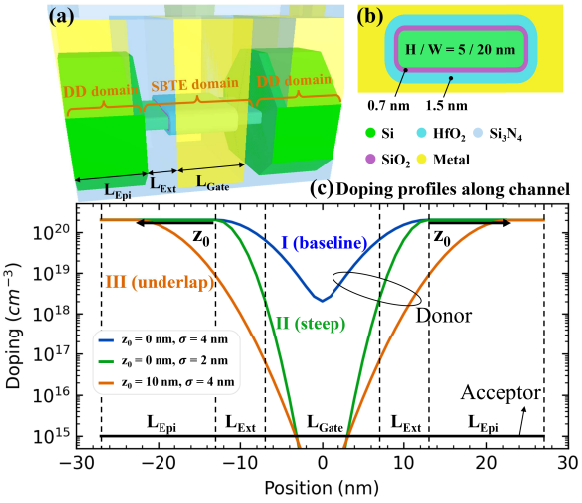

Fig. 1. (a) 3D design of the n-NSFET structure, (b) 2D cross-section at the center of the channel, and (c) three corresponding S/D doping profiles with different doping proximity z_0 and abruptness σ.

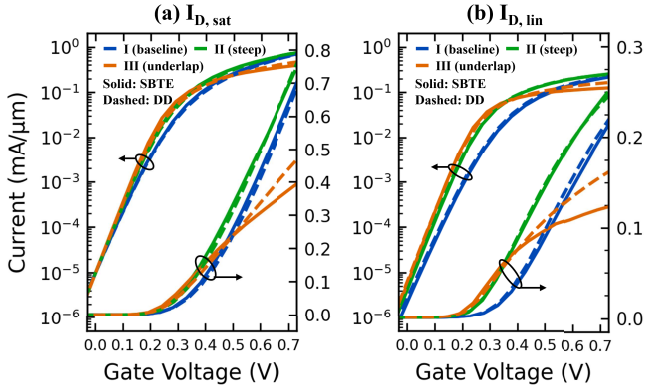

Fig. 2. (a) Saturation (V_{ds} = 0.7 V) and (b) linear (V_{ds} = 0.05 V) transfer characteristics of n-NSFETs obtained from SBTE and DD simulations with varying doping profiles, as shown in Fig. 1. The current is normalized by the effective channel width, 2(H + W) = 50 nm. The gate workfunction of each device is adjusted to align the off-state current $I_{D,sat}$ to 10 nA/μm at V_{gs} = 0 V.

scattering, inter-valley scattering, and surface roughness scattering, have been precisely calibrated against experimental data from [14] and [15]. This simulator has consistently been shown to accurately reflect experimental results, as validated in [10], [16], and [17].

III. Results and Discussion

Fig. 2 presents the transfer characteristics from SBTE simulations for three different S/D doping profiles: I (baseline) with σ = 4 nm, z_0 = 0 nm; II (steep) with σ = 2 nm; and III (underlap) with σ = 4 nm, z_0 = 10 nm, as illustrated in Fig. 1. Comparing the currents of Profiles I and II, or I and III, we observe that either a steeper σ or a larger z_0 helps suppress SCEs by reducing electrostatic coupling between the S/D and the channel, thus improving the SS. However, Profile III with its larger z_0, exhibits notable on-current degradation in both $I_{D,sat}$ and $I_{D,lin}$, with the latter showing a distinct saturation behavior. In addition, we performed calibrated DD simulations [17], replacing SBTE domain for comparison. While the calibrated DD accurately reproduces the current characteristics

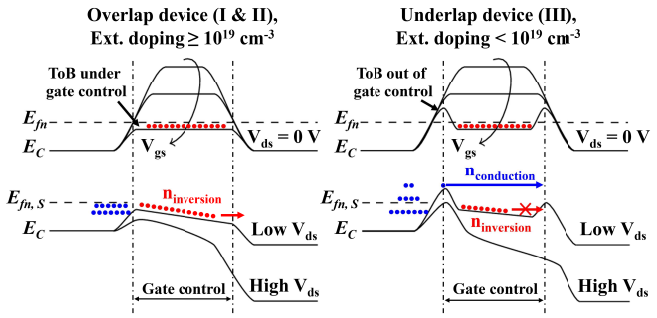

Fig. 3. Electrostatic potential profiles of (left) overlap and (right) underlap devices, illustrating the impact of device doping under operating bias.

of Profiles I and II, it fails to capture the observed anomalous current degradation in the underlap device (Profile III) regardless of the parameter choice. The discrepancy between SBTE and DD becomes increasingly pronounced with higher gate bias in this device.

To understand the root cause of the anomalous performance degradation in Profile III, we first compare the electrostatic potential profile of an overlap device with conventionally doped S/D extensions ($\geq 10^{19}$ cm^{-3}, as in Profiles I and II) and an underlap device with underdoped extensions ($< 10^{19}$ cm^{-3}, as in Profile III). This threshold was empirically identified based on the observed saturation behavior in $I_{D,lin}$. Fig. 3 illustrates the electrostatic potential profiles of these devices under modulation of V_{gs} and V_{ds}. As the overlap device gradually turns on, the top-of-the-barrier (ToB) remains under gate control. For both low and high V_{ds}, the source extension ensures sufficient carrier injection into the gate-controlled region. Consequently, the on-state current increases linearly with V_{gs}, as the inversion carrier population not only shapes the channel electrostatics but also directly facilitates the carrier conduction (i.e., $n_{inversion}$ = $n_{conduction}$). In contrast, as the underlap device turns on, the gate lowers the electrostatic potential in the channel relative to the underdoped extensions, forming secondary ToBs in these regions. The reduced carrier density in these regions already adds series resistance in the S/D path of the device in the linear regime. In saturation regime, V_{ds} lowers the secondary barriers and partially restores the gate control over $I_{D,sat}$, but the remaining source barrier still causes a proportional degradation of the current. However, to complete the picture, ballisticity must be considered. Our SBTE simulations estimate a mean free path (MFP) of approximately 10 nm in this system. Momentum randomization and energy relaxation requires multiple scattering events; since the gate length of the studied device is only 14 nm, comparable to a single MFP, the transport can be considered quasi-ballistic. This leads to a split of the carrier population into the immobile $n_{inversion}$ which governs the channel electrostatics and the mobile $n_{conduction}$ that contributes to the current. Such a split causes a loss of gate control and the onset of $I_{D,lin}$ saturation.

To quantitatively confirm this hypothesis, we analyze the carrier and current spectra extracted from the SBTE solutions for devices with Profiles II and III, as shown in Fig. 4. For Profile II, Fig. 4(a) and Fig. 4(b) show that the current spectrum closely follows the band edge where $n_{inversion}$ peaks, indicating that the ToB remains under gate control and the on-current

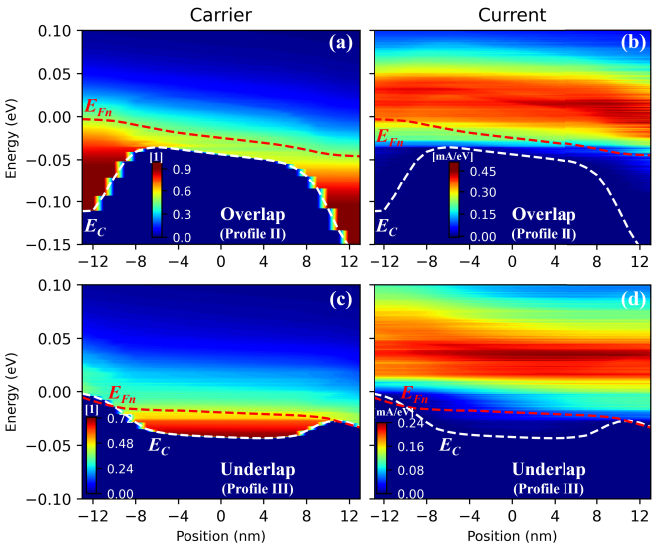

Fig. 4. (a, c) Carrier and (b, d) current spectra along the channel, extracted at V_{gs} = 0.7 V and V_{ds} = 0.05 V. The effective ground-state energy (white) and electron quasi-Fermi energy (red) are indicated by dashed lines in each figure. While (a, b) show that the current spectrum follows the band edge where $n_{inversion}$ peaks, (c, d) illustrate that $n_{inversion}$ no longer contributes to carrier conduction.

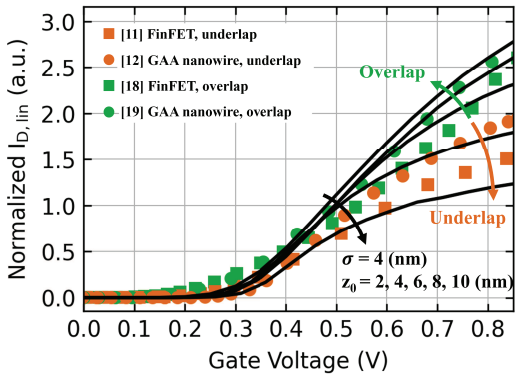

Fig. 5. Linear transfer characteristics of (lines) n-NSFETs with varying z_0, showing consistent trends with experimentally measured (symbols) underlap [11], [12] and overlap [18], [19] devices. The currents have been normalized individually and aligned around V_{th} = 0.3 V to exclude the influence of mobility, gate capacitance, and device dimensions.

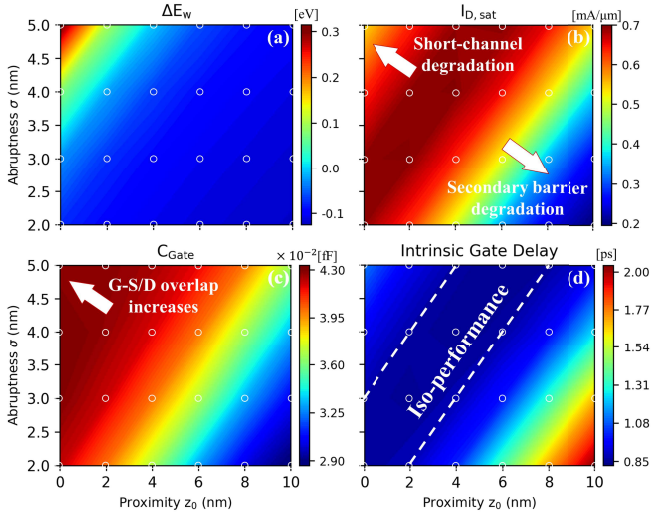

Fig. 6. Simulated performance metrics as a function of σ and z_0: (a) gate metal workfunction (E_w) shift (b) $I_{D,sat}$ (c) C_{Gate} (d) intrinsic gate delay. A baseline E_w = 4.4 eV is slightly adjusted to align the off-state current to $I_{D,sat}$ = 10 nA/μm at V_{gs} = 0 V. Panels (b–d) are extracted at V_{gs} = V_{dd} = 0.7 V. Each white circle denotes a simulated point in the parameter space.

is carried by the same population of carriers contributing to the channel charge (i.e., $n_{inversion}$ = $n_{conduction}$). In contrast, Fig. 4(c) shows that for Profile III, $n_{inversion}$ is confined within the potential well formed by the S/D extension barriers which is approximately 1–2 k_BT higher than the gate-controlled region due to the insufficient doping. Although $n_{inversion}$ can still be modulated by the gate bias, the current spectrum in Fig. 4(d) reveals that it does not contribute to carrier conduction. Instead, $I_{D,lin}$ is dominated by the quasi-ballistic transport of $n_{conduction}$. This decoupling between $n_{inversion}$ and $n_{conduction}$ leads to a loss of gate control over the $I_{D,lin}$, which explains the saturation behavior observed in Fig. 2(b). This non-local effect is accurately captured by the SBTE solution, which provides the non-equilibrium carrier distribution along the channel rather than assuming a near-equilibrium distribution at every position as the conventional DD approach inherently assumes, which overestimates the current in such device.

Fig. 5 provides experimental evidence for $I_{D,lin}$ saturation in underlap devices. The SBTE simulations with varying z_0 are compared against experimental data from ultra-scaled (L_{gate} < 15 nm) FinFETs [11], [18] and GAA nanowire transistors [12], [19]. For underlap devices, simulations with larger z_0 consistently reproduce the anomalous saturation, which originates from secondary barrier formation and the resulting non-equilibrium transport in linear regime. In contrast, overlap devices show a linear increase of $I_{D,lin}$ with V_{gs}, matching simulations with small z_0.

The simulation results in Fig. 5 raise an important question: how can the underlap doping profile be optimized to balance S/D separation with on-current performance? To address this, we provide a design guideline for selecting S/D doping profiles by minimizing the intrinsic gate delay, defined as $C_{Gate}{\cdot}V_{dd}/I_{D,sat}$, as shown in Fig. 6(d). Within the iso-performance scaling band, σ and z_0 need to be co-optimized to avoid the increase of Gate-S/D overlap capacitance (upper-left corner) and the on-current degradation (bottom-right corner) caused by secondary barriers at S/D extensions.

IV. Conclusion

In summary, this work investigates the on-current performance of ultra-scaled underlap NSFETs with varying doping abruptness σ and proximity z_0. Our results show that underdoped S/D extensions degrade the on-current due to the formation of secondary barriers beyond the gate's control. These barriers enhance non-equilibrium transport even in the linear regime, leading to the experimentally observed $I_{D,lin}$ saturation. Notably, since DD-based simulations fail to capture this effect, it may have been previously misattributed to parasitic contact resistance. Finally, we establish an iso-performance scaling path that co-optimizes σ and z_0 to avoid excessive Gate-S/D overlap capacitance and to mitigate the on-current degradation induced by S/D extension barriers.

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