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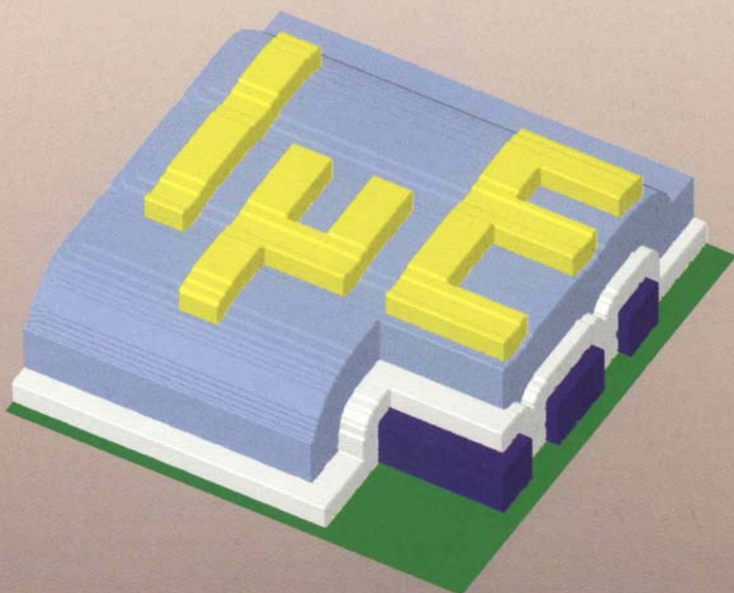

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Preface

Erasmus Langer and Siegfried Selberherr

This brochure is the twelvth annual research review of the Institute for Microelectronics. The staff, financed by the Austrian Federal Ministry of Education, Science, and Culture consists of nine full-time employees: the dean of the Faculty of Electrical Engineering and Information Technology, the head of the institute, one additional professor, three scientists, a secretary, and two technical assistants. Seventeen additional scientists are funded through scientific projects supported by our industrial partners, by the Austrian Science Fund (FWF), and by the EC Framework Programme.

This year we are glad to report participation in two new projects within the "Information Society Technology Programme (IST)" which are directly funded by the European Community, namely MAGIC-FEAT ("Meshes and Global Integration for Semiconductor Front-End Simulation") and NANOTCAD ("Nanotechnology Computer Aided Design"). We proudly report that most of our industrial partners have continued the cooperation. In addition we succeeded in starting new cooperative research with TOSHIBA, Kawasaki, Japan.

Despite the drastic lowering of the public budget accompanied by announcements of the government concerning a further more extensive reform of the universities we will not lose our motivation and will be entering the next year of our institute with considerable expectations.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the 'Technische Universität Wien' in 1980, he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik'. In 1986 he received his doctoral degree and in 1988 he joined the 'Institut für Mikroelektronik'. In 1997 he received the 'venia docendi' on 'Microelectronics'. Since 1999 Dr. Langer has been head of the 'Institut für Mikroelektronik'. His current research topic is the simulation of microstructures using High Performance Computing paradigms.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the 'Technische Universität Wien' in 1978 and 1981, respectively. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. Since 1988 he has been the head of the 'Institut für Mikroelektronik' and since 1999 he has been dean of the 'Fakultät für Elektrotechnik'. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all the technical hardware and software work of the institute.

Multi-Dimensional Modeling and Simulation of Dopant Diffusion

Tesfaye Ayalew

Within the past decade process simulation has become an essential part of new technology development in the silicon IC industry. The use of TCAD (Technology CAD) tools has been driven by the enormous cost of purely experimental approaches to technology development. Yet the power of these tools and their predictive capability are limited by the model they use. One of the limitations requiring improved models is the redistribution of dopant atoms, which determine the electrical characteristics of the final device structure.

As devices continue to get smaller, better models will certainly be required. Challenges for the future include more detailed information about damage resulting from ion implantation, better understanding of point defect properties such as equilibrium populations, diffusivities, and transient response to temperature changes, better models for point defect behavior at interfaces, and finally development of accurate methods to actually measure two- and three-dimensional dopant profiles.

Since many profiles are box-shaped, dopant diffusion in silicon often requires three-dimensional investigation of problems. One tool that makes model development substantially simpler is the recently developed general purpose partial differential equation (PDE) solver AMIGOS (Analytical Model Interface and General Object Oriented Solver), which can easily implement models of diffusion. It has been recognized for a long time

that such a simulator could be very useful for investigating the detailed physics of the reactions involved between dopants and defects. Much of the effort in modeling dopant diffusion has focused on ion implantation and damage annealing because of the great industrial importance of these processes.

For being able to cope with these different requirements the simulator AMIGOS will be extended. It is a problem-independent simulation system which can handle PDEs in time and space or in either of the two, for two or three dimensions. A significant opportunity for the future is to greatly expand this simulator in order to include multigrid methods for solving PDEs to help in the development of diffusion processing. Efforts are being made to study point defects and dopant diffusion processes, to understand and model transient enhanced diffusion (TED) and to estimate model parameter values.

Tesfaye Ayalew was born in Addis Ababa, Ethiopia in 1966. He earned his BSc degree in Electrical Engineering from Addis Ababa University in 1990. Then he served for five years at the Medical Equipment Engineering Service in Ethiopia. In 1995 he joined the Institute for Biomedical Engineering, University of Vienna, where he carried out a one year research work on functional electrostimulation. In the same year he was accepted by the 'Technische Universität Wien' where he studied Electrical Control and Computer Engineering and received the degree of 'Diplomingenieur' in March 2000. He joined the 'Institut für Mikroelektronik' in May 2000, where he is currently a PhD candidate in the field of TCAD. His research interest is focused on multi-dimensional modeling and simulation of dopant diffusion.

Genetic Optimization Methods for TCAD Analysis Tasks

Thomas Binder

In a conventional gradient-based optimization method the optimizer tries to find the dependence from each of the parameters by numerically computing the Jacobian and Hessian matrices of the system. Based on these computations a direction and step width is chosen. This method offers an efficient way of finding a local minimum. However, the found optimum strongly depends on the initial guess used. Several optimization runs with different starting values may be necessary in order to find an acceptable solution.

The cheap computing power available with a modern cluster of workstations allows for completely new ways of performing TCAD analysis tasks. A very promising approach is the use of a genetic algorithm. Although the number of evaluations is usually higher compared to gradient-based optimizers, there is no need to supply an initial guess. Instead, the algorithm randomly chooses parameter values within the allowed bounds. These parameter bounds need not be as conservative as in the gradient-based case. Instead of breaking the computation of the Jacobian matrix, a failed evaluation simply does not evolve into the next generation. As a direct consequence less human interaction with the whole system is necessary. Additionally, the execution time for the whole optimization does not depend as strongly on the number of parameters as in gradient-based methods. By selecting an appropriate genetic optimization strategy the total number of evaluations can be minimized.

In a genetic algorithm several strategies for evolving a certain population are possible. The optimizer implemented (galib) in the TCAD framework SIESTA supports the following strategies: `simple`, `steadystate`, `incremental`, and `deme`. They mostly differ in the way individuals are selected for mating and in the number of individuals surviving into the next generation. The user may tune several optimization parameters, among which the mutation and the crossover probabilities are the most important ones. The parameter `crossover` accounts for generating new individuals based on existing ones, and `mutation` randomly flips a parameter of an individual. One can think of `mutation` as a way of escaping from a local minima, whereas `crossover` tries to refine two fit individuals to form a better one. Three crossover methods are supported. With one point crossover, the algorithm splits the parameter set at a randomly chosen point into two parts and takes one half from each parent to produce an offspring. In the case of two point crossover, two points are chosen randomly. For uniform crossover, each parameter is taken from a randomly chosen parent.

Thomas Binder was born in Bad Ischl, Austria, in 1969. He studied electrical engineering and computer science at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in December 1996. During his studies he was working on several software projects mainly in the CAD, geodesy and security fields. In March 1997 he joined the 'Institut für Mikroelektronik', where he is currently working on his doctoral degree. In autumn 1998 he held a visiting research position at Sony, Atsugi, Japan. His scientific interests include data modeling, algorithms, software engineering and semiconductor technology in general.

Grid Generation for Three-Dimensional Device Simulation

Johann Cervenka

In device simulation the use of a suitable mesh generator is a crucial part which influences the whole simulation process. The placement of the grid points significantly effects the solution. Badly fitted grids cause inaccurate results; therefore, the need to refine the grid is obvious, but this boosts the amount of grid points and grid elements and might cause intolerable calculation times and memory consumption. Particularly in three-dimensional device simulations the calculation times reach the tolerable limits, and therefore the amount of grid points should be minimized.

Ortho product grids are easy to assemble, but with the complex device structures and nonplanar device surfaces used nowadays, this method will produce a waste of unwanted grid points. A tetrahedral mesh is not limited by geometry, but the control of grid density is more complicated. Refining a tetrahedral grid results in nearly equilateral tetrahedra. In a MOS transistor the channel under the polysilicon gate requires a high grid density from the surface inwards to the device, whereas a more coarse point density can be tolerated parallel to the channel surface.

A generated grid should combine the benefits of these two methods. Thus, a special procedure is chosen. The simulation domain is treated as a resistor, placed in vacuum, with two electrodes at top and bottom, where a voltage is applied.

After solving the Laplace equation, which describes the electrostatic potential, grid points in the inner part of the resistor are placed at the intersections of selected equipotential lines and field lines. The spacing between the selected equipotential and field lines can be varied independently. The cells surrounded by equipotential lines and field lines are approximately cuboidal in shape and the grid is conforming to the surfaces. For the following device simulation the set of grid points has to be tetrahedrized.

For an efficient implementation of this method special emphasis must be put upon a robust equation solver for the Laplace equation and on a stable mesh generator for the initial grid and the final mesh. Because of the sparse occupation of the matrices of the resulting equation system for solving the field equation, an iterative method, such as a conjugate gradient solver with preconditioning, is a good choice. For building the grids the three-dimensional mesher DELINK, also developed at the institute, is chosen.

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Simulation of Ferroelectric Nonvolatile Memory Cells

Klaus Dragosits

A promising approach to increase the capabilities of integrated-circuit nonvolatile memory is to take advantage of the polarization hysteresis of ferroelectric materials. For a rigorous analysis of these devices a suitable model for the simulation of two-dimensional hysteresis effects is necessary. Such a model has been developed and implemented into the device simulator MINIMOS-NT.

The simulation of the two-dimensional hysteresis curve leads to the nontrivial problem of field rotation and forces the calculation of parameters for the nonlinear locus curve at each grid point. To allow the calculation of transfer characteristics the algorithm has to be insensitive to the magnitude of the applied voltage. For a general approach to two-dimensional hysteretic effects an inhomogeneous field distribution has to be assumed. This prevents the use of a simple one-dimensional hysteresis model using the same locus curve for the entire ferroelectric region. Two different locus curves must be calculated for each grid point. Depending on the simulated ferroelectric material, different shape functions of the locus curve may be applied. These are *arctan* functions for SBT ($SrBi_2Ta_2O_9$) and *tanh* functions for PZT($Pb(Zr,Ti)0_3$). The *tanh* function allows an analytic calculation of the parameters of the locus curves. The *arctan* function parameters are derived by a Newton method.

Similarly to magnetic properties the rotation of a constant magnetic field causes a lag angle χ of the induction. The simple approach of first decreasing the electric field to zero, then increasing it to the value of the next operating point and finally adding the two polarization components derived is not feasible, as it is inconsistent with the one-dimensional hysteretic properties. Additionally, the results strongly depend on the distance between the calculated operating points. Thus we assume a straight trajectory between the vectors of the old and the newly applied electric field. This also assures a proper numerical behavior for larger applied voltage steps. The basic principle of the applied algorithm is to split the polarization and electric field of the previous operating point into components parallel and orthogonal to the next electric field. These curves yield the polarization in direction of the electric field and the remanent polarization in the orthogonal direction, thus forming a primary guess for the next polarization. The scalar values of the two components are added and compared to the maximum polarization at the given magnitude of the electric field, forming an upper limit for the available number of switching electric dipoles. Due to the vanishing electric field in the normal direction the orthogonal component is reduced appropriately with respect to this limit.

Klaus Dragosits was born in Bruck an der Mur, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. He joined the 'Institut für Mikroelektronik' in September 1997, where he is currently working on his doctoral degree. He held visiting research positions at Philips Research, Eindhoven, in March 2000 and at the Samsung Avanced Institut of Technology, Seoul, in June 2000. His scientific interests include device simulation with special emphasis on nonvolatile memory cells and high-k dielectrics.

Mesh Generation, Software Engineering, and CAD

Peter Fleischmann

Three-dimensional mesh generation naturally deals with complex geometries stored in large data files. While in theory the mesh generation process should be invisible to the user of the simulation software and a batch mode should be a sufficient user interface, in practice a more effective interface to handle such large data files is required. Besides the visualization of the simulation result, further interaction during several stages of the simulation is important for problem-backtracing and for developers. Therefore it was eminent to couple a CAD editor with the mesh generator DELINK. For several reasons the simple, surface-based public domain CAD editor AC3D was chosen and the data flow was implemented both to and from the editor. This allows the efficient examination of faulty TCAD geometries arising from semiconductor process simulation and more importantly, a manual repair when needed.

This editor was also used to construct further test structures for the mesh generator DELINK, which is still under development. Among those is a complex CMOS structure as an important key example for mesh generation in TCAD applications. Furthermore, interconnect test structures were generated which could not be described with the purely layered data format of the interconnect simulation package Smart Analysis Program (SAP). Also for this application an additional data flow had to be implemented in order to allow the coupling of SAP and DELINK, especially where boundary conditions required a

careful treatment. Among the test structures is one consisting of several conductors of triangular cross-section, crossing each other in every possible way un-aligned with the coordinate system.

Other applications where DELINK is required to provide meshing services are in the field of process simulation data management by an advanced wafer-state server and for the meshing extensions for semiconductor device simulation. For both applications DELINK's library functionality is used through the implemented application programmer interface. This API had to be extended in order to be able to provide some of the new functionality of DELINK. Most importantly, this includes the possibility of marking certain polygons or triangles of the input surface description (face marker) which are then preserved during all the local transformation steps during the mesh generation process, and which can then be consequently recognized in the output mesh. This new feature allows for example surface-based contacts where previously volumetric contacts were necessary in order to apply certain boundary conditions. This is especially important for the meshing extensions for device simulation where the device needs to be patched with two contacts in a pre-processing step.

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Analysis and Optimization of Memory Cell Structures

Andreas Gehring

With increasing device density and decreasing minimum feature size, conventional MOS transistor shrinking techniques encounter massive difficulties. In order to be in compliance with the National Semiconductor Roadmap, MOSFET channel lengths will have to be further reduced to 100nm until the year 2005. Under such circumstances, short-channel effects like DIBL (Dain-Induced Barrier Lowering), punchthrough or hot carrier oxide degradation have to be taken into account for the design of new memory cells. Considerable effort has already been spent on the optimization of MOSFET structures, emphasizing the importance of the doping profile in the channel region. However, for the proper evaluation of memory cells, the complete structure has to be taken into account. Three main optimization goals can be identified: high switching speed, low chip size and low power consumption.

These optimization parameters are directly connected to the partial capacitances of the cell. We developed a procedure for finding the total small-signal capacitance of arbitrary three-dimensional pn-junction geometries using the well-established two-dimensional device simulator MINIMOS. The interconnect capacitances can be taken into account by interconnect simulations with SCAP (Smart Capacitance Analysis Program). These values are then integrated into lumped models for circuit simulations.

In order to minimize the power consumption and maximize the retention time of memory cells, it is important to keep the leakage current through the channel region of the turned-off select transistors as low as possible. Easy ways to do so would be to decrease the gate together with the bulk voltage. However, effects like GIDL (Gate Induced Drain Leakage) may cause increasing leakage currents. A proper minimum can only be found by simulation approaches.

Such optimization procedures are important for the field of memory devices. For example, in state-of-the-art DRAM trench cells, a device area of $8F^2$ has become the lower bound, with F being the minimum feature size. This restriction can only be overcome by using different cell structures. One possibility is to switch the channel region into the vertical direction, thus achieving a considerable reduction of the cell's footprint independently of the channel length. However, there are some major differences in the channel behavior of such vertical devices. Crucial device parameters depend on the crystallographic orientation of the channel region. By means of device simulation, such effects will be identified and investigated.

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A Global Self-Heating Model for Device Simulation

Tibor Grasser

Due to the ever increasing packaging density of integrated circuits, self-heating and thermal coupling effects are getting more and more important. In order to account for self-heating effects, normally the lattice heat flow equation is solved. This alters the device performance by inclusion of thermal diffusion currents and by the temperature dependence of the physical parameters, such as band edge energies, recombination rates, and mobilities. However, this approach is problematic for several reasons. First, the heat spreading volume is normally much larger than the electrically active area and may extend to several 100 μm^3. Second, thermal effects are normally three-dimensional effects which cannot easily be approximated by two-dimensional cross-sections, as it is the case for purely electrical problems. In addition, two-dimensional thermal boundary conditions are difficult to formulate, due to two reasons: the Neumann boundary condition in the third dimension for the heat flux equation causes an overestimation of the temperature. Second, thermal boundary conditions are determined by the thermal resistors at material transitions as much as by the bulk properties. Unfortunately, these thermal resistors are normally not known.

In order to overcome these problems we make use of the observation that temperature distribution inside the devices is mainly controlled by thermal contact models. This is due to the fact that the thermally active region is truncated to the

electrically active region and that the outside region has to be approximated by some thermal contact resistances. If the thermal boundaries are modeled by an isothermal contact model without knowledge of the exact contact temperature, the resulting temperature distribution will be completely unrealistic.

Given the strong dependence on the boundary conditions, we approximate the distributed device temperature to a first order by a spatially constant value. Focusing on the terminal quantities, we now use a global self-heating model instead of the standard lattice heat flow equation to calculate the dissipated power as the Ohmic power dissipated at the contacts. The spatially constant lattice temperature is modeled as $T_L = T_\mathrm{C} + P \cdot R_g$ with R_g being the global thermal resistance.

This model is most useful for mixed-mode device simulations where thermal-coupling effects dramatically increase the complexity of the problem. Using this approximation the problem can be solved in considerably less time with reasonably accurate inclusion of thermal effects as has been verified by comparison to measurements for even sophisticated devices. The benefits provided by this approach can even be better exploited in three-dimensional device simulations as there the reduction in the number of unknowns is obviously even more significant.

Tibor Grasser was born in Vienna, Austria, in 1970. He studied communications engineering at the 'Technische Universität Wien', where he received the 'Diplomingenieur' and the Ph.D. degrees in 1995 and 1999, respectively. He joined the 'Institut für Mikroelektronik' in April 1996. His current scientific interests include circuit and device simulation, device modeling and physical aspects in general.

Higher Order Moments Transport Model for Device Simulation

Markus Gritsch

Due to decreasing device geometries non-local effects are gaining more and more importance. The well established drift-diffusion model (DD) can be derived from BOLTZMANN's transport equation using its first two moments. In conjunction with the POISSON equation one gets a closed set of partial differential equations. In order to solve this system it is necessary to discretize the equations onto an appropriate grid. Such a system cannot be solved explicitly, and the solution must be calculated by means of numeric methods. The simulation domain usually consists of a large number of subdomains, in which the solution can be approximated by algebraic equations. The unknown functions are approximated by functions with a given structure. In that way one obtains a fairly large system of, in general nonlinear, algebraic equations. After solving this system the distributed quantities potential ψ, electron concentration n and hole concentration p are obtained.

However, the DD model does not take non-local effects into account. In order to overcome these limitations the hydrodynamic transport model (HD) has been proposed, which considers the first three moments of BOLTZMANN's equation. Using four moments and neglecting the convective terms in the HD model leads to the energy-transport model (ET), which is well accepted nowadays. In addition to the quantities obtained with the DD model, the ET model gives information about the distributed carrier temperatures T_n and T_p.

Although non-local effects are governed by the HD and ET equations, some problems have been reported. Among those are the spurious velocity overshoot and problems arising from modeling the impact ionization coefficient simply as a function of the mean carrier energy which often leads to an overestimation of the effect.

An extension of the ET equations by also taking the next two moments into account results in a six moments model (SM). With the additional information provided by the new solution variables for electrons and holes β_n and β_p,referred to as kurtosis, it is possible to refine the physical models. For example for the calculation of the impact ionization coefficients the kurtosis can be used to provide a more realistic input for a standard ET impact ionization model.

Another topic currently being worked on is the behavior of floating-body devices, especially Silicon On Insulator (SOI) transistors. These devices are difficult to simulate because the floating region, since it is not connected to any contact, is the cause of numerically critical situations which can lead to wrong simulation results.

Markus Gritsch was born in Zams, Austria, in 1974. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in May 1999, where he is currently working on his doctoral degree. His scientific interests include circuit and device simulation, device modeling and physical aspects in general.

Inductance Calculation in Interconnect Structures

Christian Harlander

For a long time the speed of integrated circuits was largely determined by the switching speed of the individual transistors. The characteristics of the signal transfer from one device to the next were negligible. As switching times were accelerated, interconnect characteristics became critical and required accurate chip layout and system design for reducing the transfer delay.

With increasing packaging density and rising signal frequency inductance effects in interconnect structures gain importance for the electrical behavior of circuits. Reflections, cross talk and simultaneous switching noise increase delays or may cause logical faults and therefore must be minimized by careful design. Cross talk is a result of capacitive and inductive coupling between neighboring lines. It increases as the lines get closer and the distances they neighbor each other get longer.

The package SAP (Smart Analysis Programs) has been extended to perform the extraction of inductances. Our three-dimensional simulation tool uses the finite element method to solve the Laplace equation for domains of conducting materials. Using the derivative of the electrostatic potential the distribution of the electric current density is obtained by applying Ohm's law. The current density is used for the computation of the magnetostatic energy. Thereby, tetrahedral grid elements with quadratic shape functions are used. Two preprocessors

allow a layer-based input of the simulation geometry and the specification of the boundary conditions. They automatically perform meshing of the structures. A global grid level refinement is also available.

In contrast to other simulation tools our general approach does not assume a uniform current density in the conductive domains, provided the inductances can be related to the geometry only.

For our approach it makes a great difference whether self-inductance or mutual inductance is computed. Calculating the mutual inductance is done by rewriting the integrations as summations over each element of the conductors, which is possible due to the behavior of the integrand without any numerical difficulties. Calculation of self-inductance demands special formulae with certain integration points caused by singularities of the integrand.

The influence of the skin effect is neglected, thus results are valid as long as skin depth is large compared to the diameters of the interconnect structures. Our procedure is carried out without dividing the conductors into filaments and without assuming a uniform current density in the conductors.

Christian Harlander was born in Taxenbach, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1997. He joined the 'Institut für Mikroelektronik' in December 1997, where he is currently working on his doctoral degree in the field of three-dimensional interconnect simulation of multilevel wired VLSI circuits. In winter 2000 he held a visiting research position at Sony, Atsugi, Japan.

Optimization in Semiconductor Technology Analysis

Clemens Heitzinger

Technology CAD (TCAD) simulation environments have proven to be invaluable tools for the design and optimization of semiconductor devices. Thus the next generation of our Simulation Environment for Semiconductor Technology Analysis SIESTA is being developed with stability, flexibility and interactiveness in mind, while embracing the paradigms of functional and object-oriented programming. Dynamic load balancing enables the use of a cluster of hosts and a relaxation of the requirements on the software infrastructure. The integration of flexible, user configurable genetic optimizers and their integration with the gradient based optimizers are the most important new features.

This new approach combines the advantages of gradient based and genetic optimizers into one framework. Gradient based optimizers are well-suited for finding local extrema, whereas genetic optimizers add the capability of finding global extrema and thus make possible unattended optimizations without having to guess starting values.

The application of genetic algorithms to optimizations in our field has to take care of the fact that evaluating the score of one individual is usually computationally quite costly and that simulation tools are usually not written to accept arbitrary combinations of parameter values. Therefore, instead of the usual practice of simply picking the parameter values in pre-

defined intervals, we enable the user to impose arbitrary constraints, defined as functions in the parameter space, on the set in which solutions are searched for. Evaluating the constraints before any simulation tool is called and getting rid of futile combinations of parameter values saves computation time and eliminates the risk of the simulation tools being called with input values that might lead to unforeseen behavior.

Experiments can be interactively set up and tested. Bindings for the most common simulation tools are provided, and new bindings can easily be integrated taking advantage of the object-oriented and functional design. The results of the experiments are saved in an object database and can be interactively retrieved as starting points for further computations or for visualizations.

An independent graphical user interface is currently being developed. Running on a different computer, it can dynamically connect to and disconnect from the main program. It facilitates setting up experiments, running them, observing the optimization progress and interpreting the results.

The combination of gradient-based and genetic optimizers enables many new optimization strategies. Finding suitable starting values, a prerequisite for using gradient based optimizers, is not a requirement anymore.

Clemens Heitzinger was born in Linz, Austria, in 1974. He studied Technical Mathematics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in February 2000, where he is currently working on his doctoral degree. His scientific interests include optimization of semiconductor devices and mathematical modeling for device and circuit simulation.

Multi-Dimensional Ion Implantation Simulation with MCIMPL

Andreas Hössinger

In modern semiconductor process technology, ion implantation is used to introduce dopants into semiconductor materials. Ultra shallow junctions, very complex device structures with strongly non-planar surfaces, and the necessity to provide very accurate point defect distribution for the simulation of rapid thermal annealing processes require Monte Carlo methods for the simulation of ion implantation.

The Monte Carlo ion implantation simulator MCIMPL is a multi-dimensional simulator which can handle one-, two- and three-dimensional problems. The simulated device may be of arbitrary shape and may consist of various amorphous and crystalline materials. The implantation of a wide variety of single atomic and molecular ions can be simulated, such as boron, nitrogen, fluorine, silicon, phosphorus, arsenic, indium, antimony, BF_2 or N_2. In order to be able to provide very accurate impurity distributions and point defect distributions sophisticated models are implemented. For example the Follow Each Recoil method allows an accurate prediction of the distribution of the interstitials and vacancies and makes it possible to accurately predict the formation of implantation induced amorphous areas in a crystalline substrate.

The Monte Carlo method in general, and especially if methods like the Follow Each Recoil method are applied, is a very CPU time-consuming task. Even with several speed-up methods

such as the trajectory reuse and the trajectory split method implemented in MCIMPL, the CPU time required for the simulation of ion implantation can be more than one day for three-dimensional applications, and typically exceeds the CPU time required for the simulation of any other process step.

The parallelization of the Monte Carlo ion implantation simulation process step is therefore desirable in order to avoid a bottleneck in the process simulation flow, which consists of several successively executed process steps, because normally a cluster of workstations is available to perform process simulation and optimization. We have implemented a parallelization method based on MPI (Message Passing Interface) into MCIMPL. The parallelization strategy is optimized for a cluster of workstations connected by slow (10 MBit/s or 100 MBit/s) networks. We could achieve to keep the communication overhead so low that it has almost no influence on the performance gain achieved by parallelization. The idea of the parallelization method is to distribute the simulation domain among several processors, which makes it possible to achieve not only an almost linear performance gain but also a distribution of the memory requirement among several workstations.

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Investigations on Low Power Electronics

Robert Klima

The ever increasing success of CMOS technology is strongly coupled with the continuous miniaturization of the devices. Miniaturization yields lower costs per transistor and improves the electrical behavior. The fast growing market for portable electronics and increasing demand for lifetime and reliability have initiated a rapid worldwide development of ultra-low-power technologies to drastically reduce the overall power consumption of electronic circuits and devices.

The National Roadmap of Semiconductors prognoses gate lengths of 0.07μ within the next decade. As the sizes decrease the electric fields have to be scaled by the same factor in order to obtain similar electrical parameters. Therefore geometric parameters like the gate oxide thickness and material parameters like the channel doping have to be adjusted. But downscaling the gate thickness leads to an increased gate capacitance. Small channel lengths give rise to parasitic effects known as short channel effects.

As the sizes become smaller additional implantations become necessary. A smaller gate length results in a thinner gate oxide. In order to generate the necessary charge density channel doping has to be increased which in turn reduces the depletion layer. This area acts as a parasitic capacitance. With an additional implantation known as retrograde well this capacitance can be reduced. Pockets or halo implants are used in order to avoid punch through. Thus, the potential barrier at the source and drain well is increased which decreases leak-

age currents through the substrate. Furthermore it has been shown that a doping peak below the gate near the source well increases device performance by several ten percent compared to a uniformly doped device.

All these additional implants influence the electrical behavior of the device, as comparison to a uniformly doped device shows. Using the optimization framework SIESTA doping optimizations are performed in order to investigate and evaluate the contributions of the complex doping distribution. The doping profile is studied using distributed doping in relation to analytical and measured doping profiles. The optimal device is specified by drive performance parameters like the on and off current as well as by additional parameters describing several parasitic effects. These parameters are found by evaluating curves extracted from the output device resulting from each simulation of the optimization. The extractions of the curves are performed by scripts for an automated optimization process.

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Photolithography Simulation

Robert Kosik

LISI, an overall three-dimensional photolitography simulator, has been developed, which accounts for all of the three lithography subprocesses of mask imaging, resist exposure/bleaching and resist development. The simulator so far consists of three modules, whereby each module is specialized for one subprocess. We complement the simulator by implementation of a fast Maxwell equation solver.

Much of the tremendous progress in integrated circuit technology and performance over the past 30 years has been fueled by the progress in lithography. Optical lithography continues to be the key enabler and driver for the semiconductor industry. Modern resolution enhancement technologies allow sub-diffraction printing by controlling the phase as well as the amplitude of the light at the image plane in the printing system through the use of phase-shifting masks and other "tricks". The limit of the improvements offered by these techniques is the ability to print features at roughly half the wavelength of the light being used. However, for a rigorous simulation of phase-shifting masks the solution of the Maxwell equations is required.

A second field where a rigorous solution of the Maxwell equations is necessary is light propagation within the photosensitive resist. The resist is a thin layer of photosensitive material on top of the wafer. It records the mask pattern by absorbing light energy according to the illumination of the mask. Thereby the resist bleaches and the mask pattern are transferred to

a latent bulk-image. When modeling the light propagation within the photosensitive resist one has to take into account electro-magnetic scattering effects due to a non-planar topography. Since the geometrical dimensions are comparable with the used wavelength, a physically rigorous three-dimensional topography simulation must solve the Maxwell equations in a nonlinear medium.

For this purpose we implement a finite element solver. What makes the situation especially difficult in lithography are the boundary conditions. The aerial image simulator computes the incident light on the wafer surface, so the incoming half of the radiation is known. This corresponds to nonlocal boundary conditions, which complicates the solution of the partial differential equations.

The use of a Maxwell solver for TCAD in microelectronics is of course not restricted to lithography. While lithography is the first test area for applications, we try to keep the solver for general purpose. Adhering strictly to object-oriented design and to the principles of generic programming, it will be possible to accommodate it to a great variety of applications in the future, such as high speed transistors and opto-electronic devices.

Robert Kosik was born in Eisenstadt, Austria, in 1969. He studied technical mathematics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. After his community service he joined the 'Institut für Mikroelektronik'in October 1998, where he is currently working on his doctoral degree. His scientific interests include applied and numerical mathematics, especially computational electromagnetism.

A Monte-Carlo Method for Small Signal Analysis of the Boltzmann Equation

Hans Kosina

Understanding the Monte-Carlo (MC) method as a versatile tool for solving integral equations enables its application to a class of problems which are not accessible by purely physically-based, imitative MC methods. In electrical engineering linear small signal analysis of nonlinear systems plays an important role. Whether the linearized system is analyzed in the frequency or time domain is just a matter of convenience since the system responses obtained in either domain are linked by the Fourier transform.

A MC method permitting linear small signal analysis of bulk carrier transport has been developed. Choosing a formulation in the time domain, a small perturbing field is superimposed on a stationary field. The stationary distribution function thus is perturbed by a small response distribution function. Inserting this perturbation approach into the transient Boltzmann Equation (BE) and retaining only first order terms yields the stationary BE and a coupled Boltzmann-like equation which is linear in the perturbing field.

Compared with the transient BE, this Boltzmann-like equation has an additional term on the right-hand side containing the stationary distribution function. Assuming the perturbing field to be a Dirac delta function in time the equation determines the impulse response distribution function. The initial condition, being proportional to the gradient of the station-

ary distribution function, cannot be interpreted as an initial distribution due to lack of positive definiteness. However, the initial condition can be expressed as a difference of two positive functions, and so can the impulse response distribution function. In this way the impulse response is understood in terms of the concurrent evolution of two carrier ensembles. Using different methods for generating the initial distributions of the two ensembles gives rise to a variety of MC algorithms. Both existing and new MC algorithms are obtained in a unified way, and a transparent, physical interpretation of the algorithms is supported.

For electrons in Si the impulse response of mean energy and mean velocity has been calculated at different field strengths. The frequency-dependent differential mobility is obtained by a Fourier transform of the impulse response. In GaAs, at temperatures as low as 10K, electrons exhibit the so-called transit time resonance effect. The impulse response shows oscillatory behavior, and the real part of the differential mobility is negative in some frequency intervals.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. In summer 1993 he held a visiting research position at the Advanced Products Research and Development Laboratory at Motorola, Austin, in summer 1999 a research position at the TCAD department at Intel, Santa Clara. In March 1998 he received the 'venia docendi' in the field of 'Microelectronics'. His current interests include device simulation, modeling of carrier transport and quantum effects in semiconductor devices, new Monte Carlo algorithms, and computer aided engineering in VLSI technology.

Boltzmann and Quantum Transport in Semiconductor Devices

Mihail Nedjalkov

The behavior of small semiconductor devices is influenced by rare events occurring during the carrier transport process. The advanced Monte-Carlo (MC) simulators rely on statistical enhancement techniques in order to account for such events. The common feature of these techniques is that they can be applied only after the rare event occurs. A method which enforces the occurrence of such events has been developed for transient simulations and theoretically extended for steady-state simulations. The method modifies the probabilities which build up the natural carrier trajectories.

The correct statistics for the averaged quantities is recovered by the ratio between the physical and the modified probability, which is accumulated into a characteristic quantity called weight. The physical averages are multiplied by the weight which was collected during the trajectory evolution.

Experiments are performed by a one-dimensional MC simulator, which accounts for a variety of relevant semiconductor materials. The carriers have been forced to overcome energy barriers in two ways. The after-scattering angle has been biased in order to increase the number of particles which hit the barrier. The absorption of optical phonons has been stimulated with respect to the emission process in order to increase the carrier kinetic energy. The method demonstrated an improvement of the performance of statistical enhancement schemes.

The second issue which has been addressed here is transport modeling of carriers beyond the Boltzmann picture. Particularly the femtosecond relaxation of an electron system interacting with phonons is considered. The process is described by the zero field Barker-Ferry equation. The electron-phonon interaction is switched on after a laser pulse creates an initial electron distribution. This assumption allows to study the properties of the equation conveniently. The latter has been solved by a stochastic approach for GaAs. A variety of quantum effects can be demonstrated and explained by the structure of the kernel of the equation. The collisional broadening effect is related to the finite electron lifetime which broadens the energy conserving delta function to a Lorentzian function. The collision retardation is due to the non-Markovian character of the kinetics.

Mihail Nedjalkov was born in Sofia, Bulgaria, in 1956. He received the 'Master' degree in semiconductor physics at the Sofia University and the Ph.D degree at the Bulgarian Academy of Sciences (BAS) in 1981 and 1990. Since 1993 he has been with the CICT, BAS, currently in a procedure for Associate Professor. He was visiting researcher at the Universities of Bologna, 1992, Modena, 1994 and 1995, and Frankfurt, 1997. Since 1998 he has been holding a visiting research position at the 'Institut für Mikroelektronik'at the 'Technische Universität Wien'. Besides the national research projects, he participated in INFM (Italy) and FWF (Austria) and is currently supported by the European project NANOTCAD. His research interests include numerical theory and application of the Monte Carlo method, physics and modeling of Boltzmann and quantum transport in semiconductors and semiconductor devices.

Simulation of Heterojunction Bipolar Transistors

Vassil Palankovski

Heterojunction Bipolar Transistors (HBTs) are of significant importance for mobile telecommunication systems. Due to the ability to handle high current densities they are quite suitable for use in power amplifiers. Accurate simulation of the electrical behavior of HBTs gives deeper understanding of the underlying device physics and helps to save expensive technological efforts when improving device performance.

The two-dimensional device simulator MINIMOS-NT deals with different complex materials and structures, such as binary and ternary alloys with arbitrary material composition profiles. Various physical effects, such as band gap narrowing, surface recombination, and self-heating, are taken into account. The efficiency of the models has been proven by hydrodynamic DC-simulations with self-heating of forward, reverse and output characteristics of one-finger AlGaAs/GaAs and InGaP/GaAs-HBTs, and by small-signal RF-simulation. The S-parameters have been simulated in the range from 0 to 20 Ghz using a T-like, eight-element small-signal equivalent circuit. All simulation results are in very good agreement with measured data for several device structures in a wide ambient temperature range.

Simulations of one-finger power InGaP/GaAs-HBTs before and after both electrical and thermal stress aging have been performed. It is well known that the reliability of GaAs-HBTs

with InGaP emitter can be improved if the emitter material covers the complete p-doped base layer, forming outside the active emitter the so-called InGaP ledge. The influence of ledge thickness and of surface charges on device performance and their impact on reliability have been analyzed. The possibility of explaining device degradation mechanisms by means of numerical simulation is of high practical relevance.

Based on these investigations it is possible to explain the base current degradation of an InGaP/GaAs-HBT which was strongly stressed under conditions far from normal operating conditions. In this case the base current degradation in the middle voltage range of the forward Gummel plot can be explained by a decrease in negative surface charge density along the interface between ledge and passivation. This is possibly due to compensation of the negative surface charges by H^+ ions which are known to be present in the device due to the epitaxial manufacturing processes.

Several other effects supposed to decrease the collector current at high level injection, such as emitter contact detachment, indium segregation in the metal layer, or dislocations in the emitter cap at the InGaAs/GaAs interface, have been analyzed as well.

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Integrating Equipment Simulation into Feature Scale Profile Evolution

Wolfgang Pyka

For wafer sizes ranging up to 300 mm yield and quality issues become increasingly determined by the uniformity of the processes across the wafer. This is especially important for the formation of contacts which are usually fabricated as compounds of different layers in order to fulfill the long list of requirements such as low contact resistivity, metallurgical isolation, protection from aggressive reactants from subsequent process steps, sufficient adhesion, leakage free film formation, and void free filling.

With respect to simulation such non-uniformities across the wafer can only be covered by combining reactor and feature scale simulations. Concerning low pressure processes such an integration has been completed on three different levels. First, analytical distribution functions for the impinging particles can be arbitrarily rotated and tilted in order to account for the considered position on the wafer. Second, fitting functions for angular particle distributions resulting from Monte Carlo simulations consider particle transport from the sputter target to the wafer and can be transformed in the same way as the analytical functions. Finally, distribution functions can also be set according to particle fluxes resulting from fully three-dimensional Monte Carlo simulations of sputtering particle transport.

Reactor/feature scale integration has also been achieved for high pressure chemical vapor deposition processes. After completion of the three-dimensional feature scale continuum transport and reaction model, equipment simulations can be linked to profile evolution by setting the corresponding boundary conditions in the feature scale model according to the reactants' concentrations resulting from reactor scale simulations. Moreover, the concentration and temperature variations obtained from the equipment level simulations directly influence the species' diffusivities and the activation energy terms for the rate expressions of the chemical reactions. Variations in growth rate and overall film thickness across the wafer can be covered by adjusting the local deposition rate.

With these means of equipment simulation, variations in sputtering and chemical vapor deposition processes can be fully characterized for any position on the wafer and the influence of these variations on the final, three-dimensional film profile can be analyzed. This technique has been applied to an integrated tungsten plug-fill process consisting of a Ti PVD, TiN PVD, TiN CVD and W CVD deposition sequence and predicts possible leakages in the barrier layer formation as well as void or keyhole formation in the tungsten bulk deposition.

Wolfgang Pyka was born in Innsbruck, Austria, in 1970. He studied materials science at the 'Montanuniversität Leoben', where he received the degree of 'Diplomingenieur' in 1996. In December 1996 he joined the 'Institut für Mikroelektronik', where he received his doctoral degree in May 2000. In summer 1998 and 1999 he held visiting research positions at LSI Logic, Milpitas, CA. His work is focused on simulation and modeling of etching and deposition processes and on algorithms for topographic simulations and three-dimensional geometry generation.

Modeling and Simulation of High Electron Mobility Transistors

Rüdiger Quay

High Electron Mobility Transistors (HEMTs) based on GaAs or InP substrates are available for the frequency range up to 215 GHz at present. Pseudomorphic AlGaAs/InGaAs/GaAs HEMTs are used up to the W-band, InAlAs/InGaAs HEMTs, lattice matched to InP dominate up to the D-band, but they are challenged by metamorphic technologies under development. The pseudomorphic AlGaAs/InGaAs/GaAs HEMTs are replacing the MESFETs for an increasing number of low noise and power applications for industrial mass production. AlGaN/GaN HEMTs with gate-length down to 150 nm have successfully been demonstrated and reveal extremely promising RF-power characteristics, though a lot of technological questions are still to be answered. Device simulations of pseudomorphic AlGaAs/InGaAs/GaAs and lattice matched InAlAs/InGaAs/InP HEMTs have successfully been verified for several technologies. The simulation of AlGaN/GaN field effect transistors with MINIMOS-NT is under development parallel to the technological progress. Device simulation is used for the optimization and simplification of devices and processes and verified for the frequency range up to 120 GHz.

One focus of the work lies on process control with respect to device characteristics. This includes statistical analysis of measured data for several lots and correlation to device simulation in order to characterize technologies instead of single devices. For example, for the W-band the stability of de-

vice performance with respect to technology and bias variations over various wafers is investigated in order to develop devices suitable for mass production for gate lengths of 150 nm and below. Physically-based S-parameters simulations are used to control RF characteristics. It has been demonstrated for several devices that DC as well as RF device simulation for different HEMT technologies reveal equally good performance independently of the technology used. The extraction of large signal models from MINIMOS-NT is under development. This is based on the extended modeling features within MINIMOS-NT that can be adjusted to the technology without further changes.

Especially with respect to power applications up to 40 GHz, the description of breakdown and self-heating effects in the device becomes crucial. Self-heating is included into device simulation both by a local self-heating and a global self-heating concept. Impact ionization models are used to simulate high Drain Source voltages. Gate currents are successfully simulated and correlation to measurements reveals precise information on the breakdown mechanism of the respective HEMT technology.

Rüdiger Quay was born in Köln, Germany, in 1971. He studied physics at the University of Bonn and the RWTH Aachen, where he received his Diploma in Physics in 1997. In summer 1996 he held a visiting research position at Los Alamos National Laboratory, New Mexico, for his master's thesis. He joined the 'Institut für Mikroelektronik' in April 1998. He is currently working on his doctoral degree at Fraunhofer Institute for Applied Solid-State Physics in Freiburg, Germany. In 1999 he was a visiting researcher at the Beckman Institute, University of Illinois, Urbana Champaign. His scientific interests include device simulation, heterostructure device modeling, physically-based RF-parameter extraction, and reliability issues.

Extending the Capabilities of MINIMOS-NT

Rodrigo Rodríguez-Torres

A widespread set of problems in the electronics industry can be solved by means of three-dimensional simulations. Simulation of parasitics and other second-order effects are currently being investigated in three-dimensional approaches. Although the models do not involve too complex mathematics, the implementation in an efficient computational way is a challenging task. If the amount of operations has a large impact in a single-mode simulation, those operations should be reduced to the minimum when one wants to incorporate effects such as mixed-mode and thermal simulations.

The current version of MINIMOS-NT allows the user to simulate a device of any geometry under various operation conditions. However, the device description can only be given in two dimensions because the libraries used to read, simulate, and write the simulated devices are at present restricted to this case. The three-dimensional description is available through the PIF syntax. Due to the excellent design of the MINIMOS-NT code, carrying out those modifications needed for three-dimensional simulation only implies generating code in such a way that it does not interfere with the characteristics already present in the MINIMOS-NT simulator. As soon as this new characteristics is available, MINIMOS-NT will be used to analyze three-dimensional effects, such as magnetic effects in inversion layers from magnetic field effect transistors (MAGFETs).

MAGFETs are magnetic field sensors based on the normal deflection suffered by the carriers in an inversion layer of a field effect transistor. In order to *detect* a deflection of those carriers, which is governed by the Lorentz force, the drain contact of a normal field effect transistor is divided into several contacts. If a magnetic field is applied perpendicularly to the inversion layer of a MAGFET, it is possible to sense its magnitude and direction.

Investigation of magnetic sensors requires that a device is simulated in a three-dimensional situation, since the Lorentz force is a three-dimensional effect. However, there are many more situations and device effects which can be understood only by means of three-dimensional simulation.

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Accurate Three-Dimensional Interconnect Simulation

Rainer Sabelka

The performance of deep submicron integrated circuits is increasingly determined by the metal interconnections between devices. With clock frequencies in the GHz regime, the gap between digital and microwave designs is becoming narrow. Care must be taken of various parasitic effects, such as attenuation caused by resistive voltage drops, self-heating due to losses, delay times, crosstalk caused by capacitive or inductive coupling, or by the substrate, reflections incurred by discontinuities, skin-effect and eddy currents, for example in on-chip spiral inductors. While it is important to consider the inductive effects of very long interconnects with low resistance and, of course, of on-chip inductors, the electrical characteristics of local interconnect lines is mainly determined by their resistance and capacitance. With the introduction of new materials such as Copper and low-k dielectrics, parasitic effects could be reduced to a certain degree, but not eliminated. Hence, highly accurate models are required, especially for designs with reduced safety margins close to the physical limits.

Therefore the "Smart Analysis Programs" (SAP) have been developed. This simulation package contains tools for highly accurate extraction of parasitic capacitances, resistances, and inductances, quasi-electrostatic simulation, and investigation of the thermal behavior of the interconnect stack. Special attention has been directed to an efficient implementation concerning both runtime and memory consumption. The simula-

tor has the ability to perform calculations with anisotropic dielectric materials and coupled electro-thermal simulations with temperature-dependent material properties. The finite element method (FEM) is used for the numerical solution of the partial differential equations. This method is preferred to other methods because of its numerical robustness and the applicability to all involved equation types.

For highly accurate simulations it is essential to model the simulation domain geometrically as exactly as possible. A two- and a three-dimensional solid modeler are used to construct the simulation geometry either directly with an input deck, by generating it automatically from layout, or from using the output of a lithography and/or topography simulation. The simulation grid is either generated by a layer-based technique or with a fully unstructured Delaunay mesher.

A three-dimensional visualization program has been developed in order to display the calculated distributed scalar and vector fields such as potential, temperature or current density by means of contour faces, streamlines, cuts, and surface representation.

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Study of Quantum Effects in MOS Devices

Christian Troger

As a consequence of continuous scaling of MOS devices and the resulting high transverse electric fields at the interface, the quantum mechanical behavior of the so-called two-dimensional electron gas that forms in the channel of such transistors has to be investigated in any accurate device modeling. Even if this problem has been faced for more than two decades, the high number of recent publications in this field can be considered an indication that many problems still remain unsolved and that we are far from a reliable, easy to use, fast and robust quantum mechanical simulation tool for semiconductor devices.

In the last years we therefore developed and improved a one-dimensional Schrödinger Poisson solver (SPIN). The program is based on effective mass approximation, a non-parabolic correction for energy dispersion, uses a sinus series expansion for wave functions and includes some additional improvements for optimizing speed and accuracy. In its actual version the program can now be considered a reliable tool for the investigation of quantum effects in MOS devices.

One application was justifying the widely used quantum mechanical correction due to Hänsch for the classical electron density in the case of an oxide thickness of only 2.5nm. The results showed a good coincidence between the classical correction and the full quantum mechanical simulation for both the calculated C-V curve and the electron density. This knowledge

was used for a further speed improvement of the simulator, as we could include this correction in the initial solution.

A further important application of the Schrödinger Poisson Solver is using the resulting eigen energies and wave functions of the subbands in a subsequent Monte Carlo simulation of the electron transport in the channel. One major challenge in this task is the accurate modeling of the scattering rates between the different quantized states. The Coulomb scattering will give a significant contribution to the electron behavior during its motion along the channel. Thus for the purpose of accurate modeling, and of course in order to remove the singularity in the formula of this scattering rate, the screening effect resulting from the other electrons cannot be neglected. In contrast to the three-dimensional case, where this effect can be treated with a modified dielectric function, the screening effect for the two-dimensional case results in such complicated calculations that some simplifications are needed. We decided to consider only the screening contribution from a single subband and used again the Fourier domain for all the calculations.

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