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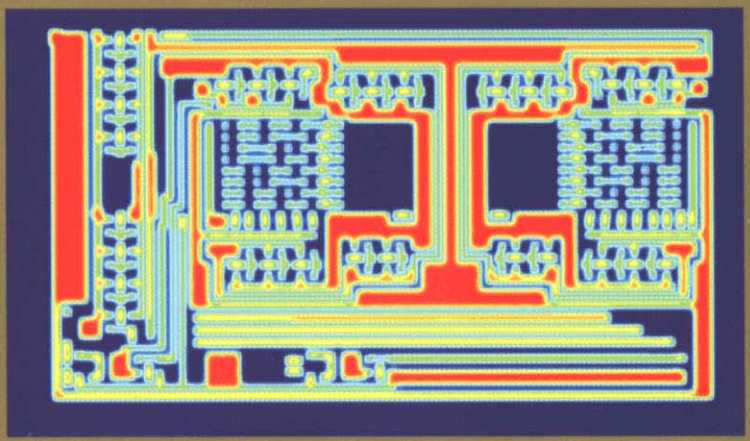

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Preface

Siegfried Selberherr

With this brochure, the annual research review of the Institute for Microelectronics, we document the successful end of the first decade of our research. The staff financed by the Austrian Ministry of Science and Transportation consists of nine full time employees: a full professor, five scientists, a secretary and two technical assistants. Eighteen additional scientists are funded through scientific projects supported by our industrial partners.

We are quite satisfied with our academic and scientific output. Over the decade 238 contributions have been prepared for conference digests, and 67 manuscripts have been published in reviewed journals or books. 36 researchers could finish their doctoral theses, and 50 students got ready with their master's theses.

Two researchers, Erasmus Langer and Hans Kosina, who have been guiding the institute from the very beginning, have crowned their research with the habilitation.

Particularly pleasing this year is an all-time-high number of contributions and participations in international conferences.

We have been successful with projects focused on microelectronics modeling issues. Technology Computer-Aided Design (TCAD) is the area which is now commonly established for this kind of activity. We shall continue our way, and are entering the next decade of our institute with high expectations.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplom-ingenieur' in electrical engineering and the doctoral degree in technical sciences from the 'Technische Universität Wien' in 1978 and 1981, respectively. Since that time he has been with the 'Technische Universität Wien' as professor. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. He has been the head of the 'Institut für Mikroelektronik' since 1988. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Interpolation Methods on a Network Distributed Grid

Thomas Binder

The simulation of a semiconductor fabrication step requires to handle various distributed quantities, so-called attributes. Such attributes are, for example, the doping profile, the stress components, lattice temperature and the like. These data are stored on a so-called wafer state grid. In order to account for the characteristic behavior of the involved attributes a wafer state library has to provide different interpolation methods. The current, non object-oriented approach delegates the problem of deciding which interpolation method to apply on what kind of attribute to the application, i.e. the simulator. The simulator would rather not care about interpolation, but instead leave this decision to a library.

When a simulation takes place the first step usually is to create a simulation grid based on the supplied input wafer state. This simulation grid can differ from the wafer state grid in terms of resolution and number or type of attributes. The step of creating the simulation grid not only demands to grid or re-grid the whole geometry of the device, but also necessitates the transfer of distributed quantities from the wafer state grid to the simulation grid. In order to facilitate this transfer for the simulators the actually used interpolation method is hidden from the user. This is achieved by an object-oriented approach, in which all used attributes are classified and each class uses its own interpolation method. This ensures that simulators need not care about interpolation methods at all. A major advan-

tage of this strategy is not only the transparent invocation of interpolation methods but also the uniform way various simulators interact with one library, thereby making integration of different simulators possible.

Another aspect when simulating process steps is the amount of time consumed by a certain simulation. One solution to decrease computation time is to split the simulation task into individual threads, each dedicated to a certain domain of the wafer state, and to distribute these threads over the network. In order to allow for such a distribution one needs a network supporting data model. Since most simulators work on grid-based data structures the demand to spread a grid over a network of computers arises. When a hierarchical data structure like a finite oct-tree is used to organize the data, leafs of this oct-tree can be held on different machines. The simulator can then start several simulation threads in parallel, each on a different computer and each working on a different simulation domain.

Thomas Binder was born in Bad Ischl, Austria, in 1969. He studied electrical engineering and computer science at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in December 1996. During his studies he was working on several software projects mainly in the CAD, geodesic and security fields. In March 1997 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. His scientific interests include data modeling, algorithms, software engineering and semiconductor technology in general.

Simulation of Ferroelectric Nonvolatile Memory Cells

Klaus Dragosits

The development of nonvolatile memory cells using ferroelectric materials leads to designs, such as the ferroelectric field effect transistor (FEMFET), which employ two-dimensional hysteretic field properties. Therefore, a general device simulator like MINIMOS-NT has to be adapted to these new devices. The simulation of the two-dimensional hysteresis curve leads to the nontrivial problem of field rotation and forces the calculation of a set of parameters for the nonlinear locus curve at each grid point. To allow the calculation of transfer characteristics the algorithm has to be insensitive to the magnitude of the applied voltage steps. To keep pace with future developments of ferroelectric devices, the expansion of the algorithm to three dimensions should be possible.

For a general approach to two-dimensional hysteretic effects an inhomogeneous field distribution has to be assumed. This prevents the use of a simple one-dimensional hysteresis model using the same locus curve for the entire ferroelectric region. Two different locus curves have to be calculated for each grid point. Therefore, numerical methods to calculate the locus curves cannot be applied.

The simulation of field rotation leads to nontrivial problems. Similarly to magnetic properties the rotation of a constant magnetic field causes a lag angle χ of the induction. For a rigorous two-dimensional analysis, the simple approach to de-

crease the electric field first to zero, then to increase it to the value of the next operating point and to add the two polarization components derived cannot be employed, as it is inconsistent with the one-dimensional hysteretic properties. Additionally, the results strongly depend on the distance between the calculated operating points. According to this we assume a straight trajectory between the vectors of the old and the newly applied electric field. This also assures a proper numerical behavior if the applied voltage steps will be increased. The basic principle of the applied algorithm is to split polarization and electric field of the previous operating point into components parallel and orthogonal to the next electric field. These curves yield the polarization in direction of the electric field and the remanent polarization in the orthogonal direction, thus forming a primary guess for the next polarization. The scalar values of the two components are added and compared to the maximum polarization at the given magnitude of the electric field, forming an upper limit for the available number of switching electric dipoles. Due to the vanishing electric field in the normal direction, making it easier to switch the dipoles in this direction than the dipoles held by the electric field, the orthogonal component is reduced appropriately in respect to this limit.

Klaus Dragosits was born in Bruck an der Mur, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. He joined the 'Institut für Mikroelektronik' in September 1997, where he is currently working for his doctoral degree. His scientific interests include device simulation with special emphasis on nonvolatile memory cells.

Slivers in Delaunay Tetrahedralizations

Peter Fleischmann

For three-dimensional meshing applications Delaunay methods are commonly employed. The reason lies in the efficiency and the mathematical background of the Delaunay triangulation as the dual of the Voronoi Graph. In fact, Delaunay techniques are preferred not merely because of the special properties of a Delaunay mesh, but often because of the efficient algorithms to compute the Delaunay triangulation. For instance, pure advancing front methods involve computationally expensive intersection tests. The advantage of Delaunay methods is the speed of computation. The connectivity between the mesh points is mathematically defined. Another property is the logical separation between distributing mesh points and connecting them ('place nodes and link'). This has several advantages. The mesh generator offers more flexibility, because the actual volume decomposition does not require to change the mesh points. There are many ways how this can be exploited. For example, an advancing front technique can be combined with a Delaunay method to produce boundary-conform meshes.

To achieve this orthogonality the 'linking' step of the mesh generator must accept an arbitrary mesh point distribution without any restriction. Then, it becomes possible to generate mesh points from advancing fronts, from simple oct-trees, or from other methods regardless of the volume decomposition. Hence, the Delaunay implementation must accept degenerate point sets (in Delaunay sense). One typical degenerate set is given by four or more co-circular points in three dimen-

sions. A straightforward Delaunay method fails to guarantee that all elements are connected properly. (Imagine a square as an interface between two cubes where both diagonals exist and intersect due to the inconsistent face connectivity.) Such cases, the well-known un-tetrahedrizable Schoenhardt polyhedron (twisted prism), and poorly shaped sliver elements have something in common. A simple experiment shows this relationship: If one applies random noise of small amplitude to the location of the points of a degenerate set, the result is a non-degenerate point set. The resulting Delaunay tetrahedralization will contain many sliver elements with the height in the order of magnitude of the amplitude of the added noise. In other words, if one takes a topologically correct Delaunay tessellation and shifts the points of the degenerate point set, the result will be slivers with either positive, zero, or negative volume.

We have extended our data-structures to allow specially marked sliver elements. They can have positive, zero, or negative volume. The mesh topology remains consistent at all times. In a post processing step such sliver elements will be removed by local transformations. In a uniform way inconsistent face connectivities resulting from degenerate point sets as well as general poor quality slivers will be removed.

Peter Fleischmann was born in Kabul, Afghanistan, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994. In December 1997 he was with NEC in Sagamihara, Japan. He is currently working for his doctoral degree. His research interests include mesh generation as well as algorithms and data structures in computational geometry.

New Features for the Device Simulator MINIMOS-NT

Tibor Grasser

Recent advances in the development of semiconductor devices have lead to more and more complex device structures. This concerns device geometry as well as the combination of different materials. Due to the rapid reduction of device geometries, the models describing the device physics increase in complexity. To gain additional insight into the performance of devices under realistic dynamic boundary conditions imposed by a circuit, mixed-mode simulation has proven to be invaluable.

Our device simulator MINIMOS-NT is equipped with an extensive mixed-mode capability including HD modeling on distributed devices. In general the convergence of HD simulations is known to be poor. Therefore, we have enhanced MINIMOS-NT with an interface where different iteration schemes such as the full Newton scheme and various block iteration schemes based upon the Gummel scheme can be easily defined and augmented with special damping algorithms.

To allow for a flexible handling of distributed devices in a mixed-mode circuit simulation, their geometry is partitioned into independent regions, so-called segments. For these segments different sets of parameters, models and algorithms can be defined independently. For example, it is possible to solve only Poisson's equation on one segment, or the transport equation for only one carrier type in addition to Poisson's equation on another segment. The segments are linked by interface

models which account for the interface conditions. This results in high flexibility which allows, for example, to use an HD model on one segment and a drift diffusion (DD) model on another segment. Furthermore, the explicit treatment of volume and interface models leads to a better condition of the linearized system compared to a method which simply reduces grid spacing in the vicinity of heterojunctions.

During the simulator development we have frequently encountered the problem that several different formulations for, e.g., the HD model are available (either in the model itself or in its discretization). To compare these formulations easily in a general manner, without adding a lot of keywords or recompiling the code, we have developed and implemented a particular strategy. The partial differential equations (PDEs) are split into their constituent parts. These parts are assembled in so-called groups which can then be selected for simulation. A proper design of these groups is of course crucial. This allows for a modular combination of equation parts to build the equation system.

Tibor Grasser was born in Vienna, Austria, in 1970. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1995. He joined the 'Institut für Mikroelektronik' in April 1996, where he is currently working for his doctoral degree. His scientific interests include circuit and device simulation, device modeling and physical aspects in general. In autumn 1997 he held a visiting research position at Hitachi, Tokyo, Japan.

Inductance Calculation in Interconnects

Christian Harlander

For a long time the speed of integrated circuits was largely determined by the switching speed of the individual transistors. The characteristics of the signal transfer from one device to the next were negligible. As switching times were accelerated, interconnect characteristics became critical and required accurate chip layout and system design for reducing the transfer delay.

Currently, interconnection- and packaging-related issues are among the main factors, determining the chip performance as well as the number of circuits that can be integrated in a single chip. Reflections, cross talk and simultaneous switching noise can increase delays or cause logical faults, and therefore should be minimized by careful design. Cross talk is a result of capacitive and inductive coupling between neighboring lines and increases as the lines get closer and the distances they neighbor each other get longer.

The package SAP (Smart Analysis Programs) has been extended to perform the extraction of inductances. The simulator SAP uses the finite element method with linear and quadratic shape functions to calculate the distributions of the electric potential. The potential is derived by solving the Laplace equation for all single lines separately, with boundary conditions of either Neumann or Dirichlet type specified on the borders of each simulation subdomain. A preconditioned conjugate gradient solver is used to solve the linear equation

system, and the program package automatically performs meshing of two- and three-dimensional structures.

The distribution of the electric current density is obtained by applying Ohm's law to the derivative of the electrostatic potential. The current density is used for the computation of the magnetic vector potential and the magnetostatic field energy of each subsystem. This magnetostatic field energy is representative of the several mutual- and self-inductances of the interconnect structure.

This method achieves accurate results for complex structures with a large penetration depth. Applying the magnetic vector potential, the integrations only have to be done over the conductive segments. For the calculation of the self-inductances these integrations are performed with higher order formulas.

Christian Harlander was born in Taxenbach, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1997. He joined the 'Institut für Mikroelektronik' in December 1997, where he is currently working for his doctoral degree in the field of three-dimensional interconnect simulation of multilevel wired VLSI circuits.

Multi-Dimensional Ion Implantation Simulation with MCIMPL

Andreas Hössinger

In modern semiconductor process technology, ion implantation is used to introduce dopants into semiconductor materials. Ultra shallow junctions and very complex device structures with strongly non-planar surfaces require Monte Carlo methods for the simulation of ion implantation. A Monte Carlo ion implantation simulator has to be able to handle problems of arbitrary dimensions for a wide variety of ion species and target materials, and the CPU time requirements for the simulation have to be within acceptable limits.

The Monte Carlo ion implantation simulator MCIMPL is a fully three-dimensional simulator which can also handle lower dimensional problems. The simulated device may consist of various amorphous and crystalline materials. Besides the use of single atomic ions (boron, fluorine, silicon, phosphorus, arsenic, indium, antimony), two methods for simulating the implantation of molecular ions have been implemented recently. The first method (molecular method) treats molecular ions as real molecules. The implanted molecule is split when it enters the target and the distributions of all atom species of the molecule are calculated individually. This method is applicable for arbitrary molecules and also for ion clusters. The second method (simple method) only calculates the trajectories for the atom species which is most significant for the considered process, like the boron atom in a BF_2 molecule. The influence of all other atom species of the implanted molecule is derived

from the distribution of the calculated atom species. This is only possible if the distributions of all atom species are similar. The advantage of this method is that it is significantly faster than the molecular method, but the calculated distributions of the interstitials and the vacancies are less accurate.

For some processes a very precise calculation of the distribution of interstitials and vacancies is necessary, because they significantly influence the behavior of dopants due to transient enhanced diffusion effects. Therefore, a follow-each-recoil method has been added to MCIMPL which can be used besides an analytical damage model. Especially for high energetic ions the damage profiles can be simulated more accurately, and the shift between interstitials and vacancies can be evaluated, whereas the analytical damage model assumes similar profiles for the interstitials and the vacancies. The major disadvantage of the follow-each-recoil method is that it significantly raises the CPU time requirements especially for ions with very high masses.

Moreover, a modified treatment of the boundary conditions has been included. All boundaries except the surface are now treated as artificial boundaries within a wafer, rather than as interfaces of the simulation domain to air.

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Three-Dimensional Device Simulation with MINIMOS-NT

Robert Klima

With the increasing integration density of integrated circuits the feature sizes of the devices become smaller and smaller. Nowadays MOS device structures with gate lengths of a few 100nm are of high industrial interest. Due to the miniaturization the device structures appear three-dimensional, and the device geometries noticeably influence the electrical characteristics and the behavior of the device. Therefore, three-dimensional device simulations have to be performed. Typical examples for this are short and narrow channel effects, and punch-through effects in Dynamic Random Access Memory (DRAM) cells.

MINIMOS-NT is a two-dimensional general purpose device and circuit simulator consisting of a number of modules, such as the solver module, the mixed-mode module, the distributed device module, and the flow control. For the description, administration and storage of geometry, grid and attribute information the Profile Interchange Format (PIF) is used. The geometry, grid and attribute support modules support two-dimensional access to data and offer a number of functions to deal with it, for example interpolation or grid refinement. The extension to three dimensions mainly affects these three key modules, where three-dimensional structures must be introduced and the related functions must be extended. The PIF is designed to specify three-dimensional structures using points,

lines, faces, solids, segments, and geometries, where additionally solid handling must be introduced to MINIMOS-NT.

MINIMOS-NT is capable of dealing with tensor product and triangular grids. For the representation of three-dimensional structures tensor product and tetrahedral grids are commonly used. As a first step, tensor product grids will be implemented.

For effective mixed-mode simulations, information about the dimensionality of a device must be hidden. Therefore, a convenient object-oriented design for the handling of devices has to be introduced. This encapsulation allows to use one-, two- and three-dimensional devices within a circuit at the same time.

In three-dimensional simulations the equation system to be solved becomes very large. The computational costs increase dramatically. So performance is one of the main issues. Due to this fact, performance analyses over all modules are done to determine the critical ones. Various algorithms have to be optimized. To guarantee short simulation times some further optimizations like appropriate data structures and data management are initialized to reduce access time to the most frequently used data.

Robert Klima was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1997. He joined the 'Institut für Mikroelektronik' in September 1997, where he is currently working for his doctoral degree. His scientific interests include device and circuit simulation, computer visualization and software technology.

Device Simulation with MINIMOS-NT

Martin Knaipp

Modeling the various physical effects plays a key role in device simulation. An important set of effects is described by the recombination/generation (GR) processes. The simulation of leakage currents and the breakdown simulation of MOSFETs can be given as examples. A device where many of the GR processes can be studied is the simple pn-diode. The behavior of the device depends on the acceptor and donor profile and on whether the diode operates in forward or reverse direction. In reverse direction the processes of Shockley-Read-Hall (SRH) generation, Auger generation, trap assisted tunneling and band-to-band tunneling are responsible for the leakage current. In case of sufficiently high carrier temperatures an impact ionization current indicates the breakdown of the device.

In case of high local electric fields the ability of a trap to generate electron-hole pairs is enhanced. This effect is called trap-assisted band-to-band tunneling and is described by the so-called field enhancement factors. These factors reduce the average emission time for the electron-hole generation. At even higher electric fields the generation via trap assisted band-to-band tunneling is superposed by the direct band to band tunneling process. This process is explained by the field emission of a valence electron leaving back a hole. The basic theory of the direct tunneling model is the calculation of the tunneling probability from carrier bound states to the conducting band states. Usually the generated carriers are located at the mini-

mum of the conduction band and the maximum of the valence band. Since silicon is an indirect semiconductor the band minimum and maximum do not coincide in momentum space. To enable carrier generation with a defined electron momentum, lattice vibrations have to support the generation process.

In forward direction the processes of SRH recombination and Auger recombination play a major role. In case of stronger electric fields the additional processes of trap-assisted tunneling and band-to-band tunneling influence the amount of forward current. Usually the maximum electric field in forward direction is caused by the space charge in the pn-junction of the diode. When the applied forward bias is increased the depletion zone and the electric field in the junction are reduced. This is why the electric field in forward direction is highest when small biases are applied in combination with narrow junctions. A device which fulfills the described conditions is the so-called Esaki diode. At small forward biases the current increases up to a maximum value. When increasing the voltage, the current decreases because of the reduced band-to-band tunneling process. In this operating region the dominant effect is the trap assisted tunneling process. When raising the voltage again the Auger recombination and SRH recombination dominate the forward current.

Martin Knaipp was born in Vienna, Austria, in 1966. He studied technical physics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. In August 1994 he joined the 'Institut für Mikroelektronik', where he is working for his doctoral degree. His work is focused on device simulation, especially in high temperature effects. In autumn 1996 he held a visiting research position at Hitachi, Tokyo, Japan.

Physical Models and Algorithms for Advanced Device Simulation

Hans Kosina

Two issues concerning the modeling and simulation of semiconductor devices have been addressed. First, indirect recombination via coupled trap levels has been studied by means of numerical simulation. Second, new algorithms aiming at a reduction of computation time of Monte Carlo transport calculations have been investigated.

Silicon particle detectors are used extensively in high energy physics experiments. In future experiments the detectors will be exposed to high particle fluences causing significant atomic displacement damage. To get better understanding of experimental data from irradiated detectors and to gain insight into the degradation process, one-dimensional simulations of such detectors have been carried out. Quantities directly comparable with experiments are quasi-static capacitance versus voltage curves, leakage current curves, and the depletion voltage. The numerical model for the detector accounts for two coupled trap levels, and the charge carried by the traps is included self-consistently in the Poisson equation.

To make Monte Carlo device simulation suitable for TCAD purposes, a reduction of computation time is required. A method has been developed which allows to treat ionized-impurity scattering, a very frequent process in semiconductor devices, more efficiently. Instead of the highly anisotropic, physical process an isotropic process is used in the simulation

which gives the same momentum relaxation time. Depending on doping concentration and carrier energy, the isotropic process yields a scattering rate which is up to four orders of magnitude lower. The theoretical analysis of the Boltzmann equation indicates that using the equivalent, isotropic process has a negligible influence on the transport of carriers in semiconductors, unless the temperature is very low. Monte Carlo calculations have demonstrated the equivalence of both types of scattering models empirically.

The commonly used Monte Carlo algorithms are imitating the real transport process by calculating physical carrier trajectories. Severe problems are encountered when scarcely populated phase space regions have to be considered. A new project has started aiming at the development of generalized algorithms, which can be constructed from a formal iteration series for the distribution function. Existing algorithms of this type are the Weighted and the Backward Monte Carlo algorithms. In this project the steady state is considered, as well as the combination of different algorithms in different device domains.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. In summer 1993 he held a visiting research position at the Advanced Research and Development Laboratory at Motorola, Austin, USA. In March 1998 he received the 'venia docendi' on 'Microelectronics'. His current interests include modeling of carrier transport and quantum effects in semiconductor devices, new Monte Carlo algorithms, and computer aided engineering in VLSI technology.

AURORA — Advanced Models, Applications, and Software Systems for High Performance Computing

Erasmus Langer

AURORA is a national research project funded by the Austrian 'Fonds zur Förderung wissenschaftlicher Forschung'. The project has been started in April 1997 with the first period of three years; the maximum duration of such a *Special Research Field* ('Spezialforschungsbereich') is ten years on the condition that the intended evaluation yields a positive result. The funds for all participating institutions amount to approximately 8.5 millions ATS per year.

AURORA has a distinctly interdisciplinary character. Seven research groups belonging to different institutes of the 'Universität Wien' and the 'Technische Universität Wien' are participating in AURORA, thus covering the fields computer science, statistics and operations research, numerical mathematics, electrochemistry, and microelectronics. The major rationale behind the initiative of all partners to establish a *Special Research Field* in the area of High Performance Computing was the prospect of synergies arising from the cooperation between language, compiler, and tool designers as well as developers of numerical algorithms on the one hand, and designers of complex, state-of-the-art applications on the other hand.

Our contribution to AURORA deals with the parallelization of program packages for the simulation of semiconductor processes and devices. The focus is currently laid on the devel-

opment of a parallel version of the existing sequential Monte Carlo code for the simulation of ion implantation, which nowadays is the most important technique for introducing dopants into semiconductors. The Monte Carlo method, which has turned out to be the choice for simulations in all three spatial dimensions, exactly follows the physical process by sequentially calculating a high number of ion paths. Since up to some millions of trajectories must be calculated in order to obtain sufficiently accurate statistical information, an increase of the throughput — by means of parallelization — is an absolute necessity.

The current state of the project is represented by a message-passing version of the Monte Carlo code that distributes the simulation space to the nodes of a heterogeneous workstation cluster. Now, the main emphasis is laid on the implementation of a dynamic load balancing strategy, which results in a re-distribution of the simulation space. In addition, investigations for the use of High Performance Fortran as high level parallelizing language are performed in cooperation with the corresponding members of AURORA.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the 'Technische Universität Wien' in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik', first as a research assistant and then as assistant professor. His research field was first the numerical simulation of semiconductor devices and later the excitation and propagation of electro-acoustic waves in anisotropic piezoelectric materials where he also received his doctoral degree in 1986. In 1988 he joined the 'Institut für Mikroelektronik'. In April 1997 he received the 'venia docendi' on 'Microelectronics'.

Extraction of Parasitic Circuit Elements in Complex Structures

Rui Martins

In submicron technologies the interconnections between devices strongly influence the performance of integrated circuits. Interconnections also limit the maximum number of circuits that can be integrated in one chip. Thus, more and more attention toward modeling interconnections is required in the deep-submicron technologies.

The package SAP (Smart Analysis Programs) can extract parasitic capacitances, resistances and inductances of three-dimensional structures. These are entered manually (for very simple examples) or generated automatically from the layout of the circuit and a simple process description. The three-dimensional model is created by projecting the planar information of the layout into the third dimension associated with some thickness given in the process description.

This procedure has several drawbacks as it assumes that the actual structures closely follow the layout and are essentially planar. However, as we enter deep-submicron technologies, this is no longer true – there are deviations from the layout due to lithographic phenomena, and the more complex processes with a large number of metal layers can result in non-planar structures. To handle these cases we have linked the layout editor, VISTA's lithography and process simulators with SAP. With the layout information, the lithography package generates a new set of masks (distorted by imaging phenomena)

that are used in the patterning steps of the process simulators. After the last process step, the resulting structures are gridded conveniently to be used by SAP. As the parasitics have to be described with a circuit level model, it is possible to interactively specify net names and contacts with the layout editor (or generate them automatically). These names are consistently kept along all simulation phases in order to be annotated in the final net list according to the names given in the layout. The net list has a SPICE compatible syntax. An advantage of this approach is that it allows to interact layout, technology and circuit parameters with each other, so one can find the best global compromise.

Besides interconnection lines we have extracted capacitances of complex structures, namely those found in Dynamic Random Access Memories (DRAMs) storage capacitors. We are also using these tools to study microelectromechanical capacitive sensors and packaging thermal effects.

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Object-Oriented Model Management for for PROMIS-NT, MINIMOS-NT, and AMIGOS

Robert Mlekus

The increasing complexity of simulation tools combined with the requirement for shorter development cycles during the implementation of new models and algorithms raises a strong demand for object-oriented development tools and languages supporting the separation of simulators into modules which can be maintained without interfering with other modules. For that reason a new library-based concept has been developed, which provides an object-oriented approach to the implementation, parameterization and selection of models without any changes to the source code of the simulator.

The *Algorithm Library* is designed to support any kind of algorithm using arbitrary user-defined data structures as parameters, which are handled in their native C++ representation. It offers a set of C++ classes and methods to handle algorithms and parameters directly in C or C++ code and in the object-oriented *Model Definition Language* (MDL).

MDL can be used as an interpreted language (using a "just in time" byte code compiler) to facilitate the development of new algorithms, or – by using a two pass concept – as a compiler language to optimize the speed of simulations. Therefore, algorithms and data structures used in the innermost simulation loops can be handled by the mechanisms of the *Algorithm Library* with almost no performance loss compared to tradi-

tional function calls. Sets of models, appropriate parameter types and their operators and functions can be packaged into dynamic link libraries which can be loaded during run time and extended by additional models defined on the input deck by using MDL.

The *Algorithm Library* is used in various simulators and tools developed at the Institute for Microelectronics. Within the diffusion simulator PROMIS-NT the *Algorithm Library* provides the primary interface to control the simulation and specifies the coefficients of a general transport equation describing the impurity distributions. Furthermore, the process temperature function, and criteria for adaptation of the simulation grid can be specified by MDL. The device simulator MINIMOS-NT utilizes the *Algorithm Library* for the management of physical models. New models can be developed by subclassing a number of predefined models either in C++ or MDL and are automatically integrated seamlessly into the standard input deck of the simulator. The simulator AMIGOS (Analytical Model Interface & General Object-Oriented Solver) uses the *Algorithm Library* to manage precompiled models and to provide additional parameter and function definitions to be used in the input deck.

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Simulation of Heterojunction Bipolar Transistors

Vassil Palankovski

Heterojunction Bipolar Transistors (HBTs) attract much industrial interest nowadays. Accurate simulations save expensive technological efforts to obtain significant improvements of the device performance. Two major aspects are followed in our work on HBTs. First, MINIMOS-NT is extended to deal with different complex materials and structures, and to account for various important physical effects, such as band gap narrowing, surface recombination, and self heating. Second, the simulator is used within our TCAD framework for several simulation and optimization issues.

Recent work has emphasized on band gap narrowing as one of the crucial heavy-doping effects to be considered for bipolar devices. We have developed a new physically-based analytical band gap narrowing model, applicable to compound semiconductors, which accounts for the semiconductor material, the dopant species, and the lattice temperature. As the minority carrier mobility is of considerable importance for 0n-p-n bipolar transistors, a new universal low field mobility model has been implemented in MINIMOS-NT. It distinguishes between majority and minority electron mobilities on the one hand, and different dopant species on the other hand, both as a function of temperature and dopant concentration.

The simulator has been equipped with an extensive model library using a large material parameter database. Presently

it handles pure materials and binary alloys of group IV semiconductors, and binary and ternary III-V alloys with arbitrary material composition profiles.

Comparative analyses of different HBTs are important for studying device characteristics and are a prerequisite for any device optimization. In particular the electrical behavior of several devices has been compared: Si BJT and Si/SiGe/Si HBTs, Si/SiGe/Si HBTs and AlGaAs/GaAs HBTs, HBT and HEMT. For some of the devices a material composition and doping profile optimization has been performed at various temperatures. Using the automatic optimization tools of the VISTA framework the best figures-of-merit, such as maximum current gain and cutoff frequency have been obtained. Currently our work focuses on a comparison of AlGaAs/GaAs and InGaP/GaAs power HBTs.

Another important issue is device performance with respect to certain applications. In a comparative drift-diffusion and hydrodynamic mixed-mode simulation of an oscillator circuit, the capabilities of MINIMOS-NT have been demonstrated. We have shown that an accurate simulation of HBT circuits must account for non-local effects, such as velocity overshoot, and therefore requires the use of the hydrodynamic transport model.

Vassil Palankovski was born in Sofia, Bulgaria, in 1969. He studied electrical engineering at the Technical University of Sofia, where he received the degree of 'Dipl. Engineer' in 1993. Afterwards he worked for Siemens JV in Bulgaria for three years. He joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien' in May 1997, where he is currently working for his doctoral degree. His scientific interests include device and circuit simulation, heterostructure device modeling and physical aspects in general.

Optimization Aspects for TCAD Applications

Richard Plasun

Semiconductor technology essentially relies on the simulation of fabrication processes and electrical characterization. In recent times, the main goal when using TCAD tools has been to find those process parameters which give the best device performance. With the increasing availability of more and more powerful computation systems the number of variable parameters in performance analysis tasks is rising. For computer aided device optimization several modules are integrated into the framework.

One of the most important modules is the nonlinear constrained optimizer. It is working with a set of control parameters, handles multiple constraints and minimizes a given target function. The constraints and the target function are defined by arbitrary terms from the input parameters and the extracted parameters of the simulated semiconductor devices. The binding between the optimizer program and the framework is done by an agent which is even able to interact if the framework and the optimizer are running on different workstations. To speed up the overall computation time several extensions like a parallel calculation of the gradient of the target function and the constraints have been implemented. Together with the improved task handling and load balancing modules the framework builds a stable and efficient optimization environment. Hence, large optimization problems requiring several thousand evaluations can be performed.

New approaches using template-based device generation steps for the definition of analytical doping profiles have made a big step forward. Here the highly CPU time consuming process simulation steps are replaced by a short generation task. The electrical characterization is done with the device simulator MINIMOS-NT. For the gradient evaluations an initialization file is specified to improve the convergence behavior. In this case the simulator only needs a few iterations to find the solution of the next operating point.

To monitor the optimization progress a graphical user interface is included in the framework. It supports multiple plots in multiple windows with sophisticated zoom and move functionality. The controls, responses, constraints, and the target function are stored in a process database in order to allow the re-usage of this process knowledge.

Issues to be addressed in the near future are modules for fitting analytical doping profiles to simulated device structures. Based on the existing optimization and analysis capabilities, tasks like reverse engineering of doping profiles can be realized.

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Rigorous Three-Dimensional Topography Simulation

Wolfgang Pyka

Due to the decreasing feature sizes in today's semiconductor technology the inclusion of all relevant three-dimensional physical and geometric correlations becomes more and more indispensable for understanding and controlling the procedures which participate in the fabrication of integrated circuits.

Since three-dimensional simulations make high demands on system resources, the most important requirements for a three-dimensional topography simulator are accurate modeling within acceptable limits of memory consumption and efficient algorithms for remaining within reasonable CPU times. Moreover, three-dimensional solid modeling and geometry editing have to supply procedures for generating and manipulating the appropriate input geometries.

Much effort has been put on improving the efficiency of the algorithms included in the etching and deposition program ETCH3D. The speed of the surface movement algorithms has been increased by more than one order for isotropic etching/deposition and for sputter deposition by the introduction of linear and spherical segment structuring elements. By this means the time required for the surface propagation can be neglected and shadow testing, which has been optimized as well, has become the critical step with respect to CPU time.

The modeling of ballistic transport determined processes has been improved and supplies a great variety of distribution func-

tions for the particles arriving at the wafer surface. Simulations can be performed at arbitrary positions on the wafer taking into account the reactor geometry and the location of the sputter target. Several parameters are available for the adaption of the analytical functions to the process conditions and an auxiliary tool has been included for fast calculation of etch/deposition rates at specified locations of the geometry. These rates can be compared with experimental results, as, for example, film thicknesses in SEM pictures, and put into the program SIESTA, which optimizes the parameters of the distribution functions.

The function of solid modeling is taken over by the multiple geometry editor for cellular data (MGC). This program provides for the creation of initial structures, masking functions with simple geometric elements or with information from layout files, simple procedures for adding and removing materials and a low level model of chemical mechanical polishing. Two- or three-dimensional cutting operations for visualizing data from MGC or ETCH3D are also supplied.

Most recently a new treatment of the boundary conditions has been implemented. The conservation of the flatness at the boundaries of the topmost surface is now guaranteed even for slanted particle incidence.

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Three-Dimensional Simulation of Thermal Oxidation

Mustafa Radi

Thermal oxidation of silicon is a critical step in the fabrication of highly integrated electronic circuits and is mainly used for isolating adjacent devices from each other. Knowledge of the physical processes that affect thermal oxidation is essential for optimizing applications.

Miniaturization of devices based on silicon technology leads to the realization of integrated structures exhibiting an increasingly complex topology. In order to reduce the development duration of state-of-the-art technologies, two- and three-dimensional process simulation capabilities are of prime interest. Difficulties in numerical modeling of silicon oxidation arise from the necessity to ensure both a wide prediction capability and a very flexible numerical solution. Accurate modeling requires the knowledge of the mechanical thin film properties of integrated circuit materials as well as stress effects of the oxidation kinetics. The efficiency of the numerical implementation depends on the ability to handle complex topological configurations within reasonable computing time.

To cope with these different requirements the extremely flexible simulator AMIGOS (Analytical Model Interface & General Object-Oriented Solver) has been developed. It is a problem-independent simulation system which can handle various nonlinear partial differential equation system in time and space in either one, two or three dimensions. There are no restrictions

whether using scalar-, field- or even tensor quantities within a model, and, if desired, any dependent field quantity can be calculated. Furthermore, the user can influence the numerical behavior of the differential equation system through complete control of the residual vector and its derivative by, for example, punishing terms or damping terms. Even interpolation and grid-adaptation formulations can be specified within a developed model and can be adapted to a particular problem very well.

With AMIGOS, a new approach to the local oxidation in three dimensions has been developed, based on a parameter-dependent smooth transition zone between silicon and silicon-dioxide. The resulting two phase problem is solved by calculating a free diffusive oxygen concentration and its chemical reaction with pure silicon to silicon-dioxide. This effect causes a volume expansion that leads to mechanical stress affecting the surrounding boundary conditions. With a suitable set of parameters this approach is equivalent to the standard sharp interface model based on the fundamental work of Deal and Grove.

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Simulation of AVC Measurements

Martin Rottinger

The development of new semiconductor devices and the down scaling of proven designs increases the demands on accurate positioning of the doping and creates a need for new methods to measure the doping distribution. One of the recently developed electronic properties probing techniques is the Auger Voltage Contrast (AVC) method.

In the AVC method a beam of high energetic electrons is focused on the surface of a cross-sectioned test device. The device is connected to ground voltage by a contact. The incident electrons generate electron-hole pairs in the semiconductor and a fraction of the secondary electrons has enough kinetic energy to leave the semiconductor.

The built-in potential causes a band bending which is a function of the doping. The kinetic energy of the emitted secondary electrons is measured and compared to the energy of electrons emitted from an undoped semiconductor. The difference in the observed kinetic energy corresponds to the band bending caused by the doping, the presence of surface states, and the interaction of the probing electron beam with the device.

AVC measurements are quite time-consuming and need specialized equipment. Therefore, the simulation of such measurements is a valuable tool for the development and improvement of procedures for the automatic delineation of the pn-junction and extraction of doping distributions from the measurement

data and for gaining a better understanding of the physical effects involved.

Simple analytical approximations describing the interaction of the electron beam and the semiconductor break down for beam current densities used in real measurements. Therefore, the semiconductor equations have to be solved numerically to calculate the surface potential. The device simulator MINIMOS-NT has been enhanced to be capable of simulating such measurements.

Appropriate models have been added to the simulator to account for the injection of electrons by the electron beam and the electron-hole pair generation caused by the incident high energy electrons. The effects of surface states have been neglected because they are important only for small beam currents.

After performing a simulation using MINIMOS-NT the surface potential is extracted at the center of the distribution of the injected electrons and generated electron-hole pairs. The simulation of an AVC scan requires a number of simulations of the same device with varying locations of the injected electrons and of the generated electron-hole pairs.

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Accurate Three-Dimensional Interconnect Analysis with SAP

Rainer Sabelka

As the performance of VLSI circuits is increasingly limited by interconnect properties, accurate three-dimensional interconnect models have become essential to chip and system design. An accurate extraction of parasitic resistances and capacitances, the calculation of crosstalk, and signal delay caused by interconnections are the most important issues. In addition, from the viewpoint of circuit reliability, the knowledge of the current density and temperature distribution in the wiring structures are important to prevent electromigration. Measurements are difficult and time-consuming and sometimes impossible at all, especially on-chip. While analytical models supplied by conventional ECAD tools prove as too inaccurate for complex geometric structures, only a fully three-dimensional simulation approach can supply the required accuracy.

The program package SAP (Smart Analysis Programs) has been developed for these reasons. The simulators of this package are based on the finite element method and can be used for highly accurate capacitance extraction, resistance calculation, transient electric and coupled electro-thermal simulations. Furthermore, three input preprocessors are available for two- and three-dimensional geometry specification and for automatic grid generation.

In the new transient electric simulation mode the evolution of the potential distribution inside and between the intercon-

nects is calculated with the finite element method and a Crank Nicholson time discretization. This mode is used for the calculation of delay times on interconnections, capacitive crosstalk and substrate coupling more accurately than with lumped or transmission line models.

The practical usability of the programs has been enhanced. The command line interface has been redesigned, large grid files are stored in a compressed file format, the manual has been revised and online-help is available.

The interactive user interface of the visualization tool SV has been extended and a mode for displaying vector type attributes, such as current density and heat flow distributions, has been added.

The solid modeler and grid generator LAYGRID uses a layer-based method for automatic three-dimensional meshing. To further enhance the quality of the generated grid the fully unstructured grid generator DELINK by Peter Fleischmann is now also available within LAYGRID.

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High-Performance Low-Power Technology

Gerhard Schrom

In the past decade Moore's law – the doubling of performance every 18 months – has remained valid. Behind the scenes, however, the way of technology development has changed dramatically from constant-voltage scaling to a constraint-based scaling scenario, where the supply voltage is reduced every few generations. In the Technology Roadmap of the Semiconductor Industries Association (SIA) of 1997 the projected supply voltage for the 70nm technology generations was set to 0.6–0.9V, as opposed to 0.9V projected in the Roadmap of 1994, and to 0.5–0.6V for 50nm gate length.

Ultra-Low-Power (ULP) CMOS, on the other hand, has demanded even lower supply voltages (about 0.2V) and higher drain leakage in order to minimize the power consumption while keeping up the performance. It can be shown that for a typical high-performance CPU the optimum tradeoff between performance and power efficiency is achieved by setting the leakage-to-drive current ratio $I_{off}/I_{on} \approx 10^{-2}$. This means leakage currents of several 100nA/μm at supply voltages of a few 100mV.

A major focus of the research activities in the field of ULP CMOS is to investigate the operation of devices, circuits, and systems under such extreme conditions and to develop reliable methods and tools for quantitative characterization, such as accurate device models and VLSI performance metrics. The same methods are also well-suited for the characterization of future low-voltage high-performance CMOS technology gener-

ations, where standard methods often fail, especially for explorative device studies, which are carried out to investigate the whole range from ULP to high-performance CMOS technology.

Another important area of low-power research is to investigate the options for interfacing to the analog world, which plays an important role especially in portable electronics. The feasibility of low-voltage op-amps and even switched-capacitor circuits operating at $V_{DD} < 0.5$V could be demonstrated using high-precision circuit simulations with MINISIM. However, the most promising approach for mixed analog digital applications is to employ analog-to-digital conversion (ADC) and to do most of the signal processing in digital. Not only is this strategy more efficient for expensive high-quality signal processing, it is also fully compatible with digital ULP CMOS technologies. It could be shown that sigma-delta converters work perfectly down to $V_{DD} = 0.2$V. In normal operation any nonlinearities are turned into white noise, which can be controlled by oversampling and noise shaping. A second-order noise shaping sigma-delta ADC designed in a 0.13μm ULP CMOS technology with an input signal bandwidth of 1MHz has yielded a dynamic range of 70dB.

Gerhard Schrom was born in Mödling, Austria, in 1963. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in March 1992. During his studies he was working on software development projects in the CAD field. He joined the 'Institut für Mikroelektronik' in April 1992, where he currently works for his doctoral degree. His research interests include device and circuit simulation, circuit design and synthesis, signal and image processing, and TCAD framework aspects. In spring 1994 he held a visiting research position at HITACHI, Tokyo, Japan. In summer 1997 he held a visiting research position at INTEL, Hillsboro OR, USA.

Asymmetrical MOS Device Structures

Michael Stockinger

The ever increasing demand for speed enhancement and higher device densities on the chip imposes a big challenge for CMOS process and device designers. New device structures have to be found to overcome imminent problems, such as leakage currents, short-channel effects, punchthrough, and DIBL (Drain Induced Barrier Lowering).

In the past various structures have been suggested to improve the device performance for VLSI design down to 0.1 μm gate length. Up to now symmetrical device structures have been exploited because of their inherent manufacturing simplicity. In the future this practice will be abandoned because asymmetrical doping structures can meet the given performance requirements more easily. However, manufacturing processes will have to be adjusted to the new device structures.

Our recent optimization of a MOS acceptor doping profile has delivered an asymmetrical device with a narrow doping peak at the source side of the channel. This simulation-based optimization — we have used MINIMOS-NT for device simulation and VISTA as the optimization framework — was performed to maximize the drive current while keeping the drain-source leakage current below 1 pA/μm. The drive current compared to a uniformly doped device was 48% higher for the 0.25 μm structure and 80% higher for the 0.1 μm structure.

These improvements can be attributed to the reduction of the effective gate length. The doping peak divides the channel

into a highly doped region and a lightly doped one. Therefore, for modeling purposes the device can be separated into two devices in series, one with a high threshold voltage and the other with a very low one (enhancement type and depletion type, respectively). The depletion type device acts only as a series resistor with low resistance whereas the enhancement type device determines the effective gate length and therefore the overall performance.

A two transistor compact model using analytical functions to describe the device behavior can be used to explain the physical background of the performance improvements. Shorter devices can deliver a higher drive current at the same drain-source leakage, but a lower bound for the gate length exists where the DIBL effect becomes relevant. Below this bound which, in this case, depends on the supply voltage and the allowed leakage current, no further drive current improvements could be observed.

Optimization processes for other performance goals like the gate delay time of a CMOS inverter or the natural frequency of a multistage ring-oscillator will be performed. As for the drive current optimization, asymmetrical device structures are expected as a result.

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Simulation Methodology for Semiconductor Technology Analysis

Rudolf Strasser

TCAD frameworks have become very important for the industrial application of technology simulation tools. Since the overall time to carry out simulations has to be minimized, an efficient simulation methodology has to be provided which strongly supports a TCAD engineer in organizing his simulations. Furthermore, a TCAD engineer needs the flexibility to use his personal favorite tools in a simple, transparent way.

Therefore, the existing capabilities of the VISTA Simulation Flow Controller (SFC) have been redesigned and straightened. All of the existing features, such as flow representation, input deck templates, split checking, parallel and distributed job execution, and load balancing have been preserved and are available in a more transparent way. A critical issue is the integration interface for simulation tools. A novel tool interface offers integration for tools with an arbitrary number of input deck templates, and an arbitrary command line. Simulation results have to be declared by specifying their type and assigning them a name, and these results are available for the following tool. The type of simulation results has to be one out of a library of available data types including files, data values, I/V curve sets and the like. Thus, arbitrary simulation tools as well as auxiliary tools can easily be incorporated in a simulation flow, without any need for coding.

One of the most challenging TCAD experiments is optimiza-

tion. Especially the simulation of coupled systems, such as the N-MOS device and the P-MOS device, raises the demand for a sophisticated simulation methodology. One can imagine that the optimization of the N-MOS device could easily degrade characteristics of the P-MOS device, and vice versa. The VISTA TCAD framework offers a mechanism to simultaneously optimize both devices in a single optimization process. A composite model, employed by the optimizer, allows for the combination of the models which represent both devices in a very simple way. This approach is not limited to two devices, but provides a general mechanism to combine several simulations in a single one.

Due to the large number of tool invocations the efficient usage of all the available computing resources is very important. VISTA job farming with its integrated load balancing mechanism offers an ultimate front end to a cluster of workstations. By means of load balancing each job is scheduled to a computer which promises a minimum of computation time.

Rudolf Strasser was born in Ried im Innkreis, Austria, in 1970. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1995. From spring 1992 to autumn 1993 he held a research position at the campus-based Engineering Center of Digital Equipment Corporation, Vienna, Austria. He joined the 'Institut für Mikroelektronik' in April 1995. In summer 1996 he was with the Advanced Products Research and Development Laboratory at Motorola, Austin, USA. He is currently working for his doctoral degree. His scientific interests include semiconductor technology, grid generation and software engineering.

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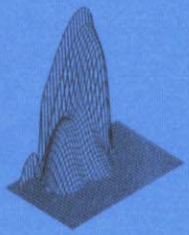

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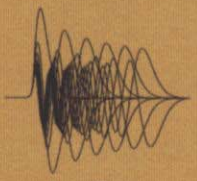

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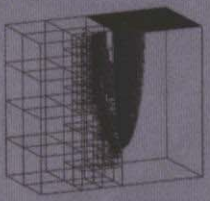

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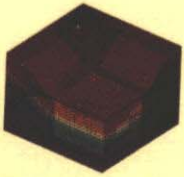

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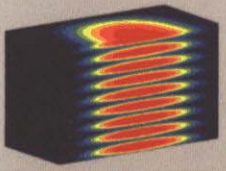

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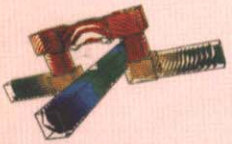

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