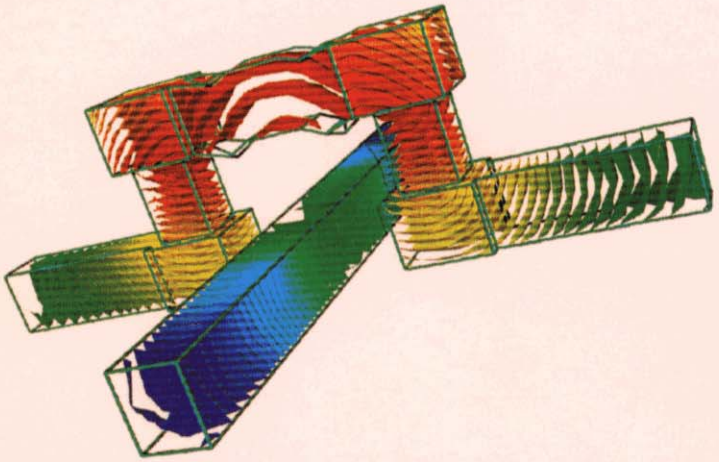
TU

TECHNISCHE
UNIVERSITÄT
WIEN



Annual Review
June 1997

INSTITUTE
FOR MICROELECTRONICS

ANNUAL REVIEW

JUNE 1997

INSTITUT FÜR MIKROELEKTRONIK
Technische Universität Wien
Gußhausstraße 27 – 29
A – 1040 Wien
AUSTRIA

http://www.iue.tuwien.ac.at/
Tel: *43/1/58801/3850
Fax: *43/1/5059224

Staff

Thomas Binder	Dipl.–Ing.	(March 1, 97–)
Walter Bohmayr	Dipl.–Ing., Dr.techn.	(–Nov. 30, 96)
Peter Fleischmann	Dipl.–Ing.	
Tibor Grasser	Dipl.–Ing.	
Ewald Haslinger		
Andreas Hössinger	Dipl.–Ing.	(July 1, 96–)
Erwin Hollensteiner	Dipl.–Ing.	(Sept. 1, 96)
Goran Kaiblinger-Grujin	Dipl.–Ing.	
Manfred Katterbauer		
Heinrich Kirchauer	Dipl.–Ing.	
Martin Knaipp	Dipl.–Ing.	
Christian Köpf	Dipl.–Ing.	
Hans Kosina	Dipl.–Ing., Dr.techn.	
Erasmus Langer	Univ.Doz., Dipl.–Ing., Dr.techn.	
Ernst Leitner	Dipl.–Ing.	
Rui Martins	Mestre	
Robert Mlekus	Dipl.–Ing.	
Vassil Palankovski	Dipl.–Ing.	(May 1, 97–)
Christoph Pichler	Dipl.–Ing., Dr.techn.	(–March 31, 97)
Richard Plasun	Dipl.–Ing.	
Wolfgang Pyka	Dipl.–Ing.	(Dec. 1, 96–)
Mustafa Radi	Dipl.–Ing.	
Martin Rottinger	Dipl.–Ing.	
Rainer Sabelka	Dipl.–Ing.	
Gerhard Schrom	Dipl.–Ing.	
Siegfried Selberherr	O.Univ.Prof., Dipl.–Ing., Dr.techn.	
Thomas Simlinger	Dipl.–Ing., Dr.techn.	(–April 30, 97)
Andreas Stach	Dipl.–Ing.	(–Sept. 30, 96)
Michael Stockinger	Dipl.–Ing.	(Feb. 1, 97–)
Rudolf Strasser	Dipl.–Ing.	
Christian Troger	Dipl.–Ing.	
Walter Tuppa	Dipl.–Ing., Dr.techn.	(–Dec. 31, 96)
Christoph Wasshuber	Dipl.–Ing., Dr.techn.	(–Sept. 30, 96)
Renate Winkler		

Contents

Staff 1

Preface 4

Fields of Research 6

Design of an Object-Oriented Wafer State Data Model 6

Three-Dimensional Mesh Generation for Applications in Technology CAD 8

Powerful Control Language for MINIMOS-NT 10

Multi-Dimensional Simulation of Ion Implantation . . 12

Diffusion and Oxidation Models 14

A New Approach of Modeling the Electron Mobility Dependence on Dopant Species 16

Photolithography Simulation 18

Substrate Current Simulation with MINIMOS-NT . . 20

Modeling of Heavy Doping Effects in Compound Semiconductors 22

Physical Model Development for Advanced Device Simulation 24

Parallelization of Program Packages for the Simulation of Micro-Structures 26

Three-Dimensional Simulation of Dopant Diffusion . 28

Using Layout Data in the VISTA Framework 30

Object-Oriented Management of Algorithms and Models 32

Simulation of Heterojunction Bipolar Transistors . . . 34

High-level Optimization Tasks in the VISTA TCAD Framework 36

Three-Dimensional Simulation of Etching and Deposition Processes 38

Three-Dimensional Simulation of Thermal Oxidation 40

Generation of Triangular Grids in MINIMOS-NT . . 42

SAP — A Finite-Element Package for Interconnect Simulation 44

VLSI Technology Optimization 46

Optimization of MOS Device Structures 48

Advanced Analysis of Semiconductor Processes Using VISTA 50

Modeling Non-Parabolicity Effects in Quantized Systems 52

Publications **54**

Industrial Sponsors **62**

Preface

Siegfried Selberherr

This brochure is the ninth annual research review of the Institute for Microelectronics. The staff financed by the Austrian Federal Ministry for Science and Transport consists of nine full time employees: the head of the institute, five scientists, a secretary and two technical assistants. Twenty additional scientists are funded through scientific projects supported by our industrial partners.

This year we can report participation in a new ESPRIT project which is directly funded by the European Union, namely PROMPT II[1], a follow-up project made possible by the success of the ESPRIT PROMPT project finished last year. We are glad to report that all our industrial partners from last year's review have continued to support our institute. In addition we have started cooperative research with two more industrial partners, namely INTEL in Hillsboro, USA and NEC in Sagamihara, Japan, of which we are very proud.

The projects of the institute are, in a continuation of our previous work, focused on microelectronics modeling issues. Technology Computer-Aided Design (TCAD) is the phrase which is commonly used for this kind of activity these days. We are quite satisfied with our academic and scientific output. Particularly pleasing is an all-time-high number of contributions and participations in international conferences and the habilitation

[1]Process Optimization in Multiple Dimensions for Semiconductor Technology II

of one member of the institute. We are entering the tenth year of our institute with considerable motivation.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplom-ingenieur' in electrical engineering and the doctoral degree in technical sciences from the 'Technische Universität Wien' in 1978 and 1981, respectively. Since that time he has been with the 'Technische Universität Wien' as professor. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. He has been the head of the 'Institut für Mikroelektronik' since 1988. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of the organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Design of an Object-Oriented Wafer State Data Model

Thomas Binder

Many different problems which must be solved in the simulation environment of a modern semiconductor fabrication process require a rather large number of individual programs, each dedicated to a certain functionality, e.g. simulating a particular process step. Usually the output of one tool has to be used as input for another, which raises the need to exchange data between the programs. The current solution to this problem is to use the *profile interchange format* (PIF) as file format common to all tools involved in the simulation process. By providing a set of access functions to this file format as well as visualization and editing tools, details of the PIF are well hidden from the user.

To improve performance and usability, a new object-oriented data model is being developed. This model has to be capable of holding all the data needed to describe a wafer state. Since most of the simulators already use grid-based data structures internally, this is an obvious way to store structural data and attributes such as material constants, distributed quantities and the like. When geometrical manipulations are desired, consistency considerations have to be taken into account, and rules to repair a grid (re-grid) according to geometry deformations have to be defined. A way of implementing an efficient grid-based data structure is a finite oct-tree, which has the advantage of implicit support for solid modeling functions. Of course it is not quite easy to define appropriate re-gridding

rules, since each application requires different grid parameters and properties. Another requirement of a wafer state data model is concurrent data access. Since it is desirable that one user is visualizing data produced by another (e.g. to watch the progress of a certain simulation process), care must be taken not to produce an inconsistent state of data at any given time. Furthermore, in a network-based computer environment, a user does not want to be concerned with the physical location the simulations take place. Therefore, networking aspects must be dealt with in an appropriate way.

Another important task of an abstract data layer is to manage results of many different simulation runs. One can either keep a bunch of individual files or a database can be used to organize file names. The database approach has the advantage that the history of results can be handled very easily, and the user does not have to concern himself with (operating-) system specifics like time stamps or similar aspects. Usually a database is running on a dedicated server, therefore efforts for 'data house-holding' are kept at a minimum.

Thomas Binder was born in Bad Ischl, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in December 1996. During his studies he was working on several software projects mainly in the CAD, geodesy and security fields. In March 1997 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. His scientific interests include data modeling, algorithms, software engineering and semiconductor technology in general.

Three-Dimensional Mesh Generation for Applications in Technology CAD

Peter Fleischmann

Three-dimensional process and device simulation have grown importance and have created the need for three-dimensional mesh generation in Technology CAD (TCAD). This development began to evolve from other disciplines such as computational mechanics and computational fluid dynamics, where a vast amount of experience in three-dimensional meshing is available. This knowledge should be utilized and adapted for the meshing tasks evolving in TCAD applications. The demands on meshing differ in TCAD and computational mechanics and fluid dynamics applications differ. Typical for semiconductor simulation purposes are extreme ratios between the size of the smallest and the largest features, where no structural simplifications can be afforded. The complexity of the simulated structures with many material segments and their interfaces and the time-dependent topology pose an increasing challenge.

The popularity of automation has lead to a better understanding of the important balance between automation and control to interactively bring in engineering judgement. However, in some cases one will strive for the utmost degree of automation facing one of the big challenges within a TCAD integrated system: The design and construction of a geometry can itself be the result of an automated analysis procedure. The structure is not derived from an input modeler or editor, instead it is the result of a topography simulation or an oxidation step during

process simulation. The automatic preprocessor would complete this integrated system and enable the fast and efficient optimization of various design and manufacturing parameters.

The input model subject to e.g. finite element analysis can be defined in two ways. Constructive solid geometry uses nodes and solids to define a structure (volume-oriented inputs). Alternatively, the same structure can be defined by its enclosing surface through nodes and polygonal elements (surface-oriented inputs). The conversion of the CAD input model to yield a meshable boundary representation can be a non-trivial process. It calls for a transformation of the input data to provide the mesher with more and/or different information on the geometry. It is easier to feed a volume-oriented mesher with a volume-oriented input model e.g. allowing topologies which are not well connected. If a cellular input model is used (e.g. from a cellular solid modeler) and CPU time is a minor concern, it can be considered to use the model directly as the mesh.

Another important issue is CAD data repair. The input model can contain a wide variety of inconsistencies harmless for visualization purposes but crucial for any meshing algorithm. In such cases one might be dependent on powerful interactive tools to resolve the problem areas.

Peter Fleischmann was born in Kabul, Afghanistan, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994. He is currently working for his doctoral degree. His research interests include mesh generation as well as algorithms and data structures in computational geometry.

Powerful Control Language for MINIMOS-NT

Tibor Grasser

A complex, general purpose device and circuit simulator such as MINIMOS-NT makes heavy demands on its controlling language. In fact, a simple input deck as the collection of static keywords is not sufficient. Even if these keywords are allowed to be functions, tables, or other complex objects, the burden of evaluation lies on the simulator. Normally, to control complex simulations such as hydrodynamic transient mixed mode simulations, dozens of keywords are introduced to cover all possible events. For instance, if the convergence fails, several decisions for continuation are imaginable.

In the case of MINIMOS-NT a different approach has been taken. The main idea is to limit the number of keywords, which are grouped in so-called sections. These keywords are allowed to be time-dependent functions, tables, expressions and the like. To accomplish this, the input deck is handled as a database which is only queried when the desired keyword is required. The simulator stores internal variables which should be externally accessible in a special section. These external variables (e.g. iteration counter, different update norms) can then be used to form keyword expressions in the input deck. When the simulator inquires a special keyword from the input deck, its current value is automatically returned.

The entire input deck functionality has been implemented as a library to handle the complex situations which can arise. This

library can be customized to special needs since external functions written in the programming language C can be added to the internal function list of the input deck library. These external functions can be used like any other function for every keyword. This feature is used for the inclusion of point clouds, general data tables stored in an ASCII file. Due to this powerful feature, the functionality of the simulator increases without the need to change one line of the simulator code. For instance, the contact voltage of every voltage source can be given as a general function of time.

Another case where these features are utilized is the control of block iteration. Especially hydrodynamic simulation requires such a great flexibility, because convergence is usually hard to achieve. For the definition of each of these iteration blocks, one section of the input deck exists. For each block several keywords such as the list of quantities to be solved, the damping scheme to be used, parameters for this damping scheme, and a stop expression are supplied to control the iteration. These sections can be arbitrarily nested, forming complex sequences of iteration blocks.

Tibor Grasser was born in Vienna, Austria, in 1970. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1995. He joined the 'Institut für Mikroelektronik' in April 1996, where he is currently working for his doctoral degree. His scientific interests include circuit and device simulation, device modeling and physical aspects in general.

Multi-Dimensional Simulation of Ion Implantation

Andreas Hössinger

In VLSI technology ion implantation has turned out to be the primary technology to introduce dopant atoms into semiconductors. Because of the large variety of applications and the small device dimensions it is important to provide flexible and multi-dimensional simulators. There are basically two different methods for the simulation of ion implantation. Firstly, an analytical method representing the doping profile by probability functions with probability moments depending on various implantation parameters. We use dependences on ion species, energy and dose. Secondly, the Monte Carlo method, which follows all ions on their way through the device until they come to rest at their final position or leave the simulation domain. The analytical simulator can handle two-dimensional problems whereas the Monte Carlo simulator can be used to solve problems of arbitrary dimension.

In order to improve the quality of the results of a two-dimensional simulation run within our TCAD-Framework VISTA we have implemented the use of triangular grids into the simulators. Previously it was necessary to interpolate the doping output of an implantation step, which was given on an ortho-product grid, to the triangular wafer state grid that is used by all other simulators. Now the implantation simulators are able to read the wafer state grid and calculate a doping concentration for all grid points. Furthermore they are able to refine the grid within regions where the resolution of the grid

is not appropriate to meet the requirements of the refinement criteria. We use a dose-, a gradient- and a grid density grading criterion, which means that the dose error has to be below a certain threshold, that the gradient of the concentration between two grid points must not exceed a given limit, and that the proportion of the areas of two adjacent triangles is limited.

Another important motivation in the simulation of ion implantation is the determination of damage in silicon crystal. This is important because self-interstitials and vacancies in the crystal can significantly influence the subsequent diffusion process, but it is impossible to measure the crystal damage directly. Under these circumstances we have started to expand the Monte Carlo simulator in order to be able to calculate not only single atomic ions, but also molecular ions. The motivation to do so was that BF_2 is widely used to implant Boron, but the damage profile is not accurate enough if we only scale the energy and modify the recombination rate of a Boron implantation.

Andreas Hössinger was born St. Pölten, Austria, in 1969. He studied technical physics at 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in January 1996. He joined the 'Institut für Mikroelektronik' in June 1996. He is currently working for his doctoral degree. His research interests include process-simulation with special emphasis on the simulation of ion implantation.

Diffusion and Oxidation Models

Erwin Hollensteiner

The technological importance of the diffusion and the oxidation process steps for integrated circuits is the major driving force for the study of these processes. Nowadays it is necessary to compute effects such as clustering, coupled diffusion, segregation, mechanical stress, or transient enhanced diffusion. Models computing these effects, have been created for implementation in the flexible simulator named AMIGOS. Additionally, one-dimensional and two-dimensional boundary models specify and compute the boundary conditions.

The coupled diffusion model describes the dopant movement based on extrinsic dopant diffusion. It assumes that the dopants are driven by the concentration gradients and the electric field which acts on all charged particles. The electric field is calculated from the built-in potential, hence local charge neutrality and Bolzmann statistics are assumed.

At high concentrations not all dopant atoms are ionized due to clustering and precipitation. The total concentration of an impurity will be made up of a mobile part and an immobile part. This cluster formation causes a drastic reduction of the diffusion coefficient at high concentrations because the gradient of the active atoms almost vanishes and the clustered part of the dopants does not diffuse. Two models for clustering are supplied, a kinetic (dynamic) clustering model and an equilibrium (static) clustering model.

Segregation of impurity or point defect species occur concur-

rently in inhomogeneous materials or material interfaces. Generally, the silicon/silicon dioxide interface is of vital importance for process development. A model simultaneously describing the species diffusion and segregation behavior has been developed. Segregation phenomena occur because the Gibbs free energy of formation of a point defect or impurity species is different in the different material regions.

Numerical simulation of local oxidation of silicon is becoming increasingly important in enhanced technologies. For this reason, numerical models of the oxidation process are being developed. The models are natural extensions of the classical Deal and Grove model, but instead of using a sharp interface description a smooth transition zone between silicon and silicon dioxide is calculated. Because of this kind of modeling the mesh remains topologically invariant during the process of oxidation and therefore no remeshing is necessary.

Erwin Hollensteiner was born in Krems, Austria, in 1973. He began to study electrical engineering at the 'Technische Universität Wien' in 1992, where he received the degree of 'Diplomingenieur' in March 1996. He joined the 'Institut für Mikroelektronik' in September 1996, where he is currently working for his doctoral degree. His scientific interests include process-simulation, general diffusion and oxidation processes.

A New Approach of Modeling the Electron Mobility Dependence on Dopant Species

Goran Kaiblinger-Grujin

As semiconductor device dimensions decreasingly approach 0.1 μm, it becomes necessary to have accurate values of the majorityand minority electron mobilities in advanced semiconductor device simulation. Despite the importance of these quantities for device applications such as bipolar transistors which are controlled by minority carrier flow in heavily doped regions, theoretical treatments are quite limited. There still remains a tendency in numerical simulation to assume that majority and minority mobilities are equal, although experiments have shown that majority and minority mobilities may differ by up to one order of magnitude in heavily doped silicon.

Moreover, there is no theoretical model to date which explains the different mobility data for As- and P-doped silicon for impurity concentrations higher than $10^{18}\,\mathrm{cm}^{-3}$. The difference between the electron mobility in As- and P-doped samples monotonically increases from 6 % at $N_I = 10^{19}\,\mathrm{cm}^{-3}$ up to 32 % for $N_I = 4 \cdot 10^{21}\,\mathrm{cm}^{-3}$. Ignoring these phenomena can lead to an incorrect interpretation of device data which strongly depend on doping concentration.

We are presenting a new theoretical approach which enables us to study the dependence of the electron mobility on the dopant species. The valence electron charge distribution of the impurities is calculated by the Thomas-Fermi theory in the energy functional formulation. Ionized impurity scattering has been

treated within the Born approximation. Our model, which is implemented in MINIMOS 6, accounts for degenerate statistics, dispersive screening and pair scattering, which become important in heavily doped semiconductors. The dielectric function is accurately approximated by a rational function. A new expression for the second Born amplitude of a Yukawa-like charge distribution is derived, which now depends on the atomic and electron numbers of the impurity ion.

Calculations have been performed in n- and p-doped Si, GaAs, and InP at 300 K. The agreement with experimental data is excellent. The results do not only confirm the experimental data of the mobility enhancement of minority electrons in degenerate p-Si, but also the lower electron mobility in As- and Sb-doped silicon in comparison to P-doped Si. While we are predicting a strong impact of the form factor on the mobility for n-doped degenerate GaAs and InP, we have found no dopant dependence on the mobility in p-doped compounds.

Goran Kaiblinger-Grujin was born in former Yugoslavia, in 1967. He began to study physics at the 'Technische Universität Wien' in 1988, where he received the degree of 'Diplomingenieur' in June 1993. From July 1993 to Feb. 1994 he worked as a technical consultant with an oil company. After his civil service he joined the 'Institut für Mikroelektronik' in January 1995. From July to Sept. 1996, he held a position as visiting researcher at the University of California, Berkeley working on physical mobility models. He is currently working for his doctoral degree. His scientific interests include semiconductor physics and device simulation.

Photolithography Simulation

Heinrich Kirchauer

An overall three-dimensional photolithography simulator accounting for all of the three lithography subprocesses of mask imaging, resist exposure/bleaching and resist development has been developed. The simulator consists of three modules, each of which has been specialized on one subprocess.

The imaging part describes the illumination of the mask. The light transmission through the optical system including the mask is simulated. The output of the imaging module is the aerial image, which is the light intensity incidenting on the wafer. Our approach combines the vector-valued version of the classical scalar theory of Fourier optics with a semi-analytical algorithm for calculating the mask's Fourier coefficients. Using this algorithm the aerial image can be determined without any aliasing errors due to mask sampling. Binary as well as phase-shift masks can be simulated. To account for partial coherent and off-axis illumination an arbitrary distributed light source is considered. The discretization of the light source is accomplished in a way to ensure a numerically efficient exposure simulation.

The exposure/bleaching module simulates the chemical reaction of the resist. The light propagation within the photosensitive resist and the electromagnetic scattering effects due to a nonplanar topography have to be modeled. The result of the exposure/bleaching module is the latent bulk image. Our approach is based on a numerical solution of the Maxwell equations and is thus the physically most rigorous one. The

bleaching reaction is described by the Dill model. Applying a quasi-static approximation, the nonlinear problem is transformed into multiple inhomogeneous but linear problems. Due to the linearity and an assumed periodicity of the simulation domain the electromagnetic field can be represented by Fourier series. Insertion of the expansions into the Maxwell equations transforms the partial differential equations into a system of ordinary differential equations for the field's Fourier coefficients. According to Sommerfeld's radiation conditions boundary conditions on top as well as at the bottom of the simulation domain have to be established. Hence, we have a two-point boundary value problem, which we solve with a shooting-method-like algorithm. This algorithm has the great advantage that the number of vertical discretization points does not influence the memory requirements and thus enables a rigorous three-dimensional workstation-based simulation. Furthermore, the additional costs due to the partial coherent illumination reduces the multiplication of the right hand sides in the final algebraic system. Hence, a rigorous simulation of nonplanar scattering effects in combination with partial coherence becomes possible. The development process is simulated with the etching tool of the VISTA framework to obtain the final resist profile.

Heinrich Kirchauer was born in Vienna, Austria, in 1969. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in March 1994. After his studies he worked on a research project about statistical signal processing at the 'Institut für Nachrichtentechnik' for six months. In December 1994 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. His scientific interests include three-dimensional process simulation with special emphasis on lithography simulation.

Substrate Current Simulation with MINIMOS-NT

Martin Knaipp

The substrate current in a standard MOSFET depends on the voltages applied to gate and drain. It can also be shown that the amount of substrate current is an indicator of the transistor lifetime. If the substrate current gets higher, the lifetime of the device is reduced. Therefore, accurate modeling of the substrate current and the resulting optimization of the device doping are important factors for increasing the device lifetime.

Let us consider the substrate current in case of a n-MOSFET. At low gate voltage but high drain voltage the maximum electric field under the gate is high. The electrons obtain their maximum average temperature near this high field region which is located close to the pn-junction. High temperature electrons can cause impact ionization, generating electron-hole pairs. The generated electrons are pushed towards the drain whereas the holes drift to the bulk contact, contributing to the substrate current. Therefore, the amount of substrate current is an indicator of the number of the hot electrons under the gate. Usually hot electrons are unwelcome because – despite impact ionization – they can damage the gate oxide. This leads to the well known degradation of the MOSFET. At low gate voltage but high drain voltage the average electron temperature in the region of interest is highest but the number of available electrons is low. This finally leads to a small substrate current.

When the gate voltage increases, the maximum electric field under the gate decreases, which leads to a lower average electron temperature. At the same time the number of available electrons is much higher because of the higher gate voltage, which finally leads to a much higher substrate current. When the gate voltage is as high as the drain voltage, the maximum electric field is lowest but the number of electrons reaches a new maximum value. The small electric field leads to a low average electron temperature which is often below the threshold energy of impact ionisation. At this operation point only few electrons reach higher temperatures so that they can perform impact ionization. This again causes a very small substrate current. Note that in this operation area the source-drain current increases but the substrate current decreases.

In our device simulator MINIMOS-NT, the newest hydrodynamic impact ionization models were implemented to simulate substrate currents on a physically motivated basis. Only the carrier temperatures and the carrier densities are used to calculate the generation rates for electrons and holes. The phenomena of carrier cooling by the impact ionization process and the additionally generated carriers are considered in a self-consistent way.

Martin Knaipp was born in Vienna, Austria, in 1966. He studied technical physics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. In August 1994 he joined the 'Institut für Mikroelektronik', where he is working for his doctoral degree. His work is focused on device simulation, especially on high temperature effects. In autumn 1996 he held a visiting research position at Hitachi, Tokyo, Japan.

Modeling of Heavy Doping Effects in Compound Semiconductors

Christian Köpf

Due to the small effective electron mass in direct III-V compounds degeneracy effects become important for carrier concentrations beyond a few 10^{17} cm^{-3}. Proper modeling of effects resulting from such commonly used doping levels is necessary to obtain accurate results in the simulation of devices on GaAs or InP substrates. Fermi statistics must be employed instead of the usually assumed Boltzmann distribution to describe carrier concentrations and derived properties. A number of many-body effects which may be either carrier-carrier or carrier-impurity interactions have impact on the electronic band structure and must therefore be considered.

The most common many-body effect is band gap renormalization. This concentration-dependent effect is usually termed band gap narrowing, since all interactions between carriers and dopants shifting the band edges reduce the band gap. Furthermore, the functional form of the density of states is changed at high doping levels via the appearance of tail states within the forbidden gap. A frequently overlooked fact is that the density of states increases with increasing concentration. This can be modeled by a concentration-dependent change of the effective mass.

Compensation and deactivation by clustering are effects which reduce the active doping concentration and thus affect transport properties indirectly. In compound semiconductors an-

other compensating effect which occurs at very high doping levels is autocompensation. This effect is caused by the amphoteric behavior of dopants which can act both as donors and acceptors. Apart from the doping level autocompensation depends on the chemical species of the dopant.

However, apart from the dopant-specific compensation behavior, the carrier mobility has also been found to depend on the species of the dopant directly. This is an additional effect contributing to the well-known difference in electron mobility in the majority/minority case which is caused by the particular screening properties of free electrons and holes. The direct species dependence of the mobility is caused by the different Coulomb scattering behavior due to the microscopic charge distribution of the doping ions. Usually a point-like impurity charge is assumed and therefore no species dependence can be examined. An analytic impurity scattering formula including the actual charge distribution can be used in a Monte Carlo transport calculation. It reveals that majority electron mobility is significantly affected in the highly degenerate region. Donors with larger atomic number lead to lower mobility values. In case of minority electron transport the influence of acceptor species is found negligible.

Christian Köpf was born in Vienna, Austria, in 1968. He studied communications and radiofrequency engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1993. He joined the 'Institut für Mikroelektronik' in November 1993, where he is currently working for his doctoral degree. In summer 1996 he was with LSI Logic in Milpitas, USA. His scientific interests include heterostructure devices, device modeling and solid state physics in general.

Physical Model Development for Advanced Device Simulation

Hans Kosina

Two mechanisms affecting the carrier transport through semiconductor devices have been investigated. The first investigated effect is size quantization. To accurately model the high-field transport in a two-dimensional electron gas several authors introduced a nonparabolicity correction in the subband dispersions. In our project we have quantitatively analyzed nonparabolicity effects in various two-dimensional electron gases. For this purpose a self-consistent Schrödinger-Poisson solver capable of dealing with silicon inversion layers and heterostructures has been developed. For heterostructures position-dependent material parameters are taken into account. The Schrödinger equation is solved in momentum space resulting in a Fourier series representation of the wave functions, whereas the Poisson equation is discretized by the finite difference method in real space. As the result of a simulation, each subband is characterized by three parameters, namely the subband energy, the subband mass and the nonparabolicity coefficient. This set of parameters serves as input for subsequent high-field transport calculations.

A second project aims at improved modeling and better understanding of the low field mobility limited by ionized-impurity scattering. The Brooks-Herring (BH) approach to ionized impurity scattering overestimates the low-field mobility of electrons in doped semiconductors. A consistent ionized-impurity scattering model has been developed which, in addition to the

BH model, accounts for degenerate statistics, dispersive screening, multi-potential scattering and the atomic form factor of the impurity atom. For the Lindhard dielectric function a rational approximation has been developed. Because coherent multi-potential scattering is too complex to be included in transport calculations only the two-potential or pair-scattering case has been considered. This is the highest order of multi-potential scattering that can be treated by analytical methods. To partly overcome the limitations of the first Born approximation on which the BH model is based a correction was derived from the Schwinger scattering amplitude. The charge distribution of the impurities is described by the Thomas-Fermi atomic model. This allows to derive an analytical expression for the atomic form factor which is a function of the atomic and the electron numbers of the impurity. Despite the various physical effects added an analytical expression for the scattering rate is retained which allows for efficient usage in Monte Carlo transport calculations. Such calculations have revealed the relative importance of the various effects. It has been found that the weakness of the plain BH model cannot be overcome by just adding one dominant effect. Instead, several nearly equally important effects have to be added.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. In summer 1993 he held a visiting research position at the Advanced Research and Development Laboratory at Motorola, Austin. Currently he is employed as an assistant professor. His current interests include modeling of carrier transport in semiconductor devices, quantum effects and computer aided engineering in VLSI technology.

Parallelization of Program Packages for the Simulation of Micro-Structures

Erasmus Langer

Since in all areas of electronics technology continues to evolve, numerical simulation of micro-structures which are playing a dominant role in the broad field of microelectronic devices is becoming increasingly important. Though the most widespread representatives are ultra large scaled integrated ("ULSI") semiconductor devices, there also exist various other kinds of devices which are based on micro-structures, for instance the surface acoustic wave ("SAW") devices.

The simulation of realistic microelectronic devices and their technological fabrication processes imply high demands on computer resources, especially concerning the computing power needed, but also the memory requirements. In order to intensify the research capability of the simulation tools, an increase of the throughput and, therefore, an acceleration of the programs are an absolute necessity. For this purpose a project which is part of an interuniversitary project, the 'Spezialforschungsbereich (SFB)' AURORA — Advanced Models, Applications, and Software Systems for High Performance Computing, has been implemented. Six institutes of the 'Universität Wien' and the 'Technische Universität Wien' are participating in the project AURORA which is funded by the Austrian 'Fonds zur Förderung der wissenschaftlichen Forschung (FWF)'.

The Monte Carlo method is rapidly gaining acceptance as a means for the simulation of ion implantation — the most

important process step for incorporating dopant atoms into semiconductors — because it accounts well for the physical reality. The Monte Carlo method plays an important role within the device simulation, too. MINIMOS uses different transport models — depending on the geometry, the bias conditions, and the desired accuracy — one of which is the Monte Carlo transport model.

A well-known drawback of the Monte Carlo approach is its considerable demand for computation time to obtain results with satisfying statistical accuracy. Therefore, the time characteristics have to be optimized in order to utilize the Monte Carlo-based solution method for practical investigations, e.g., investigation of the influence of the doping profile on the electrical behavior of the device where a loop over process and device simulation must be performed several times. Particle-based simulation is well suited for parallelization. One main goal will be the development of parallel, Monte-Carlo-based algorithms running on heterogeneous workstation networks or on distributed memory architectures. In the long term, these parallelized algorithms shall be implemented within the framework VISTA.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the 'Technische Universität Wien' in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik', first as a research assistant and then as assistant professor. His research field was first the numerical simulation of semiconductor devices and later the excitation and propagation of electro-acoustic waves in anisotropic piezoelectric materials where he also received his doctoral degree in 1986. In 1988 he joined the 'Institut für Mikroelektronik'. In April 1997 he received the 'venia docendi' in 'Mikroelektronik'.

Three-Dimensional Simulation of Dopant Diffusion

Ernst Leitner

The development of today's semiconductor devices often requires the three-dimensional investigation of problems. This accounts for the rising need of process simulators capable of handling complex three-dimensional structures consisting of several materials. Performing efficient and accurate simulations requires enhanced models and preferably error controlled mesh adaptation.

To meet these requirements an analytical modeling interface has been integrated to an object-oriented solver. The resulting program AMIGOS (Analytical Model Interface & General Object-Oriented Solver) treats the type of the partial differential equation (PDE) to be solved as input, where the discretization formulas for the desired models are read from a file. According to this model description the global equation systems for the finite element method used by the solver are set up and computed. Furthermore, the model description may hold an expression for a grid-criterion, which is used to determine elements which are either too large or too small. Within the model description heuristic criteria as well as an efficient computation of the discretization error using the Zienkiewicz-Zhu error estimator can be implemented. Application of this discretization error as grid criterion allows to control the spatial discretization error.

The grid adaptation itself is performed by using a mixed-element tree. The refinement procedure allows multiple local

refinements of elements. In three-dimensional grids a tetrahedron is split into four smaller ones located at its corners and a remaining octahedron. The latter is split into six small octahedra located at its corners and eight remaining tetrahedra, filling the leaks between. At the transition between refined and unrefined elements, the unrefined element is split up just to meet the connectivity conditions. When such a transition element has to be refined itself, the recursive refinement method is applied to the unrefined element, which ensures the shape preserving property of the method. The storage of the element tree additionally allows to undo such local refinements when necessary. This method is also applied to two-dimensional finite elements such as linear and quadratic triangular and quadrilateral elements.

Furthermore, AMIGOS is capable of coupling multiple material segments with different physical models using different physical quantities, using again the analytical model interface for the description of the boundary conditions. Further development will focus on the implementation of a variety of diffusion and oxidation models including mechanical stress, and on the moving grid problem.

Ernst Leitner was born in Gmunden, Austria, in 1968. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in January 1993, where he is currently working for his doctoral degree. In the autumn of 1994 he held a visiting research position at Philips, Eindhoven, The Netherlands. His work is focused on three-dimensional process simulation, adaptive gridding, and the basic physics of transport phenomena in solids.

Using Layout Data in the VISTA Framework

Rui Martins

The use of layout information is growing as more and more three-dimensional tools are available within the VISTA framework. This has required an extension of the editing capabilities of our geometry and layout PIF-Editor (PED). In addition to other improvements we would like to point out the support of phase-shift masks and the introduction of the custom technology file, where the editor can be configured to a specific technology. Thus, for starting a small layout file it is now very easy to use PED in a productive way, while larger designs can be created and then exported from general purpose ECAD frameworks to VISTA, as a Caltech Intermediate Format (CIF) or as Calma GDSII files.

One layout can contain a large number of devices and interconnections. As usual in these files, several of the devices are equal and are repeated all over the layout (and this is also true of typical interconnect patterns), so we have provided a user-friendly way to select one copy of the masks which form this particular device (e.g. a MOS transistor) or this interconnect region (e.g. the bias between two metal layers with high current density) that need to be simulated. Also, depending on the required precision and computer resources constraints, some of these simulations are performed with two-dimensional tools, whereas others (needing more accurate results) are using a three-dimensional tool. These two different ways are posing a problem in the preparation of the layout data used by the

suitable simulator. Our solution to this problem is that the user only needs to interactively select the simulation domain: A line in the two-dimensional case or a set of polygonal regions in the other.

The possibility of using several process and device simulators in an integrated environment is opening the possibility of extracting circuit netlists from layout information (in a SPICE like format) with a degree of accuracy far better than obtained with the classical extraction tools in ECAD frameworks. With MINIMOS and the VISTA optimizer we can achieve models for the active devices, and as SCAP and STAP can predict with high accuracy, the capacitance and the resistance values of parasitic and non-parasitic three-dimensional structures respectively, we can extract the parameters of the most important and common components found in an integrated circuit. Research on in the extraction of monolithic inductors and in interconnect modeling is continued. An advantage of this approach is that it allows for the interaction of layout, technology and circuit parameters, so one can find the best global compromise.

Rui Martins was born in Porto, Portugal, in 1968. He studied electronic and telecommunications engineering at the University of Aveiro - Portugal, where he received the degree of 'Licenciado' in 1991 and 'Mestre' in 1994. In 1993 he was with INESC (Engineering Institute for Systems and Computers) where he worked on biomedical instrumentation. He joined the 'Institut für Mikroelektronik' in October 1994 and is currently working for his doctoral degree. His scientific interests include very low power analog and digital integrated circuit design, digital signal processing and TCAD framework aspects.

Object-Oriented Management of Algorithms and Models

Robert Mlekus

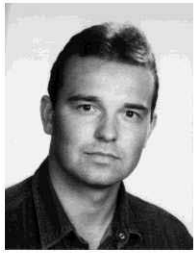
The continuous development of new processes and devices in combination with the increasing number of devices on a single chip requires a permanent improvement of process and device simulator programs by way of implementing new or enhanced models and algorithms. In traditional simulators the integration of new models requires changes in the source code of the simulator and, therefore, deep knowledge of implementation details. For that reason a new library-based concept has been developed, which provides an object-oriented approach to the implementation, parametrization and selection of models, without any changes in the source code of the simulator.

The algorithm library is designed to support any kind of algorithm using arbitrary user-defined data structures as parameters, which are handled in their native C++ representation and forwarded to the models by using references. It provides a set of C++ classes and methods to handle these algorithms and parameters directly in C or C++ code and the object-oriented Model Definition Language (MDL).

Each model is represented by an object which encapsulates instructions, private variables, parameters, documentation of the model and the information about the type of the model in a single unit. Models are separated from the simulator by interfaces which contain information about the necessary parameters, their default values and the required algorithm.

An interpreter for the MDL simplifies the development of new models by supporting the definition of new algorithms and their parameters without any changes in the source code or the executable of the simulator. To optimize the speed of simulation algorithms a MDL-compiler can be used to generate C++ source code which can be compiled into object libraries containing sets of approved models. Therefore algorithms and data structures used in the innermost simulation loops can be handled using the mechanisms of the algorithm library with almost no performance losses compared to traditional function calls.

The MDL provides statements which allow the definition of new models in an object-oriented manner, using a subset of the class definition mechanisms of the C++ language. The specification of global parameter values and the actual algorithms which are used by the simulator for a specific task are neatly integrated. Furthermore, MDL supports the developer by supplying statements for inquiring database records describing all available algorithms, their interfaces and documentation for specific simulation tasks, and reports giving debug information such as the algorithms and/or parameter values actually used.



Robert Mlekus was born in Tulln, Austria, in 1968. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994, where he is currently working for his doctoral degree. His work is focused on object-oriented techniques for the integration of physical models into process and device simulators.

Simulation of Heterostructure Bipolar Transistors

Vassil Palankovski

The development of heterostructure devices has proceeded in very rapid steps recently. Heterojunction Bipolar Transistors (HBTs), Heterojunction Field-Effect Transistors (HFETs), optical detectors, and many other devices have derived great benefits from heterostructure technology. Significant improvements in the material properties and in the performance of the devices have been obtained. The applicability of SiGe alloys in the silicon technology has established an attractive class of HBTs based on Si, which shows better performance than the conventional Si BJTs, but worse performance than the III-V compound semiconductor devices, which are still receiving most attention in HBT research. Comparative analyses of different HBTs are of great importance for studying the device characteristics and are a prerequisite for further improvements.

MINIMOS-NT is our two-dimensional device simulator with approved capabilities in the simulation of devices with complex structure. The splitting of the device geometry into different segments allows an independent use of different materials and physical models such as drift-diffusion or hydrodynamic models. For accurate simulation of HBTs the respective temperature and mole fraction-dependent models of the physical parameters of the alloys (e.g., conduction and valence band-edge energies, electron and hole effective masses, effective density of states) on the one hand, and of the mobilities on the other hand have been implemented. Shockley-Read-Hall and Auger

recombination, and doping-dependent band-gap-narrowing are taken into account. An appropriate heterojunction interface model considering the effect of tunneling electrons through the energy barrier is used for semiconductor interfaces.

As a particular example the electrical behavior of a Si BJT, a Si HBT with a SiGe narrow-gap base and a GaAs HBT with a AlGaAs wide-gap emitter at room temperature has been studied in a comparative way, i.e., the simulated devices have the same geometry and doping profiles with a high base doping concentration typical for HBTs. The respective output characteristics, current gains and high-frequency performance of the devices are in good agreement with the experimental data available. However, the complexity of the HBT structure leaves ample room for a material dependent performance optimization. Thus, a study of constraints is required in order to project performance superiority with respect to certain applications of a particular HBT structure and therefore to contribute to answering one of the crucial questions of today: "Which is the material of the future?"

Vassil Palankovski was born in Sofia, Bulgaria, in 1969. He studied electrical engineering at the Technical University of Sofia, where he received the degree of 'Dipl. Engineer' in 1993. Afterwards he worked for Siemens JV in Bulgaria for three years. He joined the 'Institut für Mikroelektronik' in May 1997, where he is currently working for his doctoral degree. His scientific interests include device simulation, heterostructure device modeling and physical aspects in general.

High-level Optimization Tasks in the VISTA TCAD Framework

Richard Plasun

The design and fabrication of smaller and faster semiconductor devices relies on the proper numerical simulation of fabrication processes and electrical characteristics. To improve manufacturability, different variations of process parameters have to be simulated and analyzed. For this purpose many features have been added to the *Vienna Integrated System for TCAD Applications* (VISTA) to support high-level analysis functionality.

For the automatic generation of experiments with different parameters, a Design of Experiments (DoE) module can be used. The type of the experimental design can be chosen out of a large number of available types. After simulating these experiments the control and response values are written into the *experiment table*, which is represented by an evaluable entity VLISP object.

The Response Surface Methodology (RSM) module fits polynomial functions to the data from the *experiment table*. Both the Design of Experiments and Response Surface Methodology modules support a number of transformations to adequately represent nonlinear systems.

For optimizing device performance parameters over a given input variable space, the optimizer module performs optimizations under nonlinear constraints and nonlinear parameter estimations. It minimizes the target function which can be as-

sembled out of input and output values. All communication between the framework and external executables works on an asynchronous basis to allow simultaneous control of a number of independent tasks within the simulation environment.

A graphical user interface to the *experiment table* gives an overview of the chosen input parameters and the extracted responses of the simulation runs. Further simulation experiments and their input parameters can be easily submitted by using pull-down menus. With the interactive RSM-viewer the fitted surface can be visualized as two- or three-dimensional graphics and sliders enable the user to understand the influence of the controls.

A future issue to be addressed is the advancement of tool binding to a hierarchical class-based approach such that more simulators and parameter extractors can be integrated faster and more stably. The template-file-based input-deck generator mechanism will be extended to serve other simulators. This will increase the flexibility of the VISTA framework.

Richard Plasun was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in March 1995. He is currently working for his doctoral degree. His scientific interests include linear and nonlinear optimization, TCAD framework aspects and software technology. From October to December 1996 he was with the National Semiconductor Corperation in Santa Clara, where he concentrated on tool binding and process optimization aspects.

Three–Dimensional Simulation of Etching and Deposition Processes

Wolfgang Pyka

Topographic simulation offers the possibility of understanding the time evolution of what happens during an etching or deposition process. Due to the decreasing feature sizes in today's semiconductor technology a rigorous simulation of three-dimensional geometry effects becomes necessary.

Our simulator is based on a general three-dimensional surface advancement algorithm, which applies morphological operations derived from image processing to a cellular material representation. The material description is stored in a three-dimensional array. The surface is represented by a linked list of all cells located at the material-vacuum interface. This list contains the geometry and rate information for all surface cells. A structuring element, a sphere in the isotropic case or an ellipsoid in general cases, moves across the surface and all positions hit by the element are marked. Subsequently the material index at the marked positions is either changed from material to vacuum or vice versa depending on whether etching or deposition should be simulated.

The etching or deposition rates are calculated by integrating the flux distribution functions over the visible area. Thus it is necessary to determine the visibility limits for each surface cell, i.e. it has to be checked whether the trajectory from the particle source to a certain surface cell is screened by other material cells or not. To minimize the required CPU time,

we do not scan the whole hemisphere above the cell but move along the boundary of the visible area instead.

Modeling of etching and deposition processes includes the analysis of flux distributions such as functions which describe the flux emanating from sputter targets with off-center maxima. Additionally, the knowledge of the surface orientation is required for processes with surface orientation-dependent interaction of the incident particles. The calculation of the surface orientation is accomplished by averaging the normal vectors of the exposed sides of all surface cells within a certain distance from the actual cell. A special algorithm allows to conserve sharp edges of the input geometry, which otherwise would be rounded by the averaging operation.

Most recently, modeling has been performed for sputter deposition processes, which lead to the formation of bulges at sharp convex edges. Probably shadowing effects are responsible for this phenomenon, but further investigations are still necessary.

Wolfgang Pyka was born in Innsbruck, Austria, in 1970. He studied material science at the 'Montanuniversität Leoben', where he received the degree of 'Diplomingenieur' in June 1996. In December 1996 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. His work is focused on simulation and modeling of etching and deposition processes and on algorithms for topographic simulations.

Three-Dimensional Simulation of Thermal Oxidation

Mustafa Radi

Thermal oxidation of silicon is a critical step in the fabrication of highly integrated electronic circuits and is mainly used for isolating adjacent devices from each other. Knowledge of the physical processes that affect thermal oxidation is essential for optimizing applications.

Miniaturization of devices based on silicon technology leads to the realization of integrated structures exhibiting an increasingly complex topology. The evolution of isolation techniques using local oxidation of silicon (LOCOS) is one of the most striking examples for that purpose. In order to reduce the development duration of such state-of-the-art technologies, two- and three-dimensional process simulation capabilities are of prime interest. Difficulties in numerical modeling of silicon oxidation arise from the necessity to ensure both a wide prediction capability and a very flexible numerical solution. Accurate modeling requires the knowledge of the characteristics of the mechanical thin film properties of integrated circuit materials as well as stress effects of the oxidation kinetics. The efficiency of the numerical implementation depends on the ability to handle complex topological configurations within reasonable computing time.

To cope with these different requirements the extremely flexible simulator AMIGOS (Analytical Model Interface & General Object Oriented Solver) has been developed. It is a problem-

independent simulation system which can handle any nonlinear partial differential equation system in time and space in either one, two or three dimension(s). There are no restrictions whether using scalar-, field- or even tensor quantities within a model, and, if desired, any dependent field quantity can be calculated. Furthermore, the user can influence the numerical behavior of the differential equation system through complete control of the residual vector and its derivative (e.g. punishing terms, damping terms, etc.). Even interpolation and grid-adaptation formulations can be formulated within a developed model and can thus be adapted to a particular problem very well.

With AMIGOS, a new approach to the local oxidation in three dimensions has been developed, based on a parameter-dependent smooth transition zone between silicon and silicon-dioxide. The resulting two phase problem is solved by calculating a free diffusive oxygen concentration and its chemical reaction with pure silicon to silicon-dioxide. This effect causes a volume expansion which leads to mechanical stress concerning the surrounding boundary conditions. With a suitable set of parameters this approach is equivalent to the standard sharp interface model based on the fundamental work of Deal and Grove.

Mustafa Radi was born in Innsbruck, Austria, in 1968. He studied electrical engineering and computer science at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in electrical engineering in 1994. He joined the 'Institut für Mikroelektronik' in August 1994, where he is currently working for his doctoral degree. His research interests include developing models and algorithms for solving systems of coupled differential equations in one-, two-, and three-dimensional silicon structures as well as High Performance Computing and Networking(HPCN).

Generation of Triangular Grids in MINIMOS-NT

Martin Rottinger

As the feature size of actual devices is further reduced the effects of non-planarities can no longer be neglected in device simulation. For efficient discretization of non-planar geometries triangular grids are used. Compared to rectangular grids the efforts for generating a quality mesh are much higher for triangular grids. Therefore, the well-known grid generator Triangle has been integrated into MINIMOS-NT.

The grid generator Triangle is also used for triangulation in process simulation. The unstructured triangular grids resulting from process simulation are not suitable for device simulation. Especially for MOS devices in which a channel builds up under certain bias conditions the grid used for implantation and diffusion steps during process simulation is not fine enough in vertical direction. The grid can be refined by specifying a maximum size for each grid element. Thereby the grid density can be increased, but the grid remains unstructured. This can lead to a considerable discretization error for the current density caused by an error in the interpolation of the carrier concentration, which shows an exponential dependence on the distance to the interface.

To avoid the error in the discretization of the current density the triangular grid elements have to be aligned to the semiconductor-insulator interface to guarantee a current flow parallel to the interface. To produce grids consisting of aligned

elements in a channel region and elements with arbitrary orientation within the bulk the input geometry has to be modified. By inserting geometry lines parallel to the interface the grid generator can be forced to produce layers of triangles which are aligned to the interface.

Only the geometry and the material type from an input file are taken into account for generating the simulation grid. The grid which has been used for process simulation is only used to specify the doping. The first step is to analyze the geometry and to search for semiconductor-insulator interfaces at which a channel might build up. At these interfaces so-called interface regions are generated.

An interface region is built up from corners and connecting straight lines, each of them consisting of a number of layers specified by the user. Depending on the angle of the interface lines the corners are classified into different types. Next appropriate templates are inserted into the geometry and the corner templates are then connected by straight lines. The modified geometry is triangulated by the grid generator and the resulting grid is used for simulation. After the simulation a further grid modification or refinement can be applied to increase the accuracy of the simulation.

Martin Rottinger was born in Wels, Austria, in 1968. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in November 1994. Currently he is working for his doctoral degree. His scientific interests include solid state device technology and device modeling. In autumn 1995 he held a visiting research position at Philips in Eindhoven, The Netherlands.

SAP — A Finite-Element Package for Interconnect Simulation

Rainer Sabelka

In deep submicron designs the interconnect structures significantly determine the overall circuit behavior. As devices are getting smaller and faster the interconnect resistance and capacitance increasingly limit the circuit speed. Additionally, the influence of thermal effects gains in significance. As a consequence of the increasing packaging density the design comes closer to the physical limits for temperature and current density. Careful investigations during the design phase become necessary to ensure circuit reliability. Since experimental measurements of these physical effects are often expensive, inaccurate or impossible, there is an increasing need for numerical calculation.

Therefore, the program package SAP (Smart Analysis Programs) has been developed. It contains tools for capacitance extraction, resistance extraction, and thermal analysis of multi-layer interconnect structures. Three input preprocessors are available for two- and three-dimensional geometry specification and for automatic grid generation.

The first tool, SCAP (Smart Capacitance Analysis Program), calculates the electric field between interconnect lines by solving Laplace's equation and derives the capacitances from the field energy. The program has been extended to support dielectric material with anisotropic permittivity. The global grid refinement algorithm has also been improved. The input parsers

of the preprocessors have been rewritten for a cleaner syntax and better error messages.

The simulator STAP (Smart Thermal Analysis Program) performs a coupled electro-thermal simulation. It solves Laplace's equation to obtain the current flow inside interconnect lines and the heat conduction equation to calculate the temperature increase caused by the generated heat. A significantly lower memory consumption has been achieved by reorganizing the simulator's internal data structure. We have tested the simulator with several applications and compared its results with experimental measurements.

For advanced investigations of the simulation results a new visualization tool has been developed. It is based on the VTK (Visualization Toolkit) graphics library and has a rich set of operations for post-processing and displaying the calculated data.

Rainer Sabelka was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in January 1995. He is currently working for his doctoral degree. He held visiting research positions at Digital Equipment Corporation, Hudson, in 1996 and at Sony, Atsugi, Japan in 1997. His scientific interests include three-dimensional interconnect simulation of multilevel wired VLSI circuits, visualization and software technology.

VLSI Technology Optimization

Gerhard Schrom

The development of VLSI technology has entered the sub-half-micron region at a rapid pace and is expected to reach 0.13μm by the year 2004. Such small dimensions are posing a number of technological and device-physical problems such as short-channel effects, hot-carrier phenomena, and, one of the most critical factors, thermal power. One way of tackling these problems is to develop *ultra-low-power (ULP)* CMOS technologies, i.e. lowering the supply and threshold voltage to a minimum value to enable a substantial reduction of the power consumption with a controllably small speed penalty. Furthermore, this technique drastically reduces hot-carrier effects and gate-induced drain leakage. For developing a ULP technology or adapting an existing technology, various different device structures have to be investigated and optimized. Two optimization strategies are primarily pursued: minimizing the power consumption with a prescribed minimum speed and maximizing the speed at a fixed supply voltage.

The direct relation to system parameters calls for new analysis methods. Drive current, leakage, and threshold control are primarily the most common traditional device performance and qualification criteria. However, these parameters are very indirectly linked to the actual system's performance. Previous work on systems analysis was usually based on analytical equations with nominal process parameters. However, such analytical models are ever less adequate for capturing the non-ideal behavior of advanced deep-sub-micron devices. On the other

hand, complete device characterization and circuit simulation to determine the system performance can often not be afforded. Therefore, a new method has been developed by carefully selecting the relevant parameters and device data sets that can be combined with a suitable system model. The method yields performance data on the system level directly from raw electrical device data obtained with a minimum set of device simulations. The input data are key technology parameters such as the nominal gate length and oxide thickness, operational parameters, such as supply voltage and temperature, and system parameters, such as activity ratio and logic depth. The output data fall into three categories: performance parameters, like speed and power consumption, qualification parameters, like noise immunity and admissible clock frequency range, and informational parameters.

This allows a system-relevant quantitative statement on the process/device performance. Furthermore, in combination with statistical analyses of the input and output parameters, a yield estimation and the identification of critical parameter ranges are possible.

Gerhard Schrom was born in Mödling, Austria, in 1963. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in March 1992. During his studies he was working on software development projects in the CAD field. He joined the 'Institut für Mikroelektronik' in April 1992, where he currently works for his doctoral degree. His research interests include device and circuit simulation, circuit design and synthesis, signal and image processing, and TCAD framework aspects. In spring 1994 he held a visiting research position at Hitachi, Tokyo, Japan.

Optimization of MOS Device Structures

Michael Stockinger

In the past, various MOS device structures have been suggested for improving the device performance for VLSI design down to $0.1\mu m$ gate length. The LDD (lightly doped drain) structure increases the breakdown voltage and reduces hot-carrier effects. Buried layers and pocket implants can efficiently prevent drain punchthrough. A common characteristic of all of these structures is the fact that doping profile variations are used to achieve specific device performance improvements.

The future trends in CMOS technology are progressive downscaling of the device geometries, achieving higher device densities on the chip, increasing the system's performance, and reducing the supply voltage and power consumption. Unfortunately, just downscaling the supply voltage leads to a loss in device speed because the on-current of the transistors will be reduced.

One way to achieve speed improvement is to provide appropriate parallel architectures on the system's level, but this will increase the circuit complexity and, therefore, the chip area. Another approach to compensate for the loss in device speed is to reduce the threshold voltage, too. As a result, the drain-to-source leakage current (also called "off-current") will increase leading to a higher standby current of the system.

By choosing an optimal device structure the ratio between the on- and the off-current of a MOS transistor can be maximized.

Starting with a simple MOS device with constant substrate doping and a specified limit for the off-current, the on-current is successively improved by doping profile optimization. The lateral and vertical doping profiles of the substrate are modeled by splines to achieve smooth profiles. The spline knots are homogeneously spread over the region underneath the gate and build up the set of optimization parameters. The optimization target is to maximize the on-current while keeping the off-current at a constant value.

VISTA provides a useful framework for this optimization task because it contains a built-in optimizer. For every optimization step the grid and the doping profiles are first computed and written to a wafer state file. Then device simulations with MINIMOS-NT are performed to obtain the device characteristics. Special care has to be taken not to aggravate other parasitic effects such as substrate current or junction capacitances. Therefore, additional device data has to be checked during optimization. Enhanced process technologies such as SOI (silicon on insulator) are also used as a starting point for optimization.

Michael Stockinger was born in Vienna, Austria, in 1970. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. After his studies he worked on an ASIC-design project at the 'Institut für Allgemeine Elektrotechnik und Elektronik' for six months. In February 1997 he joined the 'Institut für Mikroelektronik' where he is currently working for his doctoral degree. His scientific interests include device and circuit simulation, circuit design, solid state device technology, and low-power technology.

Advanced Analysis of Semiconductor Processes Using VISTA

Rudolf Strasser

The state-of-the-art process and device simulation tools provide a highly efficient means to predict the process and device performance. Nevertheless, time-consuming efforts to setup, perform, and analyze simulations often prevent designers from performing simulations, neglecting the positive impact of simulation technology on cycle time and cost reduction. The VISTA framework intends to close this gap between the potential capabilities of simulation tools and a technology engineer's time restrictions.

Easy compilation, maintenance as well as concurrent design of the process flow are very important for the simulation of process technology at industrial sites. Practically it is extremely difficult for a technology engineer to keep up with technology changes. Thus inconsistencies between the simulation input and the actual fabrication data often occur. Therefore, VISTA provides a possibility to — automatically — compile a process flow from a recipe library, which comprises the current state of a technology. Usually this library is automatically generated from fabrication data. Once this library is up to date, it is sufficient to recompile the process flow. As users can share recipe libraries, this concept also enables the concurrent development of a process.

VISTA process flow representation allows for the definition of symbolic parameters, which are used to perform split run ex-

periments. Thus a few — out of hundreds — of technology parameters can be identified and selected for investigations. Once ranges and default values for these parameters have been defined, the VISTA Design of Experiments module automatically generates split runs.

Usually a large number of simulations arises from Design of Experiments. In order to minimize the computation time required for a simulation experiment a load balancing mechanism has been implemented. VISTA periodically polls for the actual load of each registered computation host and thus enables automatic load balancing. Individual load limits for each node as well as global load limits provide a flexible and highly effective — in terms of resource optimization — distribution of simulation workload.

VISTA simulation methodology has proven to be extremely useful at industrial sites. Future development will especially emphasize on further enhancement of the practical usability of the framework.

Rudolf Strasser was born in Ried im Innkreis, Austria, in 1970. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1995. From spring 1992 to autumn 1993 he held a research position at the campus-based Engineering Center of Digital Equipment Corporation, Vienna, Austria. He joined the 'Institut für Mikroelektronik' in April 1995. In summer 1996 he was with the Advanced Products Research and Development Laboratory at Motorola, Austin. He is currently working for his doctoral degree. His scientific interests include semiconductor technology, grid generation and software engineering.

Modeling Non-Parabolicity Effects in Quantized Systems

Christian Troger

To improve the performance of MOSFETs and HEMTs these devices are continuously scaled down in their dimensions. The characteristics of such devices are mainly determined by the formed two dimensional electron gas. Thus an accurate modeling of the electron transport in such inversion layers or heterostructures has to include the following points: First, the confinement of carriers has to be treated quantum-mechanically. Therefore, a self-consistent Schrödinger-Poisson solver can be considered as an important component for the whole simulation. Second, the use of a parabolic relation between the energy and the wave vector is no longer accurate enough. As an approach to a more realistic dispersion relation we have considered the inclusion of the non-parabolic correction term that is commonly used in the bulk case.

The Schrödinger-Poisson solver for MOSFET structures uses the effective mass approximation and a new formalism that allows the inclusion of non-parabolicity in the description of a quasi two-dimensional electron gas. This formalism which solves the Schrödinger equation in momentum space can also be used for effective masses and non-parabolicity coefficients which depend on position. Using an object-oriented approach the code of the Schrödinger-Poisson solver has been extended in order to cover both cases with only a few different code portions, allowing the simulation of both heterostructures and inversion layers. As Poisson's equation is most efficiently solved

in real space, Fast Fourier Transforms are performed for each iteration to convert data from momentum to real space representation and vice versa. The implemented graphical user interface allows an easy definition of the simulated structure and the visualization of all calculated quantities for different parameter values or iteration steps. A further development will include the definition of a script language. The interface to a subsequent transport simulation is defined by a parameter set for each subband consisting of eigenenergy, effective mass and non-parabolicity coefficient.

From the first calculations we earned realistic results concerning the parameters of our introduced representation of the in-plane dispersion relation, and we were able to study quantization effects. Some algorithms allow further optimization. The calculation time can be reduced if the non-parabolicity effects are neglected in the first iteration steps. Beside this, the derivate of the electron density with respect to the potential can be calculated more accurately by means of the quantum mechanical perturbation theory which will accelerate the self-consistent iteration.

Christian Troger was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1995. He joined the 'Institut für Mikroelektronik' in September 1995, where he is currently working for his doctoral degree. His work is focused on the simulation of quantum mechanical devices.

Publications

Papers in Conference Proceedings

[V33] Knaipp M., Selberherr S.,
Investigation on Hydrodynamic Impact Ionization (II) in n-MOSFETs,
Abstracts Intl. Conf. on Computational Physics, (2.-4. June 1997, Singapore), pp.37-38.

[V32] Kaiblinger-Grujin G., Kosina H., Selberherr S.,
Electron Mobility in Doped Semiconductors,
Abstracts Intl. Conf. on Computational Physics, (2.-4. June 1997, Singapore), pp.30-31.

[V31] Troger C., Kosina H., Selberherr S.,
A Consistent Inclusion of Nonparabolicity in a Schrödinger-Poisson Solver for Silicon Inversion Layers,
Abstracts Intl. Conf. on Computational Physics, (2.-4. June 1997, Singapore), pp.26-27.

[V30] Selberherr S.,
The State of the Art in Technology Computer-Aided Design,
Abstracts Primer Taller de Technicas de Simulacion en Semiconductores, (2.-3. June 1997, Mexico City), p.1, (invited).

[V29] Wasshuber Ch., Kosina H., Selberherr S.,
Single-Electron Memories,
Proceedings Intl. Workshop on Computational Electronics, (28.-30. May 1997, Notre Dame), p.FrP1.

[V28] Kosina H., Troger C.,
SPIN – A Schrödinger Poisson Solver Including Nonparabolic Bands,
Proceedings Intl. Workshop on Computational Electronics, (28.-30. May 1997, Notre Dame), p.P51.

[V27] Brech H., Simlinger T., Grave T., Selberherr S.,
Influence of Gatelength on the DC-Characteristics and f_t of Pseudomorphic Power-HEMTs,
Proceedings Workshop on Compound Semiconductor Devices and Integrated Circuits, (25.-28. May 1997, Scheveningen), pp.1-2.

[V26] Köpf Ch., Kaiblinger-Grujin G., Kosina H., Selberherr S.,
Influence of Dopant Species on Electron Mobility in InP,
Proceedings Intl. Conf. on Indium Phosphide and Related Materials, (11.-15. May 1997, Hyannis), pp.280-283.

[V25] Kaiblinger-Grujin G., Kosina H., Selberherr S.,
Monte Carlo Simulation of Electron Transport in Doped Silicon,
Proceedings High Performance Computing Asia 1997 Conf., (28. April -2. May 1997, Seoul), pp.444-449.

[V24] Radi M., Leitner E., Hollensteiner E., Selberherr S.,
AMIGOS: Analytical Model Interface & General Object-Oriented Solver,
Proceedings Seminar Basics and Technology of Electronic Devices, (19.-22. March 1997, Großarl), pp.57-60.

[V23] Mlekus R., Selberherr S.,
An Object-Oriented Approach to the Management of Models,
Proceedings Seminar Basics and Technology of Electronic Devices, (19.-22. March 1997, Großarl), pp.53-56.

[V22] Kirchauer H., Selberherr S.,
Three-Dimensional Photolithography Simulation,
Proceedings Seminar Basics and Technology of Electronic Devices, (19.-22. March 1997, Großarl), pp.27-31.

[V21] Stach A., Sabelka R., Selberherr S.,
Three-Dimensional Layout-Based Thermal and Capacitive Simulation of Interconnect Structures,
Proceedings IASTED Intl. Conf. on Modelling, Identification and Control, (17.-19. February 1997, Innsbruck), pp.16-19.

[V20] Köpf Ch., Kosina H., Selberherr S.,
Anisotropic Electron Transport in Lattice-Mismatch-Strained GaInAs Alloys,
Abstracts of the 21st Condensed Matter Physics Meeting, (4.-7. February 1997, Pakota Island), p.TP21.

[V19] Kaiblinger-Grujin G., Kosina H., Selberherr S.,
Dependence of Electron Mobility on Dopants in Heavily Doped Semiconductors,
Abstracts of the 21st Condensed Matter Physics Meeting, (4.-7. February 1997, Pakota Island), p.TA02.

[V18] Langer E., Selberherr S.,
Three-Dimensional Process Simulation for Advanced Silicon Semiconductor Devices,
Proceedings ASDAM 96 Conf., (20.-24. October 1996, Smolenice), pp.169-177, (invited).

[V17] Schrom G., Selberherr S.,
Ultra-Low-Power CMOS Technologies,
Proceedings CAS 96 Conf., (9.-12. October 1996, Sinaia), pp.237-246, (invited).

[V16] Köpf Ch., Kosina H., Selberherr S.,
Anisotropic Mobility Model for GaInAs Covering Full Composition and Strain Range in the GaAs-InAs System,
Abstracts Intl. Symposium on Compound Semiconductors, (23.-27. September 1996, St.Petersburg), p.30 and Proceedings pp.675-678.

[V15] Langer E.,
Simulation technologischer Prozesse,
Tagungsband ÖPG-Tagung 1996, (23.–27. September 1996, Johannes Kepler Universität Linz), pp.130, (invited).

[V14] Brech H., Simlinger T., Grave T., Selberherr S.,
Current Transport in Double Heterojunction HEMTs,
Proceedings ESSDERC 96, (9.-11. September 1996, Bologna), pp.873-876.

[V13] Knaipp M., Simlinger T., Kanert W., Selberherr S.,
Analysis of Leakage Currents in Smart Power Devices,
Proceedings ESSDERC 96, (9.-11. September 1996, Bologna), pp.645-648.

[V12] Schrom G., Stach A., Selberherr S.,
A Charge Based MOSFET Model for Low-Voltage Mixed-Signal Applications,
Proceedings ESSDERC 96, (9.-11. September 1996, Bologna), pp.495-498.

[V11] Kirchauer H., Selberherr S.,
Rigorous Three-Dimensional Photolithography Simulation Over Nonplanar Structures,
Proceedings ESSDERC 96, (9.-11. September 1996, Bologna), pp.347-350.

[V10] Puchner H., Neary P., Aronowitz S., Selberherr S.,
A Transient Activation Model for Phosphorus after Sub-Amorphizing Channeling Implants,
Proceedings ESSDERC 96, (9.-11. September 1996, Bologna), pp.157-160.

[V9] Schrom G., Stach A., Selberherr S.,
A Consistent Dynamic MOSFET Model for Low-Voltage Applications,
Proceedings SISPAD 96 Conf., (2.-4. September 1996, Tokyo), pp.177-178.

[V8] Fleischmann P., Sabelka R., Stach A., Strasser R., Selberherr S.,
Grid Generation for Three-Dimensional Process and Device Simulation,
Proceedings SISPAD 96 Conf., (2.-4. September 1996, Tokyo), pp.161-166, (invited).

[V7] Pichler Ch., Plasun R., Strasser R., Selberherr S.,
Simulation Environment for Semiconductor Technology Analysis,
Proceedings SISPAD 96 Conf., (2.-4. September 1996, Tokyo), pp.147-148.

[V6] Wasshuber C., Kosina H.,
A Single Electron Device and Circuit Simulator with a New Algorithm to Incorporate Co-tunneling,
Proceedings SISPAD 96 Conf., (2.-4. September 1996, Tokyo), pp.135-136.

[V5] Fleischmann P., Selberherr S.,
A New Approach to Fully Unstructured Three-Dimensional Delaunay Mesh Generation with Improved Element Quality,
Proceedings SISPAD 96 Conf., (2.-4. September 1996, Tokyo), pp.129-130.

[V4] Kirchauer H., Selberherr S.,
Three-Dimensional Photoresist Exposure and Development Simulation,
Proceedings SISPAD 96 Conf., (2.-4. September 1996, Tokyo), pp.99-100.

[V3] Bohmayr W., Burenkov A., Lorenz J., Ryssel H., Selberherr S.,
Monte Carlo Simulation of Silicon Amorphization During Ion Implantation,
Proceedings SISPAD 96 Conf., (2.-4. September 1996, Tokyo), pp.17-18.

[V2] Tuppa W., Selberherr S.,
A CASE-Oriented Configuration Management Agent,
Proceedings IASTED Intl. Conf. on Artificial Intelligence, Expert Systems and Neural Networks (19.-21. August 1996, Honolulu), pp.368-371.

[V1] Selberherr S.,
The MINIMOS Simulator and TUV Perspective on TCAD,
Computer-Aided Design of IC Processes and Devices, (7.-8. August 1996, Stanford), (invited).

Papers in Journals and Books

[P5] Kirchauer H., Selberherr S.,
Three-Dimensional Photolithography Simulation,
IEEE Trans. Semiconductor Technology Modeling and Simulation, http://www.ieee.org/journal/tcad/, No.6, June 1997.

[P4] Simlinger T., Brech H., Grave T., Selberherr S.,
Simulation of Submicron Double-Heterojunction High Electron Mobility Transistors with MINIMOS-NT,
IEEE Trans. Electron Devices, Vol.ED-44, No.5, pp.700-707, 1997.

[P3] Pichler C., Plasun R., Strasser R., Selberherr S.,
High-Level TCAD Task Representation and Automation,
IEEE Trans. Semiconductor Technology Modeling and Simulation, http://www.ieee.org/journal/tcad/, No.5, May 1997.

[P2] Wasshuber C., Kosina H.,
A Single-Electron Device and Circuit Simulator,
Superlatt. Microstr., Vol.21, No.1, pp.37-42, 1997.

[P1] Langer E., Selberherr S.,
Prozeßsimulation: Stand der Technik,
in: Festkörperprobleme 36, edited by: Helbig R., pp.203-243, Vieweg, 1996 (invited).

Habilitation Theses

[H1] Langer E.,
Simulation von Mikrostrukturen,
Technische Universität Wien, January 1997.

Doctoral Theses

[T4] Pichler Ch.,
Integrated Semiconductor Technology Analysis,
Technische Universität Wien, March 1997.

[T3] Wasshuber Ch.,
About Single-Electron Devices and Circuits,
Technische Universität Wien, January 1997.

[T2] Tuppa W.,
VMAKE – A CASE-Oriented Configuration Management Utility,
Technische Universität Wien, October 1996.

[T1] Bohmayr W.,
Simulation der Ionenimplantation in kristalline Siliziumstrukturen,
Technische Universität Wien, September 1996.

Master's Theses

[D6] Standfest M.,
Numerische Berechnung der Zustandsdichte von Halbleitern,
Technische Universität Wien, May 1997.

[D5] Nebenführ P.,
Implementierung eines Schaltungs-Editors im OSF/Motif-Widget-Set,
Technische Universität Wien, May 1997.

[D4] Leitner H.,
Erweiterung eines graphischen Editors zum Entwurf dreidimensionaler Halbleiterstrukturen,
Technische Universität Wien, January 1997.

[D3] Starnberger K.,
Interpolationsbasierte Modellierung von MOS-Transistoren,
Technische Universität Wien, October 1996.

[D2] Binder T.,
Erstellung einer 3D Geometrie Support Library für das PIF-Fileformat,
Technische Universität Wien, October 1996.

[D1] Baldemair R.,
Numerische Verfahren zur Darstellung von Energiebändern in Halbleitern,
Technische Universität Wien, September 1996.

Industrial Sponsors

(alphabetical order)

Austria Mikro Systeme	Unterpremstätten
Christian Doppler Forschungsgesellschaft	Wien
Digital Equipment	Hudson, USA
Hitachi	Tokyo, Japan
Intel	Hillsboro, USA
LSI Logic	Milpitas, USA
Motorola	Austin, USA
National Semiconductor	Santa Clara, USA
NEC	Sagamihara, Japan
Philips	Eindhoven, The Netherlands
Siemens	München, Germany
Siemens EZM	Villach
Sony	Atsugi, Japan