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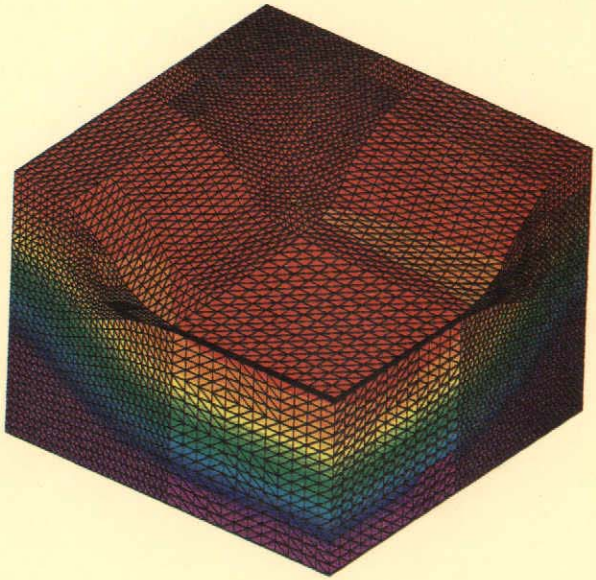

Annual Review
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INSTITUT FÜR MIKROELEKTRONIK
Technische Universität Wien
Gußhausstraße 27 – 29
A – 1040 Wien
AUSTRIA

Tel: *43/1/58801/3850
Fax: *43/1/5059224

Staff

Robert Bauer	Dipl.–Ing., Dr.	(–Dec. 31, 94)
Walter Bohmayr	Dipl.–Ing.	
Franz Fasching	Dipl.–Ing., Dr.	(–Dec. 31, 94)
Claus Fischer	Dipl.–Ing., Dr.	(–Jan. 31, 95)
Peter Fleischmann	Dipl.–Ing.	(Dec. 1, 94 –)
Michael Hackel	Dipl.–Ing.	
Stefan Halama	Dipl.–Ing., Dr.	(–Aug. 31, 94)
Ewald Haslinger		
Goran Kaiblinger-Grujin	Dipl.–Ing.	(Jan. 1, 95 –)
Manfred Katterbauer		(Feb. 1, 95 –)
Heinrich Kirchauer	Dipl.–Ing.	(Dec. 1, 94 –)
Martin Knaipp	Dipl.–Ing.	(Aug. 1, 94 –)
Christian Köpf	Dipl.–Ing.	
Hans Kosina	Dipl.–Ing., Dr.	
Erasmus Langer	Dipl.–Ing., Dr.	
Ernst Leitner	Dipl.–Ing.	
Rui Martins	Dipl.–Ing.	(Oct. 1, 94 –)
Robert Mlekus	Dipl.–Ing.	(Dec. 1, 94 –)
Christoph Pichler	Dipl.–Ing.	
Richard Plasun	Dipl.–Ing.	(Feb. 1, 95 –)
Helmut Puchner	Dipl.–Ing.	
Mustafa Radi	Dipl.–Ing.	(Aug. 1, 94 –)
Gerhard Rieger	Dipl.–Ing.	
Martin Rottinger	Dipl.–Ing.	(Nov. 1, 94 –)
Rainer Sabelka	Dipl.–Ing.	(Jan. 1, 95 –)
Gerhard Schrom	Dipl.–Ing.	
Siegfried Selberherr	O.Univ.Prof., Dipl.–Ing., Dr.	
Thomas Simlinger	Dipl.–Ing.	
Andreas Steidl	Ing.	(–Nov. 30, 94)
Martin Stiftinger	Dipl.–Ing., Dr.	(–Dec. 31, 94)
Ernst Strasser	Dipl.–Ing., Dr.	(–Dec. 31, 94)
Rudolf Strasser	Dipl.–Ing.	(April. 1, 95 –)
Walter Tuppa	Dipl.–Ing.	
Christoph Wasshuber	Dipl.–Ing.	(April 1, 95 –)
Renate Winkler		

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Preface

Siegfried Selberherr

This brochure is the seventh annual research review of the Institute for Microelectronics. The staff supported by the Austrian Ministry of Science, Research and Art consists of eight full time employees: the head of the institute, four scientists, a secretary and two technical assistants. Twenty additional scientists are funded through scientific projects!

This year we have been directly funded by the European Union for the first time for participation in two ESPRIT projects, namely ADEQUAT II[1] and PROMPT[2]. We are also glad to report that an additional industrial partner, namely LSI LOGIC in Milpitas, USA, directly supports our institute.

The projects of the institute are, in a continuation of our previous work, focused on microelectronics modeling issues. Regarding academic and scientific output we are quite satisfied. We are particularly proud of the number and quality of the doctoral and master's theses which have been completed this year.

We offer additional information about the institute through our hypertext server with the URL:

`http://www.iue.tuwien.ac.at/`

Comments are greatly appreciated.

[1]Advanced Developments for $0.25\mu m$ CMOS Technologies

[2]Process Optimization in Multiple Dimensions for Semiconductor Technology

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the Technical University of Vienna in 1978 and 1981, respectively. Since that time he has been with the Technical University of Vienna as professor. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. He has been the head of the 'Institut für Mikroelektronik' since 1988. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of the organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Trajectory Split Method for Monte Carlo Simulation of Ion Implantation

Walter Bohmayr

The traditional Monte Carlo approach for crystalline targets is based on the calculation of a large number of "distinct" ion trajectories, i.e. each trajectory is usually followed from the ion starting point at the surface of the target up to the stopping point of the ion. Since the majority of ion trajectories end at the most probable penetration depth, the statistical noise of regions with a dopant concentration several orders of magnitudes smaller than the maximum (in the following we call these areas "peripheral") cannot be tolerated and we have to increase the *total* number of calculated ions. This action, however, leads to a considerable demand for computer resources.

Therefore we have developed the *trajectory split method* for the Monte Carlo simulation of ion implantation which drastically reduces the computational effort and is applicable to two- and three-dimensional simulations. The fundamental ideas of our new simulation approach are to locally increase the number of calculated ion trajectories in areas with large statistical uncertainty and to utilize the information we can derive from the flight path of the ion up to a certain depth inside the target. For each ion, the local dopant concentration C_{loc} is checked at certain points of the flight path (*checkpoints*). At each checkpoint we relate C_{loc} to the current maximum global concentration $C_{max,current}$ by calculating the ratio $C_{loc}/C_{max,current}$. The result is compared with given relative concentration levels (we define ten levels at 0.3, 0.09, 0.027, ..., 0.3^{10}). Only if the

current local concentration in an interval falls below the previous one, a *trajectory split point* is defined at this checkpoint.

Therefore our approach is a self-adaptive algorithm because more split points are defined at areas with unsatisfying statistical accuracy. Additional trajectory branches are suppressed if an ion moves from lower to higher local concentration levels. We store the position of the ion, its energy as well as the vector of velocity, and use this data for virtual branches of ion trajectories starting at this split point.

Using this method the peripheral areas of the dopant concentration are represented by a much higher number of ion trajectories and the statistical noise is reduced. As a result, the time required to perform a simulation with comparable statistical accuracy is generally reduced by a factor of three to five in comparison to the standard approach.

Walter Bohmayr was born in Steyr, Austria, in 1969. He studied electrical engineering and computer science at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in industrial electronics and control theory in 1993. Since that time he has been with the 'Institut für Mikroelektronik' at the Technical University of Vienna as doctoral student. His work is focused on physical and mathematical models and algorithms for three-dimensional process simulation in integrated circuit fabrication.

Delaunay Mesh Generation in Three-Dimensional Space

Peter Fleischmann

The discretization of an input geometry plays a key role in today's CAD applications. A proper grid is needed to achieve satisfying solutions of the underlying equations. The Delaunay tetrahedrization is a well- known tesselation of the input geometry that improves the quality of the grid elements and hence the convergence of the subsequent solver. In fact, the frequently used Box integration method (e.g. in semiconductor device simulation) requires a Delaunay tetrahedrization of the integration domain.

So far, this issue has been neglected due to the use of structured grids. For instance, it poses no difficulty to obtain a Delaunay tetrahedrization of grid nodes which are derived from an ortho-product grid. However, with the increasing demand on efficiency, especially in three-dimensional space, a general unstructured Delaunay mesh generator becomes necessary.

The underlying concept of the mesh generator consists of the two steps of placing grid nodes and afterwards linking the combined set of geometry vertices and grid nodes. There is no limitation on the location of the grid nodes, thus offering the highest flexibility in dealing with global and local grid criteria and generating unstructured grids.

A step called boundary refinement ensures that the boundary edges and boundary faces (triangles) are conform with the Delaunay tetrahedrization of the entire point set. This step has to be applied to the interfaces within the geometry as well.

It checks the Delaunay criterion for the given triangles and inserts additional nodes where necessary.

An incremental algorithm has been implemented which performs the Delaunay tetrahedrization of any point set. In the presence of refined boundary triangles the algorithm will tesselate only the interior of the given geometry. Furthermore, the algorithm allows the re-tetrahedrization of a given subregion of the domain. In semiconductor process simulation this regridding capability plays an important role in dealing with moving boundaries. The algorithm is applicable to arbitrarily complex geometries. Due to the boundary refinement step geometry conform meshes will be generated.

Peter Fleischmann was born in Kabul, Afghanistan, in 1969. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994. He is currently working for his doctoral degree. His research interests focus on numerical grid generation and computational geometry in general.

Electron Transport and Injection in MOS Structures

Michael Hackel

Device architecture and technology, primarily for logical applications, are a challenging objective within the development of submicron field-effect transistors. Electrically Erasable Programming Read Only Memories (EEPROM) represent an important category of devices. Channel hot electrons obtained by charging the floating gate with carriers injected over the energy barrier at the Si-SiO_2 interface are exploited for cell writing. Consequently, optimized design, particularly in the case of high-density submicrometer technologies, should ideally rely on adequate modeling of electron heating. Because of the complex nonlocal nature of such phenomena, modeling of EEPROM writing has so far been largely empirical or based on oversimplified models.

As the miniaturization of MOSFETs continues there are several requirements to improve reliability of oxide damage and consequently to suppress device degradation. It has been a crucial problem to investigate gate currents from the theoretical point of view. Not only the hot-electron distribution with all its nonlocal effects has to be determined from the basic principles of physics, but also the transfer rates have to be investigated in a quantum mechanical way.

Accounting for the gate currents and the injection rates, three steps have to be considered to solve this problem in a realistic way. First, the nonlocal effects of hot carriers in the semiconductor have to be considered by a Monte Carlo simulator. As electrons in high electric fields gain energies ex-

ceeding $2eV$, band-structure effects must not be neglected. In contrast to a single-band model, the distribution function is shifted towards higher energies resulting in a considerable increase of the emission rate at the Si-SiO_2 interface. Second, the transmission probability for electrons reaching this interface is usually calculated by assuming an exponential function depending on the electric field as well as on the electron energy. In order to improve this transition rate the Wentzel-Kramers-Brillouin (WKB) approximation has to be used to account for the strong electric field in the oxide. Third, for thick oxides ($t_{OX} > 20nm$) there is a non-negligible fraction of carriers re-entering the channel domain of the semiconductor. As modern EEPROMs consist of floating gate oxides of rather large spatial dimensions and a very thin tunnel oxide, realistic gate current calculations have to meet all of these three requirements. For various MOS structures the injection of electrons is simulated within a Monte Carlo program and remarkable agreement between experimental data and theoretical predictions has been achieved.

Michael Hackel was born in Vienna, Austria, in 1965. He studied technical physics at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. During his studies he worked on projects in solid state physics and quantum field theory. He joined the 'Institut für Mikroelektronik' in January 1992. Currently he is finalizing his doctoral thesis. In spring 1994 he was holding a visiting research position at the 'Dipartimento di Elettronica, Informatica e Sistemistica' at the University of Bologna, Italy. His scientific interests include solid state device technology, device modeling and physical aspects of semiconductors in general.

A Physical Based Ionized Impurity Scattering Model for Monte Carlo Calculations

Goran Kaiblinger-Grujin

Ionized impurity scattering is one of the dominant scattering mechanism, especially at low temperatures or in highly doped material. Despite this fact a better description of Coulomb scattering than the classical Brooks-Herring treatment is still missing in device simulation. Brooks and Herring essentially used the so-called Thomas-Fermi-method which is of statistical nature and which mainly neglects all kinds of multiple interactions. Each scattering process is reduced to a two-body-problem between a single ionized impurity atom and the scattered electron, thus neglecting the interactions of all other impurities. Another inherent assumption is that each impurity contributes equally to the scattering rate.

Taking into account that a scattering event is a many-body-problem, which means that in a semiconductor electrons are exposed to an effective potential which is created by many impurities, we get a description of the scattering process which allows us to consider the dynamical screening of the impurities by the conduction electron cloud. With these refinements we are able to consider the correlation between the range of the effective potential of an ionized impurity in a charge cloud of conduction electrons and the transferred wave vector q. For q close to zero we get the Brooks-Herring result where the screening length is not a function of the transferred wave vector any more.

The fact that scattering processes are many-body-processes in nature has to be considered explicitly when calculating the scattering matrix element which we need to get the total scattering rate. To get analytical results we have to restrict ourselves to the three-body-problem, i.e. we suppose that a particular electron interacts only with two adjacent impurities simultaneously. It can be shown that two ionized impurities with the same charge scatter an electron more efficiently than a single one. This means that multiple scattering effects cause a decrease of the mobility of electrons if the impurities are equally charged and an increase if they are oppositely charged (dipole-scattering).

Calculations for silicon have shown better agreement than the traditional treatment, especially at higher doping concentrations. The effect of dynamical screening is even more distinct for semiconductors with a small effective mass like GaAs and at lower temperatures.

Other possible refinements to the standard treatment of Coulomb scattering are the inclusion of the second Born-approximation and electron-plasmon-scattering.

Goran Kaiblinger-Grujin was born in former Yugoslawia, in 1967. He began to study physics at the Technical University of Vienna in 1988, where he received the degree of 'Diplomingenieur' in 1993. He joined the 'Institut für Mikroelektronik' in January 1995. He is currently working for his doctoral degree. His scientific interests include semiconductor physics and Monte-Carlo methods for device modeling.

Three-Dimensional Optical Lithography Simulation

Heinrich Kirchauer

Among all technologies optical lithography has remained the dominant technology of delineating a pattern on the wafer according to a specified mask. To simulate optical lithography three physical aspects have to be considered: imaging, resist exposure-bleaching and resist development-etching. Each of these aspects requires its own simulation approach. Fortunately, they can be treated independently.

Imaging describes the illumination of a mask with monochromatic, temporally incoherent but locally coherent light. The commonly used wavelengths range from deep up to nearly ultraviolet, i.e. between 100 and 450 nanometers. The two-dimensional mask patterns to be resolved within a submicron process have a minimum feature size of about the same order. Hence, we use the physically appropriate diffraction theory of Fourier optics to calculate the incident light on the wafer surface.

The second and by far most demanding physical phenomenon is resist exposure-bleaching. The resist is a thin layer of photosensitive material on top of the wafer. It shall record the mask pattern by absorbing light energy according to the illumination of the mask. Thereby the resist bleaches and the mask pattern is transferred to a latent bulk-image. The optical properties depend on the exposure, this dependency is as usually described with Dill's three 'ABC' parameters. Since the geometrical dimensions are comparable with the used wavelength, a rigorous physical three-dimensional lithography simulator must solve

the Maxwell equations (MWEs) in a nonlinear medium. We simplify this sophisticated problem by assuming the resist to be linear and time invariant but inhomogeneous within the discrete time steps. In addition we only seek the steady state solution of the MWEs because the bleaching rate is negligible compared with the frequency of ultraviolet light. Hence we repeatedly have to solve the time-harmonic MWEs in an inhomogeneous medium. This is accomplished by continuing the simulation area periodically in lateral direction and reducing the MWEs to one second order partial differential equation (PDE) with laterally periodic coefficients. This PDE has a quasi-periodic solution, since the boundary conditions are also quasi-periodic. Therefore the coefficients of the PDE as well as the solution itself may be approximated by two truncated two-dimensional Fourier series yielding a set of coupled ordinary differential equations (ODEs) for the vertically dependent Fourier coefficients. This set of coupled ODEs is solved with the shooting method.

The last aspect is resist development-etching. The precalculated light distribution in the resist is converted to an etch rate following the well-known Kim model. The final isotropic etching process is simulated with the etch tool of PROMIS.

Heinrich Kirchauer was born in Vienna, Austria, in 1969. He studied communication engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in March 1994. After his studies he worked on a research project about statistical signal processing at the 'Institut für Nachrichtentechnik' for six months. In December 1994 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. His scientific interests include three-dimensional process simulation with special emphasis on lithography simulation.

The Influence of Temperatures on Device Models

Martin Knaipp

The influence of temperatures of both the lattice and the carriers plays an important role in the simulation of power devices. To describe the device in a proper way, all physical models such as mobility, band edge energy, effective density of states, etc. have to be made temperature-dependent. The number of different temperatures which are valid at the same time on the same point in the device depends on the model used to describe the device. If we use more than one local temperature, we assume that there exists more than one energy system. In general the energy balance among these systems is not attained immediately. In this case the electric field heats up the corresponding carrier system.

In the Drift-Diffusion Model the carrier systems are in thermal equilibrium with the lattice system. In this case we have only one valid temperature. The carriers are heated up by the electric field. In this model the energy relaxation time between the carriers and the lattice is zero. The electrons and holes transfer their energy to the lattice immediately. When we describe recombination and generation we have to consider the corresponding energy terms in the lattice heat flow equation.

In the hydrodynamic formulation a final energy relaxation time between the carriers and the lattice exists. The electrons and holes heated up by the electric field need some time to give their energy to the lattice. During this time they can move in the device as a consequence of thermal velocity. This way heat is transported to other places. We call this property 'non-

local effect'. In the present model heat is only transferred between the carrier systems and the lattice. Direct heat transfer between the electron and the hole system is not considered. Generally we obtain three different local temperatures.

In the thermodynamic formulation we can describe the chaotic movement of the electrons and holes using the statistical mechanics where we obtain energy balance equations for the carrier systems. Let us consider a device without any interconnections among the contacts. If we heat up this semiconductor device with an external heat source, the local thermal velocity of the carriers increases. Some of these carriers are pushed to regions with lower carrier temperature. In this case the thermal velocity decreases and the carriers cannot leave this region as fast as they have arrived. The carrier concentration increases and causes an electric field. The consequence is an electrical potential between two points in the device. In this formulation we can describe Thomson, Peltier and Seebeck effects in a proper way.

All these models have to be implemented into our new Device Simulator MINIMOS-NT. Therefore it is necessary to describe all important thermal effects in a physically consistent way.

Martin Knaipp was born in Vienna, Austria, in 1966. He studied technical physics at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. In August 1994 he joined the 'Institut für Mikroelektronik', where he is working for his doctoral degree. His work is focused on device simulation, especially on high temperature effects.

Mobility Modeling of III-V Semiconductor Alloys

Christian Köpf

Modern semiconductor devices often incorporate heterostructures to improve their electrical characteristics in many ways. Advanced growth technologies (MBE) have brought up devices which have found widespread application in optoelectronics (lasers, detectors) and have enhanced the capabilities of the classical transistor devices (HFETs, HBTs). The fastest of today's circuits are made of III-V compounds mostly grown on GaAs or InP substrates. Their physical properties are determined by the band structure which considerably varies with the material composition. Band edges, effective masses etc. can be modeled by low-order polynomials of the composition ratios.

Device simulation requires both accurate and computationally efficient models for the macroscopic physical quantities. Especially for the simulation of heterostructure devices band edges and discontinuities at interfaces must be modeled carefully. One of the most important parameters determining the transport properties is the carrier mobility.

Because of the nonparabolic many-valley band structure, which inhibits a closed-form derivation, the Monte Carlo technique is best suited to study high-field transport. Unlike the relaxation time approximation or Mathiessen's formula, the Monte Carlo method does not assume rigid approximations such as elastic scattering or a priori knowledge of the carrier distribution. In calculating the low-field mobility a Maxwell-

Boltzmann or Fermi-Dirac distribution function, however, is a reasonable approximation.

The mobility has been studied as a function of the lattice temperature, the concentration of ionized impurities, and the electric field for various materials, using a Monte Carlo simulator including phonon, impurity and alloy scattering mechanisms. Proper interpolation schemes over the material composition have been obtained.

In the drift-diffusion formalism the mobility is usually described by a function of the local driving force, *i.e.* the gradient of the quasi-Fermi level. In the hydrodynamic case the mobility is modeled as a function of the mean carrier energy. Consideration of stationary local energy balance – the power gained from the electric field equals the dissipation to the lattice – has given a functional dependence which is appropriate for silicon. However, in compounds this approach fails because of intervalley transfer leading to valley repopulation. Thus a modified approach is used with different functions for each valley. The total mobility is achieved by weighing the valley contributions by their energy dependent populations. This mobility-energy dependence cannot be directly verified by measurement but the Monte Carlo results clearly reproduce the velocity-field curves.

Christian Köpf was born in Vienna, Austria, in 1968. He studied communications and radio-frequency engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1993. He joined the 'Institut für Mikroelektronik' in November 1993, where he is currently working for his doctoral degree. His scientific interests include heterostructure devices, device modeling and solid state physics in general.

Hot-Hole Transport in Cubic Semiconductors

Hans Kosina

Efforts on numerical modeling of hot carrier transport published to date mainly deal with hot electrons. One reason might be that for electrons some important transport properties are readily revealed by assuming simple effective-mass band models. For holes, however, an effective mass approximation is poor even very close to the center of the Brillouin zone. Non-parabolicity is very pronounced and cannot be described by simple analytic expressions. The so-called warped-band model, which is essentially parabolic, cannot be implemented in the Monte Carlo technique without additional simplifications. Other than for electrons, overlap integrals cannot be neglected for holes.

A representation of the valence bands has been developed which is specifically tailored to the needs of Monte Carlo transport calculation. These needs include efficient calculation of the scattering integrals and a straightforward algorithm for the choice of the state after scattering. To represent the valence bands of cubic semiconductors a coordinate transformation is proposed such that the hole energy becomes an independent variable. This choice considerably simplifies the evaluation of the integrated scattering probability and the selection of the state after scattering in a Monte Carlo procedure. In the new coordinate system, a numerically given band structure is expanded into a series of spherical harmonics. This expansion technique, which is capable of resolving details of the band structure not only close to the center of the Brillouin zone

but also at the zone boundary, can be applied within an energy range of several electron-volts. Depending on the energy range and the number of spherical harmonics accounted for the model can be considered either as an improved analytical band model or as a full-band model. The numerical band structure of silicon used in this work has been computed by a nonlocal empirical pseudopotential method. Measured velocity versus field curves can well be reproduced by Monte Carlo simulations employing the new band representation and the consistent scattering rates.

Another project has been finished which deals with non-linear transport in quantum-wells. A multi-subband Monte Carlo program for AlGaAs/GaAs heterostructures has been developed. Overlap integrals needed for the scattering rates are supplied by a self-consistent Schrödinger-Poisson solver. In the very first version parabolic bands and hence parabolic in-plane dispersion relations have been assumed. To describe high-field transport more realistically the formalism will be extended to include non-parabolicity.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the Vienna Technical University in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the Technical University of Vienna. In summer 1993 he held a visiting research position at the Advanced Research and Development Laboratory at Motorola, Austin. Currently he is employed as an assistant professor in the device modeling group. His current interests include modeling of hot carrier phenomena and quantum effects in semiconductor devices and computer aided engineering in VLSI technology.

Parallelization of Program Packages for the Simulation of Semiconductor Processes and Devices

Erasmus Langer

The simulation of realistic semiconductor devices and their technological fabrication processes imply high demands on computer resources, especially concerning the needed computing power, but also the high memory requirements. In order to intensify the research capability of the simulation tools, an increase of the throughput and, therefore, an acceleration of the programs are an absolute necessity. This project is planned to be part of an interuniversitary project on high performance computing systems.

The simulation of semiconductor processes and devices is on the one hand based on the numerical time-dependent solution of a set of partial differential equations in two-or three-spatial dimensions, and on the other hand Monte Carlo-or cell-based algorithms are used. The latter are well suited for a significant acceleration by means of parallelizing. One main goal will be the development of parallel, Monte Carlo based and cell-based algorithms running on heterogeneous workstation networks or on distributed memory architectures.

The Monte Carlo method is rapidly gaining acceptance as a means for the simulation of ion implantation due to its physically-based algorithms. A well-known drawback of the Monte Carlo approach is its considerable demand for computer resources to obtain results with satisfying statistical accuracy. To utilize the facilities of Monte Carlo-based algo-

rithms the time characteristics have to be optimized. Parallelization seems to be suited best to achieve a considerable computational speed-up because a particle based simulation offers a variety of options.

Silicon dioxide is mainly used for efficient isolation of adjacent devices from each other. Knowledge of the physical processes that affect thermal oxidation is essential to optimizing the applications. Because of their complexity the physical mechanisms are not yet fully understood and until today no satisfying model has been found which fulfills all experimental conditions. One possible missing link in the thermal oxidation simulation is a lack of using coupled models between mechanical stress and the associated diffusion processes. Therefore the problem of coupled differential equations concerning diffusion and mechanical stress is simulated with a particle-based algorithm in connection with cellular automata. These extensions are also highly recommended for parallel algorithms since the coupling can be limited to a local area, and therefore can be solved on parallel computers keeping communication as limited as possible.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the Technical University of Vienna in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik', first as a research assistant and then as assistant professor. In the beginning his research field was the numerical simulation of semiconductor devices and later the excitation and propagation of electro-acoustic waves in anisotropic piezoelectric materials where he also received his doctoral degree in 1986. In 1988 he joined the newly founded 'Institut für Mikroelektronik'. Currently he is mainly working in the field of simulation and analysis of micro-structures with a focus on ultra large scaled integrated semiconductor devices and acoustic wave devices.

Three-Dimensional Simulation of Dopant Diffusion

Ernst Leitner

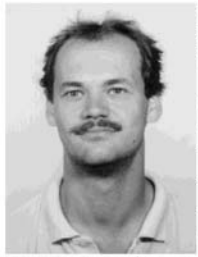
The development of today's semiconductor devices often requires the investigation of three-dimensional problems. This raises the need for process simulators capable of handling complex three-dimensional structures consisting of several materials.

The numerical solution of the partial differential equations describing dopant diffusion is usually performed using an appropriate discretization in space and time. Whereas the time domain is simple to discretize, the spatial discretization offers several challenges: The computational grid has to resolve both the geometrical domain and the impurity distributions. Furthermore, as the diffusion advances several regridding steps are necessary to combine efficient solution and controlled discretization errors.

The geometry can usually be resolved by comparably few elements. On the other hand the dopant distribution varies quite strongly so that very small elements are necessary for accurate resolution. Furthermore, distortions of the element shapes should be avoided because they cause badly conditioned equation systems. And finally, the overall number of elements should be kept as small as possible. The main idea to comply with these requirements deals with recursive refinement of the elements that are necessary for geometry resolving. But the refinement strategy has to preserve the element quality in order to avoid bad element distortions. The chosen method refines a given tetrahedron into four small tetrahedra, located

at the corners, and the remaining octahedra. For recursive refinement the octahedra are split into six small octahedra once again placed at the corners of the parent element, and eight tetrahedra filling the remaining leaks. These small tetrahedra have the same shape as the original "grandparent" tetrahedron.

Before starting the simulation itself, the grid elements are refined recursively until the resulting grid resolves the initial impurity profiles with sufficient accuracy. After each subsequent time step all elements are checked on their discretization errors and are either refined again or replaced by their parents. The solution values for newly inserted nodes are interpolated by a third order interpolation function. We estimate the discretization error by means of a 'least-square-fit' of a piecewise linear gradient to the piecewise constant gradient which is provided by the piecewise linearly approximated impurity profile. The nonlinear partial differential equations which describe the diffusion equations are approximated by the Finite Element Method using linear shape functions and a standard Galerkin weighting.



Ernst Leitner was born in Gmunden, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. In January 1993 he joined the 'Institut für Mikroelektronik' where he is currently working for his doctoral degree. In the autumn of 1994 he held a visiting research position at PHILIPS, Eindhoven, The Netherlands. His work is focused on three-dimensional process simulation, numerical grid generation, and the basic physics of transport phenomena in solids.

Interfacing Layout Mask Information with VISTA

Rui Martins

The VISTA framework supports the creation and definition of geometries that are required by its diverse applications and tools. However, it is desirable to have the possibility to import this kind of data from exterior sources, like layout data coming directly from integrated circuit design frameworks (eg. Cadence, Menthor Graphics, Magic). This will simplify the process, because VISTA does not have a dedicated tool for entering layout mask information, as it is primarily a Technology CAD framework.

The GDSII stream format is the most popular form for describing integrated circuits, supported by almost every IC design framework, and it is the natural choice for interfacing layout data with VISTA. For this purpose a converter that translates GDSII into Profile Interchange Format (PIF) has been written. As PIF is the common database format in VISTA, every tool can now principally access this data easily.

Caltech Intermediate Format (CIF) is a more recent format and is also becoming widespread in applications that manipulate geometric data. As it is a text file format and uses a simple set of graphics primitives that can be easily read and edited, a CIF to PIF converter has also been included. With the possibility of reading these two formats, VISTA can import lateral geometry data from virtually any other CAD framework.

In most cases we are not interested in the simulation of a complete layout (which requires too much computer resources). It

is important, however, to be able to select from the imported layout areas of interest (e.g. a DRAM cell or a critical transistor) that must be simulated with high accuracy, which is not offered by classical circuit simulators like SPICE, or that even require a 3-D simulation. The definition of these areas can be done within the PIF Editor (PED) in a very user-friendly way.

The input data to most of VISTA's process and device simulators is not in the wafer plane as layout is. So we must execute further steps, the most important being the application of perpendicular cuts to masks. Here PED is also used to define the cut line that specifies the plane where simulations will be carried out, the electrical contact points, and some optional measurement points. The goal is to simulate simple parts of an arbitrary layout in a completely automated manner for a given technology recipe.

Rui Martins was born in Porto, Portugal, in 1968. He studied electronics and telecommunications engineering at the University of Aveiro - Portugal, where he received the degree of 'Licenciado' in 1991 and 'Mestre' in 1994. In 1993 he joined INESC (Institute for Systems and Computers) where he worked on biomedical instrumentation. He joined the 'Institut für Mikroelektronik' in October 1994. He is currently working for his doctoral degree. His scientific interests include very low power analog and digital integrated circuit design, digital signal processing and TCAD framework aspects.

Polygonal Geometry Reconstruction after Cellular Etching or Deposition Simulation

Robert Mlekus

In two-dimensional process simulation, etching and deposition simulations are central steps. The thereby required surface advancement algorithms of the two-dimensional process simulator PROMIS are performed on a cellular geometry representation. During the simulation each of the cells contains one material type. Etching and deposition are modeled by changing the material type of some cells, leaving their geometric extensions unchanged.

Therefore, during process simulation it is necessary for each etching or deposition simulation step to discretize the original polygonal geometry, run the simulation and recalculate a final polygonal geometry representation. Former algorithms use only the final discrete geometry description to compute the final polygonal geometry. Discretization errors occur all over the geometry, demanding the regridding of every geometry conform grid defined on the original geometry. In addition discretization errors of subsequent etching or deposition simulation steps might accumulate and under certain circumstances endanger the accuracy of the whole process simulation.

To minimize these problems a cellular algorithm has been developed which generates the final polygonal geometry by combining information from the original polygonal, the original discrete and the final discrete geometry. This algorithm totally avoids any discretization errors in those parts of the geometry which are not affected by the surface movements resulting from the simulation. Therefore the extensions of the cells giv-

ing the accuracy of the discretization must only be adjusted to the minimum extensions of the affected parts of the geometry. Structures much smaller than the resolution of the discretization will keep their original shape when they are not affected by the etching or deposition simulation.

The computation of the final polygonal geometry is a two-step sequence. Firstly each cell is analyzed whether it has kept its original geometry information or whether the inside geometry parts have changed by means of etching or deposition. A provisional geometry is constructed by modifying a copy of the original polygonal geometry with simple geometric operations inside of etched or deposited cells. In a second step the structure which is thereby created is simplified and locally smoothed as far as it is not defined by parts of the original polygonal geometry.

The increased computational effort of this new algorithm can be justified by considerable savings of calculation time in following regridding algorithms as these only have to be applied in those parts of the geometry which have actually changed during the etching or deposition simulation.

Robert Mlekus was born in Tulln, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994, where he is currently working for his doctoral degree. His work is focused on object-oriented techniques for the integration of physical models into process and device simulators.

Process Flow Representation and Design Automation

Christoph Pichler

The definition and execution of multi-step process and device simulation sequences is supported by VISTA's Simulation Flow Control Module (SFC) which consists of a hierarchical, graphical point-and-click simulation flow editor, a run database for storing and retrieving output, error, and log data, and a control unit for the automatic parallel execution of simulation tasks across the network. Automatic split point detection minimizes the number of necessary computations. Complex design tasks like sensitivity analysis and parameter optimization are based on a set of task-level framework services that allow the creation, modification, and execution of process flow instances, the submission of tasks for execution, the retrieval of responses, and the persistent storage of results.

Tool integration on the data level, i.e., concerning the exchange of wafer and device data represented in the PIF format, remains a subject of research. Efficiency considerations and the rather unsatisfactory performance of certain regridding strategies indicate that the rigidly file-oriented PIF application layer might require some redesign efforts. On the control level, a tool description format is being devised that serves as a common source for the generation of system commands, input decks, and visual user interfaces. Ultimately, all simulators and auxiliary PIF tools shall be made available as a *wafer processor* module that operates as a wafer manipulation server for more complex applications.

Issues to be addressed in the future include the specification of

a lithography mask data representation, the development of an interface with existing layout editors, and the integration of independent design-of-experiments (DoE) and response-surface-modeling (RSM) modules into the framework. Based on the existing optimization capabilities, simulator calibration shall be supported more conveniently with several instances of a given tool available to the designer. Regarding the graphical user interface, the use of inflexible *panels* has to be abandoned in favor of user-definable data entry forms. Finally, the transition from a simulator-based flow representation to a more process-oriented one shall be accomplished.

Christoph Pichler was born in Vienna, Austria, in 1966. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. During his studies he held several summer trainee positions at electrical engineering companies in Austria and Switzerland. In November 1991 he joined the Engineering Design Research Center at Carnegie Mellon University where he worked on rapid prototyping and automation in manufacturing. He joined the 'Institut für Mikroelektronik' in November 1992 and is currently working for his doctoral degree. His scientific interests include engineering design, semiconductor technology, and system integration. From January to May 1995, he held a visiting researcher position at the University of California, Berkeley, working on systems aspects of three-dimensional lithography simulation.

Response Surface Models for Process Optimization

Richard Plasun

The large number of input parameters of modern semiconductor processes makes the development and optimization of new devices very CPU-time intensive. The purpose of a TCAD system is to help process designers to get better and faster surveys of the influence of the most critical process parameters. For this purpose it is possible to evaluate the dependencies between the input and the output parameters of the process or device simulator with statistical analysis and Response Surface Modeling (RSM).

However, implementers need a number of scaling factors in the program to describe the influence of different grids or simulation methods. These factors can be calibrated by evaluating a RSM and compared with measured data from a wafer fab.

This project deals with the integration of RSM into the VISTA TCAD framework. In VISTA this complex problem is separated into the following modules. The Design of Experiment (DoE) module creates a set of the input parameters in the observation parameter space which is defined by the designer. The Simulation Flow Control module (SFC) adds the split points to the process flow and handles the simulation experiments. The responses are extracted from the output of the process or device simulators and added to the experiment table. With this table the RSM module can fit the surface. Finally an optimizer extracts the critical parameters of this surface.

The DoE, RSM and optimizer modules work on a higher level than the ordinary process flow. For this reason a meta experiment language has to be designed.

In the usual approach of RSM surfaces of second order with and without cross terms are used to fit the response data. Knowledge of the relation between input and output parameters cannot be included.

New methods with an emphasis on the application of fuzzy logic models, usage of non-polynomial surfaces and special transformations for the input and output data have to be studied to increase the number of required simulator runs.

Richard Plasun was born in Vienna, Austria, in 1969. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in March 1995. He is currently working for his doctoral degree. His scientific interests include linear and nonlinear optimization and software technology.

Advanced Process Modeling in Multilayer Structures

Helmut Puchner

By decreasing the thermal budget during processing many effects have been figured out in the last years. For specific applications effects like point-defect enhancement, stacking faults or mechanical stress can no longer be ignored. The conventional process models have to be revised with state-of-the-art methods to gain new perspectives. The main problem of diffusion models developed nowadays is the insufficient verification of experimental data, because there are not enough data available or the data are measured under different process conditions. Therefore the process modeling procedures mostly capture specific problems. Nevertheless, process simulation gives a more detailed description of the "real" process than the interpretation of measured results without simulation does.

We have been developing the new process simulator PROMIS-NT to solve the diffusion problem in arbitrary two-dimensional structures. The box integration method is used to discretize the diffusion equation on a specified ortho-product or unstructured grid. Several physical models for the diffusing dopants are available, e.g. uncoupled diffusion or coupled diffusion including the Scharfetter-Gummel discretization to account for the electrostatic potential. Different models can be applied on different target materials to avoid a modeling overkill in inactive device regions.

Another important task in the simulation of diffusion processes is the initial dopant distribution by a former ion-implantation process. There are two basic methods to simulate the ion im-

plantation, first the Monte Carlo method where the flight path of a single ion is calculated and stored in boxes when the final energy is reached, and second an analytical description of the implantation process by means of probability moments. Several distribution functions can be derived from this probability moments. We have used the so-called "L-Moments" in combination with the "Four-parameter Kappa Distribution Function" for the first time in semiconductor simulation to specify the dopant profile. To resolve the arbitrary two-dimensional simulation geometry we have used a slab method where in each slab the vertical distribution function is initialized and the lateral distribution is given by a convolution integral.

All of the above activities are embedded in the VISTA project, and all the physical parameters are provided by VISTA's Material Server data base.

Helmut Puchner was born in Steyr, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in October 1992. He is currently working for his doctoral degree. From 1988 to 1990 he held summer positions in Switzerland and Germany working on control engineering. His research interests include process-simulation in poly-crystalline silicon, general diffusion processes and grid generation for nonplanar device structures.

Simulation of Thermal Oxidation in 3D-Silicon-Structures Using Cellular Automata

Mustafa Radi

Thermal oxidation of silicon, which is one of the most important steps in the fabrication of highly integrated electronic circuits, is mainly used for efficient isolation of adjacent devices from each other. Knowledge of the physical processes that affect thermal oxidation is essential for optimizing applications. Because of their complexity the physical mechanisms are not yet fully understood, and until today no satisfying model that matches all experimental conditions has been found.

Miniaturization of devices based on silicon technology leads to the realization of integrated structures exhibiting an increasingly complex topology. The evolution of isolation techniques using local oxidation of silicon (LOCOS) is one of the most striking examples for that purpose. In order to reduce the developing duration of such state-of-the-art technologies, two- and three-dimensional process simulation capabilities are of prime interest. Difficulties in numerical modeling of silicon oxidation arise from the necessity to ensure both a wide prediction capability and a very flexible numerical solution. The modeling accuracy involves the characterization and calibration of the mechanical thin film properties of integrated circuit materials as well as the stress-dependence of the oxidation kinetics, while the efficiency of the numerical implementation concerns its ability to handle real, complex, topological configurations within reasonable computing time.

To cope with these different requirements a set of coupled simulators has to be developed. First the diffusion-reaction behavior must be implemented in order to compute the oxidant-concentration at each time step, which is part of a particle-dynamic algorithm based on a cellular automaton. This pre-step leads to a growing oxide-layer with material deformation which can best be treated by a finite element method to describe the material's elasticity, viscoelasticity or its incompressible non-Newtonian flow at high temperatures.

Obviously the computation time and memory requirements of such a complex coupled simulation especially in three-dimensional problems will rapidly increase if no powerful numerical solver is available. Therefore, first steps to develop a fast multigrid solver, which is known as a very stable method for solving non-linear equation systems, are undertaken. Furthermore, using this kind of solver preserves all possibilities of efficient parallelization on parallel computers as well as on heterogeneous networks, which will surely be of increasing interest in the near future.

Mustafa Radi was born in Innsbruck, Austria, in 1968. He studied electrical engineering and computer science at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in electrical engineering in 1994. He joined the 'Institut für Mikroelektronik' in August 1994, where he is currently working for his doctoral degree. His research interests include developing physical models and algorithms for thermal oxidation in three-dimensional silicon structures based on particle-dynamic processes (Cellular Automata) as well as High Performance Computing and Networking(HPCN).

A Wafer-State Editor for TCAD Purposes

Gerhard Rieger

For many tasks in technology computer aided design (TCAD) frameworks there is a need for simple geometric operations like initial wafer generation or uncritical process steps that do not require the accuracy provided by large-scale numeric simulations.

The profile interchange format (PIF) editor fulfills these jobs for the Viennese integrated systems for TCAD applications (VISTA) framework. Furthermore, it provides a graphical user interface that allows to perform data processing interactively via an X Windows display.

To load and execute command files a LISP interpreter has been integrated into the PIF editor (PED). It provides geometric and user interface primitives and allows to combine basic functions for more complex editing facilities. All its data processing functions can be used in batch mode as well as interactively. In the latter mode the PED processes all events like mouse movement or menu selection by an infinite state machine that checks the input for validity and controls the appearance of the PED depending on the current mode.

The most important basic function types provided by the PED are inquiry, creation, modification, and removal. These can be applied to geometric objects and to scalar attributes. The underlying space may be one-, two-, or three-dimensional.

Most operations provided by the PED work at wafer-state level, i.e., input data as well as output data follow the semantic rules of the PIF semiconductor device specifications.

Nevertheless, it is possible to make modifications at a lower description level, e.g. for repairs of inconsistent data.

The PED has been split into a couple of different modules to make it more flexible. The `kernel` module performs data manipulations and triggers a display update if necessary. In stand–alone configuration it allows batch processing of LISP files. By adding the `view` module which converts PIF data and viewpoint specification to a sequence of graphical function calls and a module of the `device` class which provides the appropriate drawing functions, a hardcopy capability is achieved. Interactive modes are available through the `control` module which contains the state machine. Comprehensive graphical editing configuration also requires a screen- based and interactive `device` class module and the `shell` with graphical user interface elements.

With these features and the possibility of invoking external executables the PED is a powerful supplement to the VISTA framework for geometric modeling and intermediate data processing.

Gerhard Rieger was born in Vienna, Austria, in 1963. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. He joined the 'Institut für Mikroelektronik' in December 1991, where he currently works for his doctoral degree. In 1994 he held a visiting research position at SONY, Atsugi, Japan. His research interests include programming languages and compilers, software technology, geometry, and visualization.

Transient Simulation of Charge-Coupled Devices

Martin Rottinger

Charge-Coupled Devices (CCDs) have a broad field of application in optical imaging and analog signal processing. Since their invention in 1970 the performance of CCDs, such as noise reduction, photo-sensitivity, resolution and power consumption, has been improved continuously. In contrast to this development simulation of CCDs, particularly transient simulation, has not been practicable because of the high requirements on computational resources, hence only single CCD cells have been simulated.

Using our simulator, MINIMOS-NT, it is possible to simulate complex device structures with reasonable demands on computational resources. For instance, CCDs containing up to 60 gates have been simulated in two-space dimensions on a workstation equipped with 128MB of main memory.

To perform a transient simulation a controlled voltage, current or charge source may be applied on each contact of the simulated device. At every time step the respective voltage, current and charge values of each controlled contact have to be specified. The size of these specified time steps is arbitrary. To assure the desired degree of accuracy of the simulation the size of the calculated time steps is adjusted appropriately.

For transient integration a predictor-corrector method has been evaluated to be best suited for the semiconductor problem. The predictor used to estimate the size of the next time step is based on a quadratic extrapolation of the potential-

update norm. The ratio of the estimated step size and the previous step size is restricted to a maximum, the sectio aurea constant (1.618...), to limit the step size variations. With this restriction a quasi-uniform mesh is achieved which gives a second order local truncation error. After the calculation of each time step the potential update is checked. For this purpose the $L2$ norm and the infinity norm are calculated. If at least one of these norms exceeds a respective threshold, the step size is reduced by quadratic interpolation and the calculation is repeated.

In order to accurately follow the predefined contact signals it is necessary to calculate a time step at the instances used to specify the contact signals. This requires a reduction of the estimated step size to exactly match the instance and causes an increase in the total number of required time steps. Therefore the number of specified instances should be as small as possible to take full advantage of the quadratic time step estimate. To reduce the number of specified instances necessary for a sufficient representation of nonlinear contact signals a quadratic interpolation is used.

Martin Rottinger was born in Wels, Austria, in 1968. He studied communications engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in November 1994. Currently he is working for his doctoral degree. His scientific interests include solid state device technology and device modeling.

Integration of SCAP into VISTA and Three-Dimensional PIF Visualization

Rainer Sabelka

The integration of our three-dimensional capacitance analysis program SCAP (Smart Capacitance Extraction Program) into VISTA has been completed. Therefore a flexible simulator for calculating linear capacitances in two- and three-dimensional structures is available and can communicate with other process simulation modules within VISTA. Furthermore, due to the integration the simulator profits from the large variety of already existing geometry, gridding and visualization tools of the VISTA framework.

SCAP calculates capacitance values in wiring structures from the electrostatic field energy. The finite element method is used to discretize Laplace's equation to derive the potential distribution for certain applied conductor potentials. The system matrix is solved by a conjugate gradient solver, for extracting the partial capacitances a Gaussian solver is used.

The simulator now reads its input data from a PIF-file (Profile Interchange Format), including geometry, material types, resistivity and permittivity. Geometric segments with a resistivity below a configurable threshold are considered as (ideal) conductors, otherwise as insulators. Default values for the resistivity or permittivity of a specific material are obtained from the VISTA material database. The calculation grid is also read from PIF. Dirichlet boundary conditions are set for grid points at the border between conducting and insulating materials of the simulation geometry.

After the simulation run the results (potential distributions of the individual runs and partial capacitance values) are written back to the PIF-file and can be used for further analysis within VISTA.

Furthermore, a general three-dimensional PIF visualization tool has been developed. This work is based on the SCAP visualization postprocessor. The developed tool is capable of reading unstructured and tensor-product grids as well as scalar attributes (for instance electric potential, temperature) defined on these grids. Vector attributes are reduced to their Euclidean norm and the attribute values are displayed as color and can be scaled linearly or logarithmically. Furthermore, an interactive menu system has been added which uses the VUI (Vista User Interface) and the XVW (X-Windows VISTA Widget-set) libraries of VISTA. The program is event-driven and can be controlled by both mouse and keyboard. All time-consuming algorithms are interruptible. Before displaying an object an outline consisting of only a few lines is drawn. This feature is useful for the rotation of complex objects to select the desired viewpoint.

Rainer Sabelka was born in Vienna, Austria, in 1969. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in January 1995. He is currently working for his doctoral degree. His scientific interests include three-dimensional interconnect simulation of multilevel wired VLSI circuits, visualization and software technology.

Ultra-Low-Power CMOS Design

Gerhard Schrom

In recent years it has been widely accepted that the 5V standard supply voltage can no longer be maintained because of the many severe problems originating from constant-voltage scaling in the sub-micron region, hot-carrier degradation and thermal dissipation being the most severe. Lowering the supply voltage is the most efficient way to overcome these problems, thus reducing the power consumption at the same time which is an important aspect of portable equipment. A large spectrum of low-voltage (LV) products operating at 3.3V is already available on the market.

A further drastic reduction of the supply voltage V_{DD} down to several 100mV leads to ultra-low-power (ULP) CMOS technologies which feature an even better device reliability and a further reduction of the power consumption by one to two orders of magnitude at the same performance of the system. Work on ultra-low-power CMOS is done in two directions: 1) finding the absolute performance limits of ultra-low-power technologies, 2) determining the minimum changes to existing advanced industrial processes to make them ultra-low-power.

Analytical investigations of the absolute lower bounds of CMOS supply voltage V_{DD} provide the necessary information about the borderline which cannot be crossed even with an ideal CMOS process, operating the devices entirely in the subthreshold regime. For certain critical circuits like inverters, gates, and ring oscillators the lower bound for V_{DD} has been determined in multiples of the thermal voltage U_T. Assuming a minimum-transistor design with a maximum fan-in of three

the minimum V_{DD} was found to be $3.22U_T$ (83mV at 300K). For a real, i.e., a non-ideal process, the achievable minimum V_{DD} is higher, mainly because of the non-ideal gate swing $S > 63\text{mV}$ and because of statistical parameter deviations. An upper-bound estimate of this effect can be determined as $V_{DD,nonideal} = S \cdot V_{DD,ideal}$.

Previous numerical analyses have shown that a process design for $V_{DD} = 200mV$ is possible, therefore the minimum achievable V_{DD} is expected to lie in the range of $> 83\text{mV} \ldots 200\text{mV}$. Based on these results and on previous TCAD simulations a systematic investigation of ULP CMOS technology options with complete process and device simulation is done using VISTA's tools with the Simulation Flow Controller (SFC). The performance evaluation of a process is based on *circuit performance* rather than on device parameters alone. For this purpose a special VLSI performance evaluation method has been developed which is based on a table-driven device model and a simplified ring oscillator model. The resulting values for the inverter delay are accurate to within some 10% compared to full device level simulations of ring oscillators.

Gerhard Schrom was born in Mödling, Austria, in 1963. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in March 1992. During his studies he was working on software development projects in the CAD field. He joined the 'Institut für Mikroelektronik' in April 1992, where he currently works for his doctoral degree. His research interests include device and circuit simulation, circuit design and synthesis, signal and image processing, and TCAD framework aspects. In spring 1994 he held a visiting research position at HITACHI, Tokyo, Japan.

Generic Device Simulation with MINIMOS-NT

Thomas Simlinger

In recent times the advances in the development of semiconductor devices tend to more and more complex device structures. This concerns the geometrical device structure as well as the combination of different materials. For instance, high electron mobility transistors (HEMT) have conquered the area of high-frequency applications. These transistors are built from several layers of semiconductor alloys to obtain a channel with high electron mobility. But also BiCMOS devices or CCDs show complex device geometries. This provides new challenges to device simulation. Our new device simulator MINIMOS-NT is based on modern software concepts to comply with these demands. Object-oriented algorithms are featuring a discretization and equation assembly. These concepts hold for two dimensions as well as for three dimensions in space.

The basic idea of handling the complex device structures is to split the entire geometry into distinct regions. For these "segments" the material properties as well as the physical models, i.e., certain sets of partial differential equations can be defined independently. This results in a high flexibility which allows, e.g. the use of a hydrodynamic model in the channel of a high electron mobility transistor and a drift-diffusion model in the neighboring supply region. This allows the development engineer to use a complex model exactly where it is necessary and hence to alleviate the problem of superfluous high computational efforts and time consuming calculations. Nevertheless, a consistent solution for the entire device is computed.

Therefore the independent segments are linked together by interface models which account for the interface conditions. As material properties within neighboring segments are arbitrary, these properties and physical quantities show a discontinuous behavior at interfaces between segments. Algorithms modeling abrupt changes across interfaces can easily be implemented within such interface models.

For example, heterostructure devices such as high electron mobility transistors show an extremely rapid spatial change of material properties at interfaces where a wide band gap semiconductor (supply region) follows a narrow band gap semiconductor (channel). The electrons are mainly located inside the undoped channel with high electron mobility. On the drain-sided end of the channel the electrons must surmount the energy barrier between channel and supply region to reach the drain contact. This effect is explained by real space transfer, i.e., at sufficiently strong electric fields the carriers become heated and the electrons are able to surmount the barrier. Splitting the device geometry into segments allows the description of the abrupt heterojunction between channel and supply region, e.g. by using a thermionic emission model, and the use of a hydrodynamic model for the channel to account for the real space transfer by carrier heating.

Thomas Simlinger was born in Mödling, Austria, in 1963. He studied communications engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in October 1992, where he is currently working for his doctoral degree. His scientific interests include algorithms and data models, device modeling and physical aspects in general.

Semiconductor Process Characterization using Technology CAD

Rudolf Strasser

During the past decade numerous tools for the simulation of semiconductor fabrication processes and semiconductor device behavior have been developed. By means of the VISTA framework these simulators have been integrated in order to enable accurate simulations of state-of-the-art semiconductor devices.

The VISTA framework is applied to the simulation of complete industrial semiconductor processes. In contrast to only investigating isolated process steps it is possible to treat the entire fabrication process as a whole. Critical process parameters are identified using sensitivity analysis, furthermore optimization is applied to find optimal sets of process parameters. Various processes are compared with another using this evaluation environment (virtual IC Factory).

The model parameters have a strong impact on the output of a simulation. Therefore calibration is an important issue for semiconductor simulation. Before a simulation can be expected to deliver reliable results the model parameters have to be calibrated in order to match the simulated results with the physical ones. Furthermore a proper set of numerical simulation parameters (grids, accuracy parameters) has to be provided in order to deliver correct results and simulation times that are not confined to simulation tasks such as optimization.

The results of simulations will be optimized sets of control parameters (process information) reflecting the actual process. A process database will be developed in order to allow the re-

usage of this costly gained process knowledge. This process database will be the result of both simulations and experiments.

The main ingredients of device fabrication are technology data (process flow) and a sequence of lithography masks (layout), which can be imported from GDSII files. The separate treatment of technology data and mask data allows investigations of mutual dependencies of semiconductor devices and process steps, i.e., process steps which enhance the properties of one device might interfere with the process requirements of another device on the same wafer. This is of particular importance to modular process design.

To enhance the functionality of VISTA the integration and usage of as many different simulation tools as possible is desired (SUPREM IV, MINIMOS NT, SCAP). In order to allow the substitution of equivalent simulators such as PROMIS and SUPREM IV it is necessary to store the process information in a simulator-independent way. This simplifies the substitution of one simulation tool by another one, provided that it supports the same functionality.

Rudolf Strasser was born in Ried im Innkreis, Austria, in 1970. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1995. From spring 1992 to autumn 1993 he held a research position at the campus-based Engineering Center of Digital Equipment Corporation, Vienna, Austria. He joined the 'Institut für Mikroelektronik' in April 1995. He is currently working for his doctoral degree. His scientific interests include semiconductor technology multigrid methods and software engineering.

The Tool Abstraction Concept of VMAKE

Walter Tuppa

The VMAKE utility which was developed at our institute in 1993 has been enhanced by the Tool Abstraction Concept (TAC) to support a language binding between `C` and the Viennese version of XLISP (a `LISP` dialect) called VLISP. This allows an easy integration of `C` functions and constants into the VLISP kernel without knowledge of the internal data structures of the interpreter.

These extensions to VMAKE are made available by some new rules defined in the VMAKE description files.

- *Define-TAC-Target* to declare some source files in a source domain (currently only `C` is supported).
- *Create-TAC-Interface* to create the language binding code from a source domain to a target domain (currently only `VLISP` is supported).

The main advantage of this support in VMAKE is that the complex binding code (parameter checking and type conversion) is done automatically. The information for the creation of an interface code is extracted directly from the source code and the documentation of the exported functions by special comments (some extension to the documentation standard within the VISTA project).

The language interface generator supports many features of the `LISP` programming language like optional parameters and key parameters (with default values), lists and vectors as input

to C array parameters (needing two parameters in C, the array and the length parameter, NULL terminated arrays are not supported) and automatic memory management for allocated C resources (if known by TAC). The returned values of a function can be checked (failure of functions return NIL in VLISP) and multiple return values are returned in a list. Array parameters are converted back into lists for easy manipulation in VLISP. Bound constants are symbols in LISP with an unmodifyable value. All LISP names are automatically generated from the C function and constant names.

Since FORTRAN is still used as major programming language for some simulators at the institute, an interface generator between C and FORTRAN will be introduced in the near future. One problem in this binding is the different array indexing between these two languages and different values for logical TRUE and FALSE values in FORTRAN. Another problem is the passing of string parameters which can be very complex on different platforms. Finally, the name space depends on the operating system, too.

Walter Tuppa was born in Vienna, Austria, in 1966. Having received the degree of 'Diplomingenieur' in computer science from the Technical University of Vienna in 1991 and in electrical engineering in 1992, he joined the 'Institut für Mikroelektronik' in July 1991. He is working on the VISTA project. At present, he is working for his doctoral degree in electrical engineering.

Simulation of Single Electron Tunnel Devices

Christoph Wasshuber

Due to the tremendous capabilities inherent in the field of Single Electron Tunneling (SET) this technologie has gained a lot of interest in the last years. Although being still far away from producing SET devices industrially one is close enough to fabricate experimental devices and consider possible future applications and production techniques. With this technology extremely small and low-power devices can be produced, with the advantage that their basic performance parameters improve by down-scaling their spatial dimensions. In the laboratory many SET devices like transistors, memory cells, pumps, turnstils and various logic gates (NAND, NOR, ...) have already been produced and tested. The basic physical understanding has also been achieved.

In this phase, where theoretical results are experimentally verified, where new ideas in process technology and device architecture emerge, the need for a quick numerical evaluation of the proposed devices is obvious. Analytical results are only possible for the simplest devices. The aim of this project is to develope a SET device simulator which fills a part of the gap between theoretical physics and industrial production.

The approach is to use a Monte Carlo technique to simulate the tunnel events of single electrons through various arbitrarily connected tunnel junctions. The change in energy for the whole system for each possible tunnel event determines the probability of this particular event, which further determines the average time between consecutive tunnel events. A main feature of

the simulator will be the inclusion of the so called Macroscopic Quantum Tunneling of Charge (q-MQT) phenomenon. This quantum mechanical effect, is a simultaneous tunneling of two or more electrons in two or more tunnel junctions via an intermediate virtual state. Besides tunnel junctions, capacitors and ideal voltage sources, either constant, piece-wise linearly time dependent or voltage controlled, will allow simulation.

The goal is to use this simulator for the numerical verification of proposed devices and whole logic architectures, to support the improvement of these devices and to evaluate disturbing effects coming from thermal agitation and q-MQT of electrons.

Christoph Wasshuber was born in Vienna, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in March 1993. Afterwards he studied for one and a half years at the University of Tokyo, Japan, starting his doctoral research. In April 1995 he joined the 'Institut für Mikroelektronik', where he is working currently for his doctoral degree. His work is focused on device simulation, especially quantum mechanical devices.

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