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Modeling and Simulation of Thermal Annealing of Implanted GaN and SiC

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Abstract

While silicon-based power devices are approaching their limits regarding fundamental material properties, the interest in wide-bandgap semiconductors is growing. However, the most promising alternatives, such as gallium nitride (GaN) and silicon carbide (SiC), cause several challenges in the fabrication process. Whereas the SiC technology is almost in a mature state, GaN requires further research. A processing step of utmost importance for power devices is ion implantation, which has to be followed by an annealing step in order to achieve sufficient electrical activation efficiency.

This thesis addresses the challenges of GaN technology and compares them to the situation of SiC technology. In particular, the physical mechanism during the thermal annealing and the influence of process parameters (e.g., temperature and annealing time) on the electrical activation efficiency are investigated. Semi-empirical models are derived from experimental data in order to simulate GaN and SiC power device structures with closely coupled process and device simulations.

The proposed semi-empirical models are confirmed to accurately describe the electrical activation state of aluminum-, boron-, nitrogen-, and phosphorus-implanted SiC. A model extension allows to predict the steady-state activation state of silicon-implanted GaN. The models are employed within an elaborate simulation study on state-of-the-art 4H-SiC double-implanted metal oxide semiconductor field effect transistors (DMOSFETs) and GaN junction barrier Schottky (JBS) rectifiers. In particular, increasing the annealing temperature by 100 °C is found to result in a threshold voltage shift of 1.5 V in the DMOSFETs and the JBS rectifiers' specific on-state resistance is reduced by one order of magnitude for a temperature increase of 50 °C. The strong impact on the devices' characteristics corroborates the significance of modeling annealing capabilities.

Kurzfassung

Auf Silizium basierende Leistungsbauelemente nähern sich den Grenzen der fundamentalen Materialeigenschaften, wodurch das Interesse an Halbleitern mit breitem Bandabstand wächst. Die vielversprechenden Alternativen, wie Galliumnitrid (GaN) und Siliziumcarbid (SiC), stellen jedoch große Anforderungen an den Fabrikationsprozess. Während die SiC-Technologie bereits sehr weit entwickelt ist, erfordert GaN weitere Forschung. Von enormer Wichtigkeit für Leistungsbauelemente ist der Prozessschritt der Ionenimplantation, der einen nachfolgenden Annealing-Schritt benötigt, um eine ausreichend hohe elektrische Aktivierung zu erreichen.

Diese Arbeit präsentiert die Herausforderungen der GaN-Technologie und vergleicht diese mit der Situation der SiC-Technologie. Die physikalischen Mechanismen während des thermischen Annealings und der Einfluss von Prozessparametern, wie der Temperatur und der Annealing-Zeit, auf die Effizienz der elektrischen Aktivierung werden untersucht. Semi-empirische Modelle werden aus experimentellen Daten hergeleitet, um GaN und SiC Leistungsbauelemente mit eng gekoppelten Prozess- und Bauelementsimulationen zu simulieren.

Die vorgeschlagenen semi-empirischen Modelle beschreiben mit hoher Genauigkeit den elektrischen Aktivierungszustand von Aluminium-, Bor-, Stickstoff- und Phosphor-implantierten SiC. Eine Modellerweiterung ermöglicht die Vorhersage der elektrischen Aktivierung im Gleichgewicht von Silizium-implantiertem GaN. Die Modelle werden in einer aufwendigen Simulationsuntersuchung von hochmodernen doppelt-implantierten SiC Metall-Oxid-Halbleiter-Feld-effekttransistoren (DMOSFETs) und GaN Junction Barrier Schottky (JBS) Dioden angewendet. Eine Erhöhung der Annealing-Temperatur bedingt eine Verschiebung der Schwellspannung um 1.5 V in den betrachteten DMOSFETs und der spezifische Durchlasswiderstand der JBS Dioden wird um eine Größenordnung reduziert, wenn die Annealing-Temperatur um 50 °C erhöht wird. Die großen Auswirkungen auf die Kennlinien der Bauelemente unterstreichen die Bedeutung der Modellierung von Annealing-Prozessen.

Acknowledgement

One of the qualities of semiconductor physics that attracted me initially was its intricate, yet fascinating nature. When I was working on my final paper *Der Transistor und seine Anwendungen in der Digitaltechnik* on the bipolar junction transistor back in the school days, I was enthralled by the idea that sound physical understanding of the various processes in a semiconductor can lead to elegant, sometimes seemingly rudimentary, mathematical descriptions that prove to facilitate insights in the operation of something as practical as semiconductor devices. The beautiful concept of thoroughly studying nature in order to harness its complexity was a vital source of motivation to study Electrical Engineering and Information Technology.

The inspiring lecture on microelectronic device simulations by Prof. Tibor Grasser, Prof. Hans Kosina, and Michael Walzl during my bachelor's studies captured my imagination and drew me back to the world of semiconductors. The lecture turned out to be the starting point of a series of projects at the Institute of Microelectronics that I could work on. Starting with the bachelor's thesis on oxide defects and dopant positions supervised by Prof. Tibor Grasser and Michael Walzl I could learn about the different computational facets in semiconductor technology (technology computer-aided design). An internship supervised by Josef Weinbub and Lukas Gnam on high performance meshing exposed me to the numerical and geometrical challenges. Assisting Theresia Knobloch with modeling devices based on two-dimensional materials, I learned about the peculiarities and pitfalls of adapting models that were originally formulated for silicon to more exotic materials. I am indebted to everyone mentioned above for providing these possibilities.

Having experienced the professional and intellectuality stimulating working conditions at the Institute of Microelectronics I naturally approached Josef Weinbub for the master's thesis. He suggested to get in contact with Vito Šimonka, who worked on silicon carbide process simulations, which is really a 'hot' topic. During the last year I highly appreciated the fruitful and sometimes heated discussions, which were driven by Vito's exceptional energy and humor. He always was tremendously helpful in every respect, in particular, by answering my countless questions and e-mails and introducing me to the scientific world with its conferences, journal papers, etc., which culminated in contributing to a journal paper and submitting the main results of the investigations to two international conferences. I want to express my gratitude to Andreas Hössinger from Silvaco and Prof. Siegfried Selberherr, who, besides Vito and Josef, supported me in the process of optimizing the figures, the content, and the linguistic details of a professional scientific text.

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List of Acronyms

BFOM	Baliga's figure of merit
CSL	current spreading layer
CVD	chemical vapor deposition
DFT	density functional theory
DMOSFET	double-implanted metal-oxide-semiconductor field-effect transistor
HEMT	high electron mobility transistor
HTCVD	high temperature chemical vapor deposition
HVPE	hydride vapour phase epitaxy
JBS	junction barrier Schottky
JFET	junction-gate field-effect transistor
LAMMPS	large-scale atomic/molecular massively parallel simulator
LEEBI	low energy electron beam irradiation
LED	light emitting diode
MBE	molecular beam epitaxy
MOCVD	metalorganic vapour phase epitaxy
MOSFET	metal-oxide-semiconductor field-effect transistor
RIE	reactive-ion etching
RTA	rapid thermal annealing
SIMS	secondary ion mass spectroscopy
SRH	Shockley-Read-Hall (generation-recombination)
TCAD	technology computer-aided design
UV	ultraviolet

1. Introduction

Semiconductor technology is still dominated by silicon (Si), which has been established as the most important material in microelectronics due to its excellent properties that allowed to optimize the large-scale fabrication process of electronic devices and integrated circuits. The presentation of the first silicon-based transistor in 1954 [1] was succeeded by decades of intense research effort. Si today is the most understood material and therefore usually the semiconductor of choice for applications in microelectronics. However, there are specialized applications imposing specific requirements on the material properties, which cannot be accomplished by Si.

High frequency and optoelectronics applications require a direct bandgap and high electron mobilities, which is provided by group III-V compound semiconductors such as gallium arsenide and indium phosphide. In high temperature electronics, materials with wider bandgaps than Si are needed in order to overcome the temperature limit of approximately 120°C imposed by silicon. The related domain of power electronics, which involves the conversion of electric power employing semiconductor devices, demands exceptional thermal and breakdown properties [2]. Wide-bandgap semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC), offer properties that are much better suited for power electronics than Si. However, challenges in the device fabrication processes prohibit to harness the full potential of these semiconductors. Consequently, Si is still the predominant material in power electronics, nevertheless its limits are being quickly approached, which leads to intensified research efforts in wide-bandgap materials, in particular GaN and SiC [3].

Even though SiC process technology is almost in a mature state and breakthroughs in the field of optoelectronics have been achieved with GaN, sophisticated vertical current power devices [3] can only be realized with well-controlled doping by ion implantation. In order to achieve high electrical activation of the implanted dopants, a subsequent annealing step, which repairs the lattice damage introduced by the ion bombardment, is crucial. However, extremely high temperatures (i.e., SiC: > 1500°C and GaN: > 1300°C) are required, which strongly exacerbates the thermal annealing processes due to the high demands on the annealing equipment.

1.1. Focus and Scope

This work provides a better understanding of the technological and physical challenges associated with ion implantation and the subsequent annealing step in GaN and SiC. Electrical activation models are developed and discussed, improving the modeling capabilities of technology computer-aided design (TCAD; see Section 5.1) simulation tools, which are comprised of process, device, and circuit simulations. TCAD is vital to optimize electronic devices and systems by conducting parameter studies and enabling convenient simulation based predictions, minimizing the need for conventional and expansive experimental investigations. Ultimately,

the developed models are used to study the impact of annealing parameters on device characteristics, clearly highlighting the impact of electrical activation and thus the importance of this work.

1.2. Structure

This work's investigations cover a comparison of GaN and SiC process technology and a discussion of their potential for electronics applications in Chapter 2. The electrical activation of implanted dopants is governed by micro-physical processes associated with the lattice defects introduced by implantation damage. Approaches to physically model these processes are presented in Chapter 3. An annealing step is characterized by a set of process parameters, such as annealing time and temperature, which determine the activation efficiency and thus the device characteristics. In Chapter 4 an empirical transient activation model, that allows to accurately predict the activation state after ion implantation into GaN and SiC as a function of the annealing conditions, is proposed. Doped regions are essential for every semiconductor device and the controllability of electrically active dopant concentrations is crucial for highly optimized power device structures. In Chapter 5 comprehensive process and device simulations are performed in order to examine the impact of annealing process parameters on the device characteristics of state-of-the-art GaN- and SiC-based power devices.

2. GaN and SiC

With their attractive material properties the wide-bandgap semiconductors GaN and SiC are promising candidates for several fields of application in microelectronics. However, the process technology for these semiconductors has evolved differently, with SiC being in a more mature state regarding the precise control of ion implantation and annealing processes at the moment [2], [3]. Nevertheless, the revolutionary GaN-based blue light emitting diodes (LEDs) enabled power-saving white light sources¹, which found their way into many households. In this chapter the similarities and differences between GaN and SiC and their individual challenges in process technology are discussed. Special attention is drawn to the implantation and annealing steps, because of this work's focus and their importance for the fabrication of sophisticated device structures.

2.1. Material Properties

SiC The compound semiconductor SiC has been found to crystallize in a variety of structures, which are commonly referred to as polytypes. The main crystallographic building blocks are the tetrahedral bonds of the tetravalent Si and carbon (C) atoms. A polytype is characterized by a stacking sequence, which is given by the variation of the occupied lattice sites along the c-axis. More than 200 polytypes have been found, with the most important being the cubic 3C-SiC and the hexagonal 4H-SiC and 6H-SiC. Figure 2.1a shows the crystal structure of 4H-SiC with its characteristic ABCB|ABCB stacking sequence.

Even though all polytypes are characterized by a strong Si-C bond, the physical properties strongly differ between various polytypes. Due to its high electron mobility the 4H-SiC is the most commonly used for electronics applications. 6H-SiC has been thoroughly studied as well, however, the electron mobility is inferior to 4H-SiC. 4H-SiC exhibits a wide-bandgap (3.26 eV), which is indirect (as is the case for all polytypes). Figure 2.2 visualizes the bandgap and lattice constants for several commonly used semiconductors for comparison. The melting point is an excellent measure for the high temperature capabilities of a material and 4H-SiC's melting point is exceptionally high ($\approx 2800^\circ\text{C}$) [2], which is linked to the high binding energies². For power electronics the thermal conductivity and the critical field strength are vital. 4H-SiC shows excellent values with $5\text{ Wcm}^{-1}\text{K}^{-1}$ and 3.5 MVcm^{-1} , respectively [2].

¹White light sources can be realized by exciting a yellow phosphor with blue light emitted by GaN-based LEDs. The yellow phosphor emits light with a broad spectrum, which is perceived as white by the human eye [4].

²The melting point for Si is 1414°C .

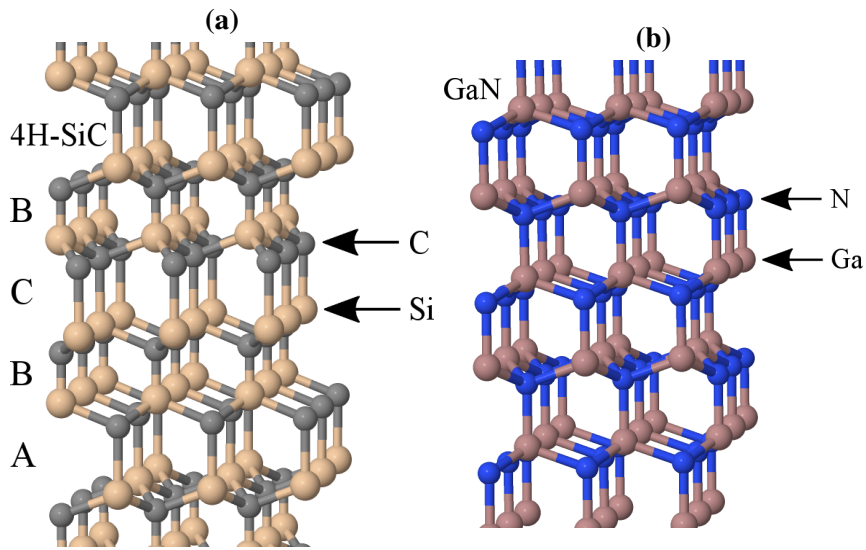


Figure 2.1.: (a) Crystal structure of 4H-SiC, which is characterized by the ABCB|ABCB stacking sequence. (b) Crystal structure of GaN, which is the wurtzite structure.

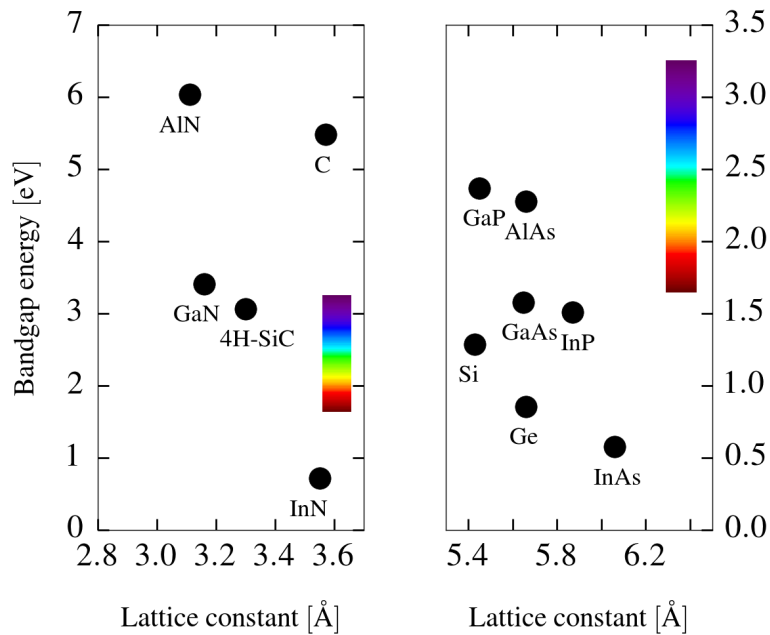


Figure 2.2.: Bandgap energy and lattice constants for commonly employed semiconductors. For materials with non-cubic crystal lattices (such GaN or 4H-SiC) the smallest lattice constant is given. The color palette illustrates the color of the emitted light that is associated with the bandgap. While the aluminum arsenide (AlAs) - GaAs alloy system allows to realize bandgap emission in the green and red spectrum, indium gallium arsenide (InGaAs) alloys are employed to realize emission in the blue spectrum.

GaN GaN crystallizes in the wurtzite structure, which is based on a hexagonal lattice. Figure 2.1b illustrates that the crystal structure is non-centrosymmetric and inherently polarized due to the net separation of the Ga^{3+} and N^- ions [5]. The non-centrosymmetric lattice causes polarization effects in GaN. Spontaneous polarization is observed along the c-axis of the Wurtzite structure, which causes a strong electric field. Additionally, piezoelectric polarization with piezoelectric constants that are ten-times higher than any other III-V semiconductors has been observed[6]–[8].

GaN's bandgap at room temperature is 3.4 eV, which is three times higher than for Si (1.1 eV). Like all III-N semiconductors, GaN is characterized by a direct bandgap, allowing highly efficient electron-photon interaction [9]. The melting point is nearly as high as for SiC with 2500 °C [10]. For GaN a critical field strength of 3.3 MVcm^{-1} is observed, however, the thermal conductivity is significantly lower than for 4H-SiC ($1.3 \text{ Wcm}^{-1}\text{K}^{-1}$) [3].

Figure 2.3 summarizes GaN's and 4H-SiC's material properties in comparison to other semiconductors, i.e., Si and gallium arsenide (GaAs), corroborating that both semiconductors, GaN and 4H-SiC, are excellently suited for application in power electronics. However, in order to exploit their full potential, well-controlled and optimized fabrication processes are required. In the following section the significant processing challenges for both semiconductors are discussed.

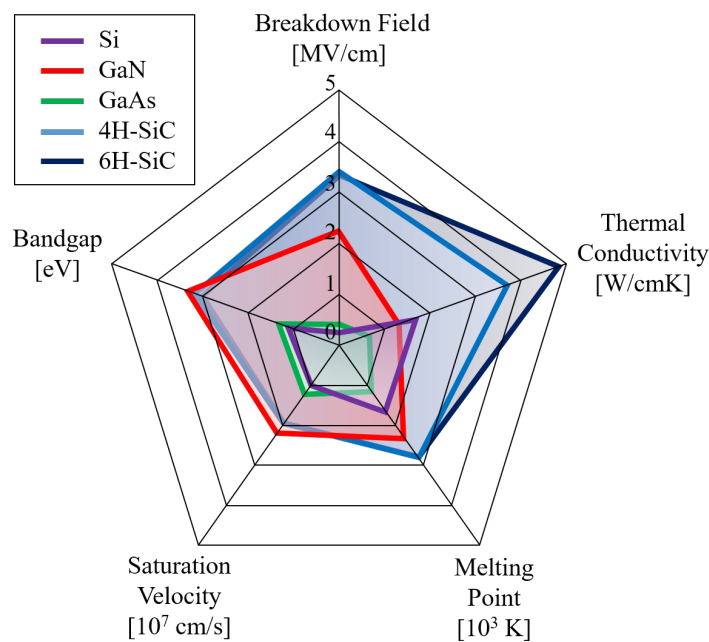


Figure 2.3.: Comparison of the material properties of Si, GaN, GaAs, 4H-SiC and 6H-SiC.

2.2. Fabrication

2.2.1. Substrate and Thin Film Fabrication

Every semiconductor device concept relies on high substrate and thin film quality, because efficient electronic transport is only possible in nearly perfect crystalline structures with low defect concentrations. From a historical point of view, breakthroughs in this field are indispensable for every semiconductor material system.

SiC substrates are fabricated using the Levy or seeded sublimation process. Both require seeds that originate the Acheson Process. Although the process was, in principle, functional in the 1970s, the defect density in the resulting substrates were problematic. The most famous extended defect is the SiC micro-pipe, which is a screw dislocation that propagates through the entire bulk. This potentially device-killing defect could be eliminated and is no longer a major concern. On the contrary, thin films can be deposited using high temperature chemical vapor deposition with process temperatures around 1600 °C [2].

Due to the fact that a process similar to the Czochralski growth for Si does not exist, GaN substrates are fabricated on top of foreign substrates (Si, sapphire). Commonly employed methods are hybrid vapor phase epitaxy (HVPE) and ammonothermal growth [11]–[13]. Compared to the well controlled Si substrates, GaN substrates exhibit a higher defect density and are more prone to contain extended defects, which severely reduce the device quality. The development of metalorganic vapor phase epitaxy (MOCVD) for the controlled fabrication of epitaxial GaN films by Akasaki and Amano [14] revolutionized GaN process technology, which culminated in the demonstration of the first GaN-based blue LED. Even though molecular beam epitaxy (MBE) can be alternatively used, MOCVD is still the standard thin film fabrication technique [3].

A special thin film fabrication technique is thermal oxidation, where the semiconductor is chemically modified near the surface. The resulting semiconductor-insulator interfaces are essential for device isolation, passivation, and gate oxide formation in metal-oxide-semiconductor field effect transistors (MOSFETs). 4H-SiC is particularly attractive regarding oxidation, as it allows for naturally growing silicon dioxide (SiO₂) - as with Si. The chemical reaction proceeds according to [15] (dry oxidation)



The native SiO₂ allows to achieve quality semiconductor-oxide interfaces with the interface state densities in the order of 10¹² cm⁻²eV⁻¹, which is significantly higher than for modern Si-SiO₂ interfaces, where values around 10¹⁰ cm⁻²eV⁻¹ are typically not exceeded [16]–[18]. Having SiO₂ as native oxide, SiC technology strongly benefits from the highly stable and extensively investigated oxide [19].

Oxidation of GaN is more involved. In an oxygen (O) rich atmosphere the off-stoichiometric native gallium oxide GaO_x is formed,



Even though thin films have been recently successfully oxidized [20], thick thermal oxides (≈ 100 nm) exhibit poor surface quality. Therefore, dielectric films (e.g., silicon oxide, silicon nitride or aluminum oxide) are preferentially deposited on GaN substrates.

A high quality substrate and precisely controlled thin film deposition/growth allows to define the semiconductor device geometry by additive processes. However, sophisticated device structures require subtractive processes as well. This is realized by the etching processes discussed in the next section.

2.2.2. Etching

In order to fabricate complex device geometries by a subtractive process, a precise control of etching technology is required. Even though wet chemical etching is possible for GaN and SiC, dry etching is better suited for industrial applications [5]. In particular, reactive-ion etching (RIE) techniques that operate with chlorine compounds are important. However, RIE typically induces lattice defects and disorder, which can be minimized by optimizing the etching process parameters. In particular, for GaN there is still room for improvement regarding plasma composition [2], [21], [22].

With thin film fabrication and etching techniques complex device geometries can be realized. However, to engineer particular electrical properties, impurities are deliberately introduced into the semiconductor. This process is called doping and is discussed in the following.

2.2.3. Doping

The basic building blocks of every electronic device are pn-junctions [23], which allow to control the electronic transport. Consequently, well-defined n- and/or p-doped regions are required. Si can be doped during growth (in situ doping), by diffusion of impurities or via ion implantation. Both 4H-SiC and GaN are characterized by small diffusion coefficients of the common impurity species, resulting in negligible impurity diffusion³. Consequently, doping by diffusion is not feasible for these materials.

Two alternatives have been established, in situ doping and ion implantation. In situ doping is essentially a modification of the thin film fabrication step. By intentionally adding impurities to the growth atmosphere, the doping concentration of the thin film can be precisely controlled. In order to fabricate deep doping profiles and sophisticated vertical device structures, ion implantation is required. Impurity ions are extracted from a gaseous source and electrostatically accelerated to high energies (keV). Subsequently, the ions are injected into the target material (e.g. GaN-substrate), where they are slowed down by nuclear and electronic scattering. An important side effect of the high energy implantation is that the host atoms are displaced, leading to severe lattice disorder, which is further discussed in Section 3.1.

³The diffusion coefficients of all relevant impurities in GaN are below $2 \times 10^{-13} \text{ cm}^2\text{s}^{-1}$ at 1400°C [24]. For SiC the coefficients are even smaller for 1700°C [2].

SiC By implanting phosphorus (P) or nitrogen (N) n-doped SiC can be achieved. Aluminum (Al) and boron (B) are used for p-type doping. Ion implantation technology for 4H-SiC has matured to the point that the implanted profiles can be precisely controlled. However, it has been observed that high dose implantation ($> 10^{15} \text{ cm}^{-2}$) is more efficient if the implantations are performed at elevated temperatures (1500°C). Due to the enhanced thermal energy the annealing process already starts during the implantation process. This phenomenon is referred to as in situ annealing [25]. Due to its small atomic radius, implanted B (in 4H-SiC) shows some peculiarities. E.g., high ionization energy (350 meV) and out diffusion during hot implantation have been observed [2].

GaN Like all III-N materials, GaN is characterized by larger binding energies and smaller inter-atomic distances than Si. Therefore, it is more difficult to incorporate substitutional impurities. Furthermore, there is a high threshold for damage accumulation, which makes GaN highly difficult to amorphize. The physical reason is the high ionicity of the Ga-N bond. Donor incorporation of Si with maximum concentrations exceeding 10^{20} cm^{-3} has been demonstrated. Alternatively, oxygen (O) also serves as donor impurity. The most commonly used acceptor impurity is magnesium (Mg) [5], [9], [10], [24], [26], [27].

The implantation process is complicated because as-grown GaN has been found to exhibit n-type background doping with an effective donor concentration of $N_D = 10^{16} \text{ cm}^{-3}$ [9]. The physical reason has been controversially discussed throughout the 1990s and early 2000s. Even though some experimental studies were indicating that N vacancies play a role, it has recently been concluded that O is unintentionally incorporated during growth contamination [28], [29]. Furthermore, magnesium-hydrogen (Mg-H) complexes play a decisive role in the unintentional dopant passivation of Mg-doped GaN [30].

Ion bombardment induces lattice damage that always requires an annealing step following ion implantation. In the next section annealing is discussed from a process technology point of view. The physical mechanisms are further examined in Chapter 3.

2.2.4. Annealing

In order to recover from the lattice damage caused by ion implantation, energy must be introduced into the host crystal. Usually, thermal energy is used, which is practically achieved by heating the implanted crystal to elevated temperatures (thermal annealing). Even though alternative anneal technologies like low energy electron beam irradiation (LEEBI) can be employed as well [31], [32], thermal annealing is the standard process.

The annealing temperatures that are required to successfully activate implanted impurities depend on the atomic binding energies and thus are related to the melting temperatures. It has been empirically determined that $2/3$ of the melting temperature results in high activation of dopants [24]. For 4H-SiC and GaN this amounts to approximately 1850°C and 1650°C , respectively, which are both extremely high and present considerable technological challenges. The annealing equipment, the substrate, and the sample are required to endure those temperatures. A rapid thermal annealing (RTA) setup, which consists of halogen lamps and reflecting cavities, allows to precisely control the temperature ramps. The most critical task is accurate temperature measurement, which is performed with pyrometers [33].

SiC For 4H-SiC substrates Si desorption from the surface and migration of surface atoms results in high surface roughnesses. These detrimental effects can be reduced by depositing a cap layer on top of the substrate. In particular, carbon caps, which are usually deposited with radio frequency sputtering, have proven successful. After the annealing step the cap can be smoothly removed by oxygen plasma etching resulting in high quality surfaces [2].

GaN The annealing process of implanted GaN is significantly more challenging. Independent of doping concentration, the substrate surface starts to severely decompose at 840°C for atmospheric pressures. N atoms are lost by forming gaseous N₂. Additionally, Ga droplets are left behind on the surface. This process is thermally activated, which causes the reaction rates to strongly increase for higher anneal temperatures, rendering thermal annealing steps without further precautions close to impossible [10]. Similar to SiC, capping layers have been observed to successfully avoid surface decomposition. Before thermal annealing a AlN, SiO₂ or SiN layer, which protects the surface, is deposited. After annealing, the cap is removed to allow further device processing [34], [35]. Figure 2.4 illustrates the typical process sequence.

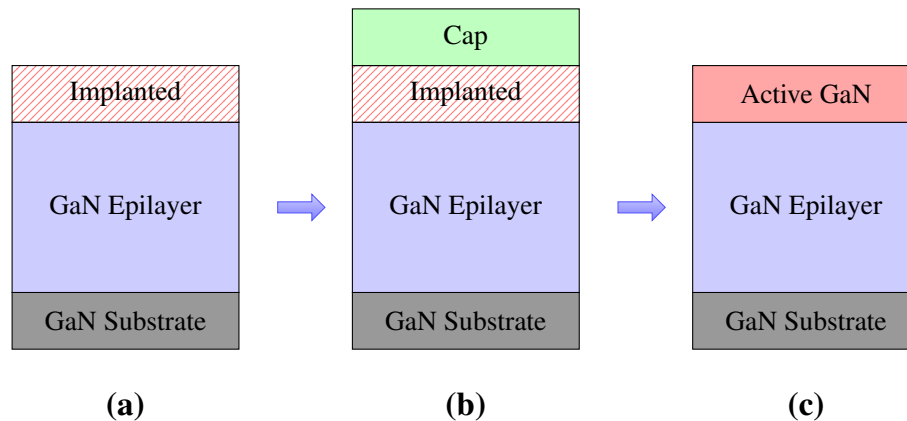


Figure 2.4.: Typical process sequence to protect a GaN sample's surface during the high-temperature annealing step. (a) The dopants are implanted into the epitaxial layer. (b) A cap layer (such as SiO₂ or AlN) is deposited and the thermal annealing step is performed. (c) After thermal annealing the implanted dopants are electrically active and the cap is removed.

The capping technology has been effectively employed to achieve a high activation efficiency in Si-implanted GaN. Annealing temperatures in the range from 1200°C to 1350°C have been realized. Strikingly, a reduced activation efficiency for low ($\approx 10^{17} \text{ cm}^{-3}$) and moderate ($\approx 10^{18} \text{ cm}^{-3}$) doping concentrations has been observed [36]–[38], which is in contrast to the full activation that is typically achieved in SiC (as discussed in Section 4.3). This phenomenon has been attributed to compensation by unintentionally introduced elements such as carbon, but is still controversially discussed in the literature [28], [38], [39].

Activation of Mg-implanted GaN (forming p-type regions) is more difficult than Si-implanted GaN. On the one hand, this is caused by background doping, which has to be compensated and thus requires enhanced acceptor concentrations. On the other hand, it has been observed that annealing temperatures above 1350°C are necessary [40]. This is linked to the formation of Mg-H complexes that do not contribute electrons to the conduction current [41]–[43]. In order

to enhance the activation efficiency, RTA procedures have been investigated, which involve two-step annealing [44] and multicycle RTA [35], [40], [45]. The fabrication techniques discussed in the previous sections provide tools to realize sophisticated semiconductor devices based on GaN and 4H-SiC. In the following, the applicability of these semiconductors for power electronics is assessed with figure of merits and characteristic device structures are discussed.

2.3. Applications

In this section a selection of the most relevant device concepts that are based on 4H-SiC or GaN are presented. In power electronics, electric power is converted using electronic circuits. The range of applications comprises AC-DC converters, automobile electronics, power supply units, factory automation, and power transmission. The growing market of electric vehicles additionally reinforces the need for efficient power conversion technologies. In Si-based power devices conversion efficiency is limited to approximately 90%, with the rest dissipating as heat, corroborating the need for an improved technology [2].

Power device structures are preferentially manufactured with a vertical device structure. This allows to place one terminal on the opposite side of the chip and thus enabling uniform current densities and high total currents [46]. In order to assess and optimize device performance figure of merits are employed. These are typically either highly significant device parameters, such as blocking voltage and on-state resistance or derived quantities. Baliga [47] introduced a derived quantity, which characterizes the influence of the material properties on the crucial on-state resistance that is associated with vertical devices. The ideal specific on-state resistance is given by

$$R_{\text{on}} = \frac{4V_{\text{B}}^2}{\epsilon_s \mu_n E_c^3} = \frac{4V_{\text{B}}^2}{\text{BFOM}}, \quad (2.3)$$

where V_{B} is the breakdown voltage, ϵ_s is the semiconductor's permittivity, μ_n is the bulk electron mobility, and E_c is the critical electric field associated with avalanche breakdown at the blocking interface (metal-semiconductor interface or pn-junction). The denominator $\text{BFOM} = \epsilon_s \mu_n E_c^3$ is commonly referred to as Baliga's figure of merit (BFOM). A semiconductor material is considered well suited for vertical power devices if the on-state resistance is small, or equivalently, BFOM is high. The relation between the BFOM calculated by Baliga for GaN, 4H-SiC, and Si is [47]

$$\text{BFOM}_{\text{GaN}} \approx 0.5 \cdot \text{BFOM}_{\text{4H-SiC}} \approx 5 \times 10^{-4} \cdot \text{BFOM}_{\text{Si}}. \quad (2.4)$$

The high values for GaN and 4H-SiC indicate the exceptional potential of these semiconductors to drastically improve the performance of Si-based power devices. Two typical vertical power device structures are the double-implanted MOSFET (DMOSFET, shown in Figure 5.1) and the junction barrier Schottky (JBS) rectifier (Figure 5.7), which are both further examined in Chapter 5.

Apart from vertical power devices, the polarization properties of GaN allow to design high performance lateral device structures. The high electron mobility transistor (HEMT), which is characterized by a two-dimensional (2D) electron gas layer, allows to increase the electron

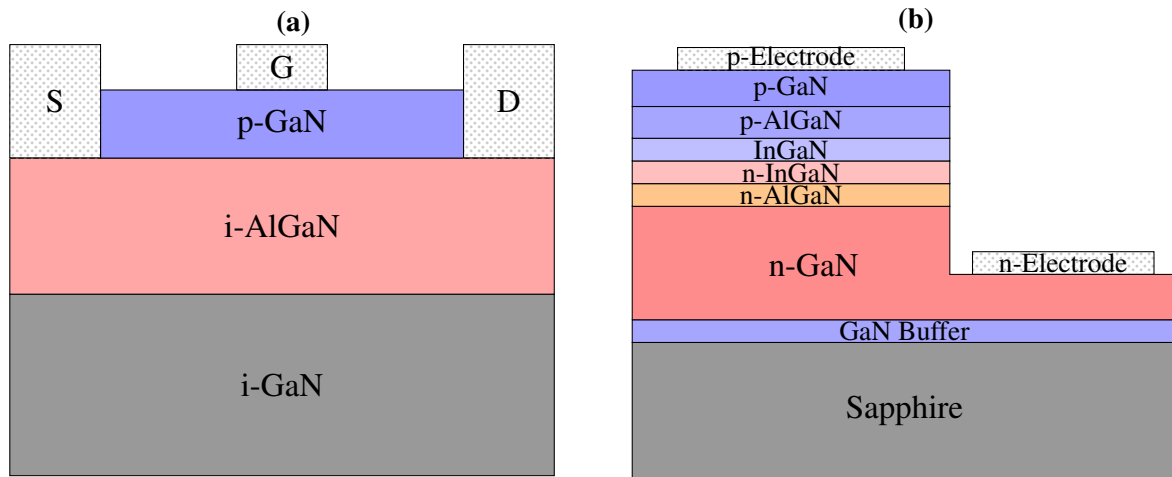


Figure 2.5.: **(a)** GaN HEMT that is based on lateral current flow [3]. S refers to the source, G to the gate, and D to the drain contact. The prefix i refers to intrinsic and p to p-doped regions. High electron mobilities are achieved by exploiting the GaN's inherent polarization at the GaN-AlGaN hetero-junction. **(b)** Schematic GaN vertical LED structure. The AlGaN and InGaN alloys can be precisely engineered to enable light emission in the UV and blue range of the spectrum. In order to grow a GaN epilayer on the sapphire substrate, an auxiliary buffer layer is deposited.

mobility to values above the bulk mobility. With high electron mobility a high switching speed can be achieved, making the structure ideally suited for high frequency applications. GaN's inherent polarization allows to form the 2D electron gas layer without resorting to additional spacer layers, which are necessary for GaAs-based HEMTs (Figure 2.5a). Lateral devices rely on heterojunctions (i.e., junctions between semiconductor with dissimilar lattice constants and bandgaps) between GaN and the alloy aluminum gallium nitride (AlGaN). The active region of a lateral device is close to the surface, which imposes less rigorous demands on the bulk crystal quality. Due to the high defect concentrations in GaN substrates, HEMTs were demonstrated earlier than vertical devices [3], [48].

A wide-bandgap semiconductor can also be applied in the field of optoelectronics and photonics. With 3.4 eV and 3.26 eV bandgaps for GaN and 4H-SiC, respectively, light generation and detection in the ultraviolet (UV) part of the electromagnetic spectrum is possible. 4H-SiC-based UV photodetectors have been successfully realized [49]. Despite having an indirect bandgap, SiC-based LEDs are commercially available, however, GaN's direct bandgap allows to realize considerably more efficient LEDs for wavelength near the visible spectrum. The demonstration of the first commercially available blue LED by Nakamura et al. in 1994 [50] marked an important milestone for the GaN technology. Figure 2.5b schematically shows a LED device structure, which uses the aluminum concentration in the AlGaN alloys to control the spectrum of the emitted light. The realization of blue GaN-based LEDs laid the foundation for efficient white light sources and was only possible with the progress in thin film deposition (MOCVD) and Mg activation technology, spearheaded by Akasaki et al. [32]. In 2014, the Nobel Prize in physics was awarded to I. Akasaki, H. Amano and S. Nakamura for *efficient blue light-emitting diodes leading to bright and energy-saving white light sources* [51].

3. Physical Mechanisms of Annealing

Thermal annealing is an important technological process step in semiconductor technology. Originating from metallurgy the term thermal annealing refers to the process of heating a material above the recrystallization temperature and subsequently cooling it down at a slow rate. Heating above recrystallization temperature allows to decrease defect concentrations and stress in the material's lattice [52]. In general, the atomic configuration in a crystal is continuously rearranging if additional energy is added to the system.

Thermal annealing is crucial for the doping of semiconductors by means of ion implantation. Due to multiple collisions the ion bombardment causes disarray in the former single crystal. A plethora of defects, most prominently point defects, is formed and referred to as implantation damage. Most importantly, the accumulated defects do not allow the introduced dopants to contribute to the electric properties of the semiconductor, which are desired to be precisely controlled by doping. As a consequence, thermal annealing after implantation is required. In this chapter the nature of the lattice damage induced by ion implantation and the physical processes leading to electrical activation are discussed.

3.1. Ion Implantation Induced Damage

When discussing the doping of semiconductors, it is of utmost importance to differentiate between the chemical concentration of dopants C_x and the electrically active concentration C_a . The former essentially counts the number of incorporated impurity atoms (e.g. Mg in GaN or Al in SiC) in a unit volume. In order to contribute to the electric properties, the impurity atoms are required to be ionized. However, this is only possible if the impurity occupies a lattice site. In order to achieve the situation of full electrical activation, where every implanted atom contributes to conductivity, the impurity atoms have to occupy lattice site and thus replace host atoms. An ideal replacement is not possible in a real system. Therefore, the achievable active donor or acceptor concentrations are limited.

3.1.1. Activation Limiting Factors

For every solid material there is a solubility limit, which is also referred to as solid solubility. This is the maximum concentration that the impurity can attain in the semiconductor (in thermal equilibrium). If the solubility limit is exceeded, agglomerates and clusters of impurity atoms are formed. In the case of high impurity concentrations it is energetically more favorable for the individual impurity atoms to form bonds to each other than to host atoms. As a consequence, a two phase system is emerging and the electrical activation saturates [42], [53].

Even if the impurity concentration is considerably below solid solubility the incorporation of impurities in configurations other than host lattice site replacements can have detrimental effects on electrical activation. Impurity atoms can occupy interstitial lattice sites or cause vacancies generated by the ion bombardment. In compound semiconductors like SiC and GaN antisite defects (e.g., N atom on Ga site in GaN) are of importance as well. Additionally, native point defects in the host crystal like self-interstitials can lead to deactivation by means of compensation. Figure 3.1 sketches the common point defects. Figure 3.2 visualizes the lattice damage that is induced by implanted Al in 4H-SiC. Point defects affect the quality of the doped layers, e.g., Ga vacancies have been identified as effective acceptors, which compensate n-type doping. Furthermore, impurity species can be unintentionally introduced during the implantation process. In GaN the compensation of p-type doping through incorporation of O during Mg implantation has been studied thoroughly [28], [29], [42].

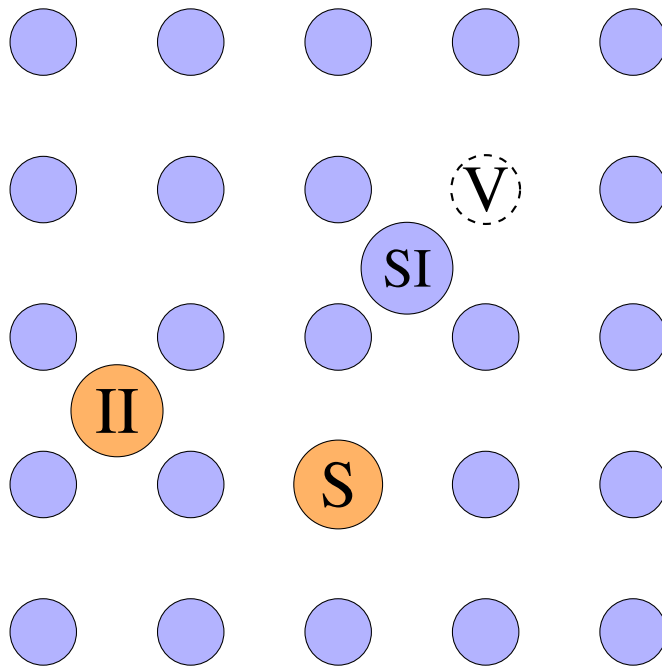


Figure 3.1.: Illustration of the fundamental point defects, i.e., interstitial impurity (II), substitutional impurity (S), native vacancy (V) and self-interstitial (SI). The host atoms are represented by the blue and impurity atoms by the orange circles.

In order to fully understand the doping process, the species contributing to the net doping have to be investigated. Typically, a combination of experimental characterization techniques and theoretical calculations is employed to examine the micro-physical impact of native and impurity-related defects. This is illustrated in the next section in an exemplary way for GaN.

3.1.2. Impurities and Defects in GaN

In Chapter 2 the challenges of achieving high activation ratios in GaN have been highlighted. The reasons for those difficulties are controversially discussed in the literature: Experimental and theoretical studies were conducted improving the understanding of the atomic configuration of doped GaN [9], [42], [55]–[58]. In this section the most important point defects in GaN are

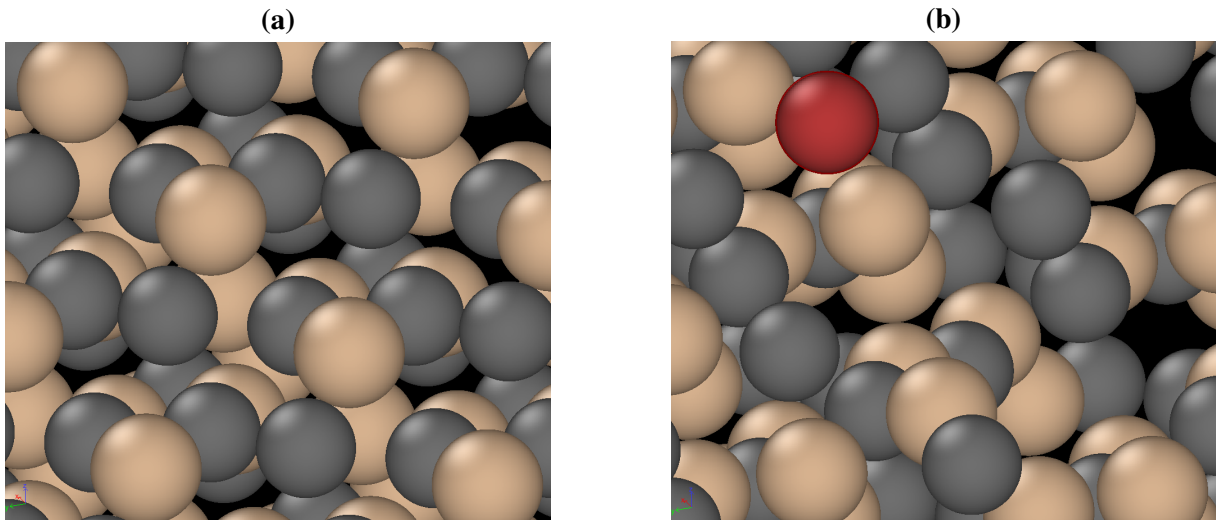


Figure 3.2.: Visualization of the implantation damage in 4H-SiC. **(a)** A perfect 4H-SiC-crystal is shown, based on a molecular dynamics simulation (large-scale atomic/molecular massively parallel simulator, LAMMPS [54]). **(b)** An impurity atom (Al, red) is implanted into the crystal and induces lattice damage.

presented in order to illustrate the typical implantation induced crystal damage in compound semiconductors.

Even though implantation damage is usually associated with deviating atomic configurations involving impurity atoms, the recoil cascade initiated by the ion bombardment leads to native point defects as well. Ga or N atoms can be pushed away from their favored lattice sites and eventually occupy a (meta)-stable position in between. This configuration is called self-interstitial and for the compound semiconductor GaN there are the Ga and the N self-interstitials (Ga_i and N_i). A Ga atom can also occupy a N site and vice versa (antisite defects - Ga_N , N_Ga). Additionally, a Ga or a N atom can leave its original, immediate surroundings and leave its lattice site behind empty, which is referred to as vacancy (V_Ga , V_N) [29].

Experimental investigations show that the typical concentrations of the different defect types strongly differ. Vacancies are present in significant concentrations even in bulk GaN, whereas antisite defects are rare. The probability of forming a certain defect type depends on the associated energy barriers which have to be overcome in order to change the atomic configuration. In theoretical studies the concept of formation energy E_D^f is used to quantify the energy barrier. Usually density function theory (DFT) calculations are employed to determine formation energies.

The N vacancy V_N came to prominence because it was regarded as being the main reason for the difficult p-type doping. Theoretical studies show that V_N acts as a shallow donor in GaN. Therefore, the intended p-type doping is compensated by the vacancies. The formation energy of N vacancies is usually high, indicating only minor concentrations in the crystal. However, in p-type GaN the formation energy is significantly smaller, which results in increased creation rates of N vacancies. The counterpart, the Ga vacancy V_Ga is responsible for yellow luminescence in GaN. Even though GaN's bandgap suggests photon emission in the UV, the Ga

vacancy introduces additional states allowing optical transitions around 2.1 eV [29], [42], [57], [59].

The self-interstitials N_i and Ga_i together with the antisite defects N_{Ga} and Ga_N are characterized by a significantly higher formation energy, which is caused by the strong distortion in the lattice. Nevertheless, depending on the position of the Fermi level these defects may act as acceptors or donors (amphoteric defects), which adds a further degree of complication, especially in high temperature conditions [42].

Donor incorporation in GaN has been successfully achieved using ion implantation of silicon. Due to the similar atomic radius, the Ga site is favorable for a Si atom (Si_{Ga}). On the contrary, the N site (and additionally the N interstitial configuration) are energetically unfavorable. Therefore, it is very likely that implanted Si atoms are incorporated at the desired lattice site. There are, however, further elements that lead to unintentional incorporation of donors. O has been established as being the main reason for the unintentional n-type conductivity in GaN discussed in Section 2.2.3. A potentially amphoteric dopant is C. Its significance was controversially discussed in the 1990s [60], but more recent investigations showed very high formation energies for C impurities [29], [42].

The most scientifically involved and historically impactful point defect is the Mg impurity in GaN. Mg is favorably incorporated at Ga sites Mg_{Ga} . The formation energy is low enough to enable large active Mg concentrations in GaN with the help of annealing techniques like low energy electron beam irradiation (LEEBI) or thermal annealing. However, the ionization energy is high (200 meV) and the Mg atoms form agglomerates with N atoms (e.g. Mg_3N_2) affecting the solubility limit of Mg in GaN. Additionally, a strong compensation mechanism was observed experimentally and linked to H complexes. The reduction of the concentration of compensated acceptors using LEEBI (Nakamura et al. [61]) was one of the significant breakthroughs enabling blue GaN-based LEDs [29], [42], [59].

The point defects discussed in this section can potentially all exist after an implantation step. Having described the variety of implantation-induced defects, the influence of thermal annealing has to be considered.

3.2. Thermal Annealing

Figure 3.3 illustrates the situation after ion implantation from an abstract point of view. Immediately after (or during the ongoing) implantation the (crystal-) system is in a non-equilibrium state. The atoms (both host and impurity atoms) immediately react and relax towards a local minimum in energy, which is referred to as in situ lattice recovery. The relaxation process typically takes place at very short time scales. This phenomenon is of importance for SiC, where implantation at elevated temperature improves the final electrical activation [2].

However, in situ lattice damage recovery is typically limited by energy barriers which prevent the atoms from further reconfiguration. In order to overcome these energy barriers, additional energy can be added to system in the form of heat (e.g., thermal annealing). At higher temperatures the higher vibrational energy enables more elaborate reconfiguration. The essential difference compared to the in situ recovery process is the time scale of the reconfiguration.

These are typically in the seconds and minutes regime (for 4H-SiC even in the hours regime for high doping concentrations $> 10^{19} \text{ cm}^{-3}$ [62]) and define the required annealing times.

The atomic reconfiguration that takes place during the annealing step is a short range reconfiguration. This is in contrast to the diffusion process, which is characterized by atomistic transport over longer ranges. Nevertheless, the elevated temperature during thermal annealing magnifies the diffusion coefficients as well. In particular, the impurity diffusivity has to be taken into account. Arsenic (As) diffusion is of importance, because the associated diffusivity is high, which leads to a broadening of the implantation profile [63]. For GaN and SiC diffusion of impurity during thermal annealing is a minor issue. Except for implanted B in SiC, the diffusivity can be usually neglected.

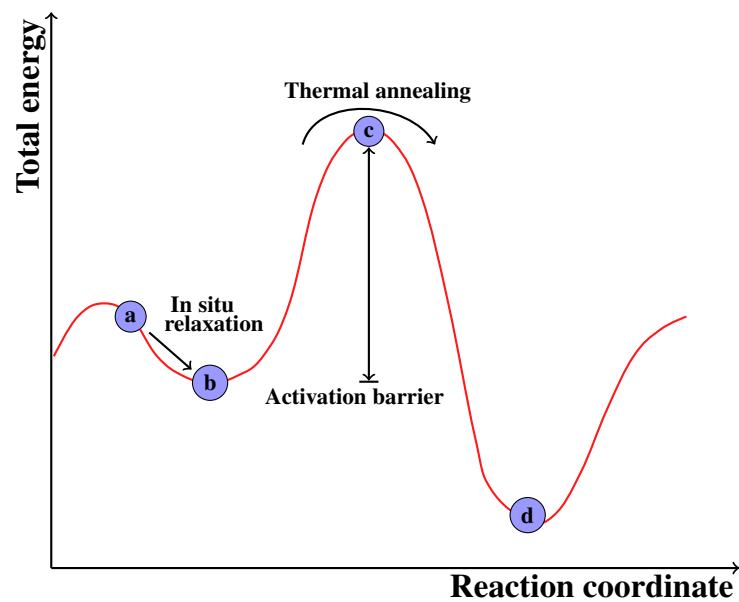


Figure 3.3.: Schematic illustration of the thermal annealing process. The implantation process induces an energetically non-favorable state (a). The system (i.e., host crystal and implanted impurities) immediately relaxes to a state that is stable in equilibrium (b). However, this state is characterized by poor electrical activation. More elaborate atomic reconfiguration is necessary to overcome the activation barrier (c). Subsequent relaxation to an energy minimum (d), which is associated with elaborate electrical activation.

A related issue is impurity cluster formation and growth for high implantation doses leading to over-saturated or amorphous region (precipitates). Due to their complexity a comprehensive physical description is difficult. However, they are highly significant, because their presence strongly deteriorates semiconductor device performance [38], [63]. The next section deals with approaches to understand the micro-physical processes that proceed during annealing steps.

3.3. Approaches to Physical Modeling

In Section 3.1.2 and Section 3.2 the mechanisms of lattice damage and thermal annealing are discussed in a very general and abstract way. In order to gain further insight into the processes related to implantation and electrical (de-)activation, it is beneficial to employ methods from

thermodynamics and physical chemistry. In this section approaches to physical modeling are summarized. Similar techniques have been successfully employed for modeling As diffusion and activation in Si [63].

3.3.1. Point Defect Reaction Equations

The key idea is to break the complex atomic reconfiguration down into simple reaction equations describing the conversions between different types of point defects. In other words, the reaction equations allow to characterize the sources and sinks of point defects in the lattice. In the following, an elemental semiconductor is assumed, i.e, there is only one type of vacancy and interstitial. This assumption facilitates the formulation of reaction equations but can be straightforwardly generalized for compound semiconductors. A vacancy V can form a dopant-vacancy pair AV with a substitutional impurity atom A . The corresponding reaction equation is



indicating the dynamic equilibrium between the individual defects and the dopant-vacancy pair. A dopant-vacancy pair can be regarded as physical entity. A similar case is the interstitial mechanism (also called kick-out reaction I)



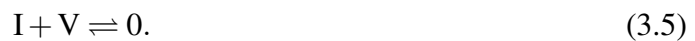
which involves an interstitial A and a dopant-interstitial pair AI . A dopant atom can also occupy an interstitial lattice site A_i , which is described by the substitutional interchange mechanism (kick-out reaction II)



Likewise, it is possible that the impurity atom 'jumps' to a vacancy (Frank-Turnbull mechanism)



Furthermore, host atoms can spontaneously move from a lattice site to an interstitial site leaving a vacancy behind (Frenkel mechanism)



In Section 3.1.2 the importance of point defect cluster formation is highlighted. An interstitial cluster can be modeled by



and the recombination of cluster with vacancies by



The reactions given above express the transition between the different neutral defect states. However, point defects can assume a charged state as well, which is of special importance for the annealing process. Due to the additional Coulomb forces, the interaction with the surrounding atomic configuration is significantly influenced. Having to describe the exact charge state is a

major complication and the involved configurations depend heavily on the considered material. To give one example, the vacancy mechanism involving charged species can be described with



where $i, j \in \{\dots, -1, 0, 1, \dots\}$ refers to the charge state of the substitutional impurity and the vacancy, respectively. During ion implantation bulk atoms are knocked off the lattice sites, thus interstitials and vacancies are created. However, this process is not an equilibrium process, which requires the Frenkel formulation (3.5) to be adapted



Additionally, the knocked-off atoms usually have enough energy to create a collision cascade and a multitude of interstitials and vacancy pairs is created. Being a non-equilibrium process, simplifying assumptions are required to be able to describe ion implantation damage within the framework of equilibrium reactions. It is commonly assumed that a perfect annealing step, which leaves only one additional interstitial (i.e, the host atom that is pushed off its lattice site) per dopant behind. For implantation with a concentration of N , the equilibrium state is modeled by [63], [64]

$$\text{num}(I) - \text{num}(V) = N, \quad (3.10)$$

where num refers to the number of interstitials or vacancies.

The reaction equations describe the transition between different potentially charged defect states. However a full description of physical state requires information about the concentration of the point defects. Statistical mechanics can provide this as it is discussed in the next section.

3.3.2. Equilibrium Concentration Modeling

When a system is considered at temperatures T above 0 K statistical mechanics predicts that a certain concentration of point defects exists in (quasi-) equilibrium. The native point defect concentration C_D depends on the formation energy E_D^f for a generic defect D and the concentration of available lattice sites C_s

$$\frac{C_D}{C_s} = \theta_D \exp\left(-\frac{E_D^f}{k_B T}\right), \quad (3.11)$$

where θ_X is the number of degrees of internal freedom of the defects on lattice sites (spin or orientation degeneracy) and k_B is the Boltzmann constant. The formation energy can be determined by resorting to ab-initio calculations (DFT, see also Section 3.1.2) or measurement techniques like positron annihilation or deep-level transient spectroscopy [64].

Having the concentration of neutral defects established, the concept of equilibrium coefficients K can be employed to determine the concentration of charged defects. Assuming Maxwell-Boltzmann statistics and relatively small defect concentrations ($C_D \ll C_s$, dilute concentration

approximation) the theory developed for neutral defects can be extended to describe charged defect configurations,

$$C_D^i = K_{D^i} C_D^0 (n_i/n)^i \quad (3.12)$$

where C_D^i is the concentration of the generic point defect D in charge state i , K_{D^i} is the reaction coefficient and C_D^0 is the concentration of the neutral charge state¹. The equilibrium theory can be employed because the electric charging processes are very fast and can be assumed to occur in quasi-equilibrium [63].

For impurity related defects, generically referred to as AD, (3.11) and (3.12) can be adapted to

$$C_{AD} = \theta_{AD} \frac{C_A \cdot C_D}{C_s} \exp\left(\frac{E_{AD}^f}{k_B T}\right) \quad (3.13)$$

and

$$C_{(AX)^i} = K_{(AX)^i} C_{(AX)^0} \left(\frac{n_i}{n}\right)^i. \quad (3.14)$$

In order to determine the total concentration of charged defects (native and impurity-related) equilibrium equations have to be formulated for every defect type and eventually summed up [64].

With the steps discussed above the concentration of every point defect type is in principle described. However, it is important to account for the spatial distribution of point defects. Similar to lattice atoms, the thermal excitation causes on the macroscopic scale diffusive behavior of the defect, allowing to apply a continuum diffusion modeling approach, which can describe the spatial distribution and temporal progression of the point defects. This is of importance for implantation damage and electrical activation modeling, because species redistribution and defect cluster formation can be described within a continuous framework, i.e., partial differential equations.

3.3.3. Diffusion Modeling - Five Stream Model

Even if the diffusion coefficients of dopants are negligibly low (as it is the case for GaN and 4H-SiC), the diffusion of native and impurity point defects affects the electrical activation processes. Point defect diffusion promotes the formation of clusters and is thus necessary to account for. In the solid state the atoms are constricted to vibrations around their lattice site, which hampers diffusion. However, in the presence of point defects, atoms can change its lattice site. Investigations of diffusion in Si crystals have shown that solid state diffusion is promoted by interstitials and vacancies. From a macroscopic point of view, steep gradients in the concentration of the diffusing species are reduced with time. This is similar to the situation in fluids. However, the diffusion coefficient in the solid state are several orders of magnitude smaller than

¹The factor n_i/n follows the Maxwell-Boltzmann statistics $\frac{n_i}{n} = \exp\left(\frac{E_f^0 - E_f^i}{k_B T}\right)$ [64].

in fluids [65]. Nevertheless, a continuum modeling approach is usually employed. For every point defect D (including impurity atoms) a continuity equation of the form

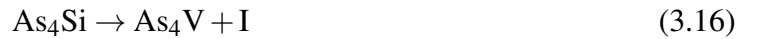
$$\frac{\partial C_D}{\partial t} = -\nabla \cdot J_D + G_D, \quad (3.15)$$

with the native point defect concentration C_D , the flux of dopants/point defects J_D , and a general generation term G_D , is used. The continuity equations describe the temporal and spatial development of the defect and dopant concentrations. For an elemental semiconductor five continuity equations have to be considered: For every dopant species three dopant related equations (A, AI, AV) and two native defect related equations (I, V). Thus, this model is referred to as Five Stream model. For compound semiconductor the different types of vacancies and interstitials (e.g. V_{Ga} , V_N , Ga_i , N_i in GaN) have to be considered as well by an additional equation for each type.

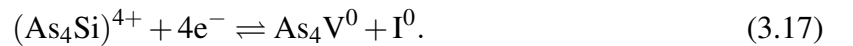
The total flux J_D is composed of a diffusion and drift component. The former is promoted by gradients in the point defect concentration and assumes the form of Fick's first law. The latter is only of importance for point defects in a charged state. An applied electric field leads to a spatial drift. Both components introduce parameters, the point defect related diffusion coefficients, which are not directly measurable. Therefore, they have to be related to the macroscopic (measurable) diffusivities. The general generation term G_D contains the information about the kinetics of point defect creation. Consequently, G_D is determined by the concentrations of the reactants and products associated with the defect reaction equations given in Section 3.3.1 [63], [64], [66].

3.3.4. Electrical Activation Modeling

The framework of the Five Stream model can be extended to account for electrical activation. From the variety of possible point defect reactions, the most important reactions that lead to electrical activation have to be established. For As activation in Si the formation of AsV clusters has been experimentally attested to be responsible for reduced activation. For instance, Mg_3N_2 clusters are associated with de-activation in GaN. Usually a multitude of cluster configurations is found experimentally. With the help of ab-initio calculations (DFT and nudged elastic band) the most energetically favorable reactions can be determined. Nevertheless, the plethora of possible reactions drastically complicates the process. To give an example, in Si the As cluster equation



has proven successful. In order to account for a cluster's impact on electrical activation the release and emission of free electrons has to be modeled as well. For the considered example this leads to



Even with the essential mechanism established, the reaction equations and the Five Stream Model contain various coefficients. Their number can be reduced by expressing them in terms of the main quantities, namely defect concentration, equilibrium coefficients, carrier concentrations, macroscopic diffusion coefficients, and binding energies. Nevertheless, their values have to be adapted in a fitting process to data from experiments. Figure 3.4 illustrates that the discussed modeling approach has been successfully employed by Fastenko [63] to reproduce the

measured saturation of electrical activation of As in silicon. While for dopant concentrations smaller than approximately $5 \times 10^{19} \text{ cm}^{-3}$ full activation can be achieved employing high anneal temperatures, the activation efficiency saturates for concentrations above this value. This can be attributed to the intensified cluster formation for high dopant concentrations.

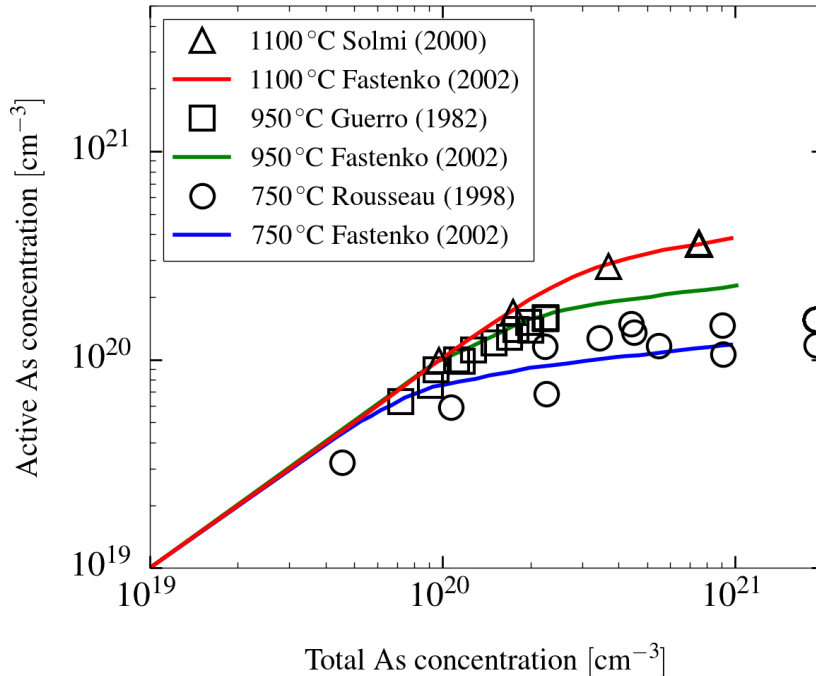


Figure 3.4.: Electrically active concentrations of As in Si as a function of the implanted concentration. The accurate simulation results that have been presented by Fastenko [63] (solid lines) demonstrate that the approach to model electrical activation on the basis of point defects is successful. Reproduced from [63].

3.3.5. Summary

The approaches of diffusion and (de)activation modeling of dopants, which have already been successfully employed for As dopants in silicon, can be adapted to apply to other materials (such as GaN) as well. The characterization of the point defects and associated reactions enables a deeper understanding of the underlying micro-physical effects that deteriorate electrical activation. However, several challenges have to be overcome in order to formulate a comprehensive model allowing predictions about the activation state:

- Experimental characterization of native and dopant-related point defects.
- Experimental investigation of additional defects introduced by semiconductor processing steps: chemical reactions (e.g. thermal oxidation) or ion-implantation (e.g., vacancy-type clusters).
- Determination of energetically favorable defect configuration and reactions using ab-initio calculation (DFT) with a special attention to the charge state of defects.

- Selection of the most important defect formation reactions based on the experimental and ab-initio calculation input.
- Formulation of the (possibly extended) Five Stream model including all important defect types.
- Determination of coefficients and binding energies by fitting to experimental data. This requires the availability of comprehensive experimental data for the considered dopant and host material, which includes diffusion-coefficients, active concentrations (transient and equilibrium values) and point defect reaction rates.
- (De-)activation modeling: Investigation of the mechanisms that limit electrical activation (e.g., clustering or compensation by unintentionally incorporated elements).

Even though a multitude of experimental studies have investigated defects in GaN and SiC, a fully physical activation model has not been developed. This can be partly attributed to the complexity that is induced by the presence of two type atoms in the respective lattices. The consequential variety of point defects presented in Section 3.1.2 gives rise to a plethora of possible micro-physical causes of reduced activation. However, further research is necessary to gain a better understanding of the micro-physical mechanisms. In the next chapter, a semi-empirical approach to model the activation process, which captures the main macro-physical properties, but does not require full knowledge about the micro-physical processes is discussed.

4. Empirical Modeling of Annealing

The description of the processes during ion implantation and thermal annealing presented in Chapter 3 allows for an understanding of the underlying mechanisms. Implantation process engineering is usually concerned with questions regarding process parameters like implantation dose, annealing time, and annealing temperature. A fully calibrated physical model is in principle capable of delivering the required information to answer these questions, however, only at the cost of high computational effort. A different approach, which is being successfully employed in many fields of semiconductor technology simulation, is the empirical modeling approach. This section highlights the general objective of the empirical method and discusses its application to model electrical activation of dopants in the wide-bandgap semiconductors GaN and 4H-SiC. Phenomenological models that allow to optimize the fundamental process parameters associated with thermal annealing are derived from experimental data for a variety of combinations of dopant atoms and host materials. Additionally, the relation between the model parameters and the micro-physical processes are examined.

4.1. Objectives of Empirical Modeling

Empirical modeling focuses on the available experimental data and draws the attention to the fundamental idea of observing nature. The development of semiconductor process aims to optimize the final device's macroscopic behavior (i.e., current-voltage characteristics, breakdown voltages, etc.) Therefore, it is a valid approach to abstract from the micro-physical complexity that is sketched in Chapter 3 and reduce everything to the macroscopic quantity electrical activation ratio R_{act} , which describes the ratio between electrically active and total dopant concentration. The main task is then to establish a functional relation (mathematical equation) between R_{act} and all relevant process parameters. This is most naturally accomplished by setting up experiments and vary the parameters of interest and determine the auxiliary coefficients of the functional relation by fitting the coefficients to the experimental results.

The empirical approach offers only limited insights about the underlying physical processes. However, for device engineering this is not a major concern. The efficient calculation of etching geometries, implantation profiles, and oxide thicknesses requires a mathematical description of the considered material properties that should be as simple as possible to facilitate shortest possible simulation times by simultaneously acceptable accuracy. Nevertheless, the parameters and coefficients appearing in the model equations can be related to physical quantities. The semi-empirical approach targets that issue by developing a greatly simplified physical model, which captures the essentials of the processes. The model predictions are subsequently compared to experimental observations and additional terms added to achieve suitable coincidence. An example from the area of oxidation is the Deal-Grove model, which describes the thermal oxidation kinetics of Si based on diffusion and reaction rates of the oxidizing species. However,

the Deal-Grove model does not satisfactorily describe oxide growth in the thin film regime, which led Massoud *et al.* to propose additional empirical terms [19], [67].

(Semi-) empirical models have the essential advantage that they provide the tools to optimize the process parameters. Especially in the industrial environment a reduction of annealing time is beneficial. With a well calibrated activation model the optimum combination of annealing time and temperature, which allows reliable device operation, can be predicted. However, accurate calibration is only possible if comprehensive experimental data is available. In the next section the experimental findings for implanted SiC and GaN are reviewed.

4.2. Review of Experimental Findings

The quality of an annealing step is characterized by the electrical activation efficiency

$$R_{\text{act}} = \frac{C_a}{C_x}, \quad (4.1)$$

which is defined as the ratio between the electrically active dopant concentration C_a and the implanted concentration C_x . The main objective is to investigate the impact of the major process parameters, i.e., annealing temperature T_A and annealing time t_A , on the electrical activation efficiency. Activation efficiency is a local quantity that cannot be directly measured. However, if implanted regions are activated with high efficiency, the region's electrical resistivity is low. This allows to determine the electrical activation efficiency from a series of resistivity measurements.

The electrical resistivity of doped semiconductors can be measured and the most commonly employed technique is the Hall-Effect measurement (van der Pauw geometry) [68], which allows to measure the sheet resistance of an implanted layer. Hall-Effect measurement are favored over simple two- or four-point current/voltage measurements, because the majority carrier mobility and the sheet carrier concentration can be determined as well. Under the assumption of full ionization of dopants (further discussed in Section 5.2.3) even the dopant concentration can be obtained, if one doping type (p or n) dominates. However, while the assumption of full activation holds for Si, this is not the case for the wide-bandgap semiconductors GaN and SiC at room temperatures. However, using the charge neutrality equation it is still possible to determine the active dopant concentration C_a [69], [70].

The implanted doping profile can be determined by secondary-ion mass spectrometry (SIMS), which is a sensitive analysis technique for the investigation of thin film composition. In particular, the chemical dopant concentration profile and thereby the implanted concentration C_x can be measured [71]. In most experiments a box profile is implanted employing multiple implantation steps, allowing to estimate an effective dopant concentration from the implantation dose. With the information about resistivity and implanted concentration it is possible to calculate the effective electrical activation efficiency of the implanted layer [30], [37].

4.3. Experimentally Obtained Electrical Activation Efficiencies

In the literature a plethora of implantation and annealing experiments with different substrates, impurities, and process conditions are discussed. Even though the micro-physical processes are different for GaN, SiC, and Si, the general dependence of activation efficiency on annealing time t_A and temperature T_A are similar. Figure 4.1a shows the characteristic activation transient for implanted Al in 4H-SiC [62]. The activation rate continuously decreases and the maximum achievable activation is only slowly reached, indicating a transient of first order. While the final activation rate $R_{\text{act}}(t_A \rightarrow \infty)$ is well defined, the initial activation efficiency $R_{\text{act}}(t_A = 0)$ is more involved. Activation efficiencies for short activation times (< 10 s) are difficult to measure, because such measurements require highly dynamic temperature profiles. For particularly elevated annealing temperatures above 1000°C for GaN and above 1500°C for SiC the examined sample can not be assumed to reside in an isothermal state after just a few seconds. In contrast, for the annealing times shown in Figure 4.1a the sample can be safely assumed to have been isothermally annealed at a well-defined annealing temperature T_A .

The annealing temperature strongly affects electrical activation. Figure 4.1b depicts a strong increase of the electrical activation within a narrow temperature band, similar to the prototypical logistic growth function

$$f(x) = A [1 + \exp(-k(x - x_0))]^{-1}. \quad (4.2)$$

The transition temperature between low and high activation strongly depends on the implanted element, which is shown by shifted curves for implanted Al and B (4H-SiC substrate). Strikingly, the slope in activation is high, which implies that raising the annealing temperature by as little as 50°C can significantly improve the electrical activation (e.g. compare $\approx 10\%$ at 1500°C vs. $\approx 78\%$ at 1550°C for Al) [2].

An experimentally obtained activation efficiency is considered as steady-state efficiency, if a prolonged annealing treatment does not raise the activation level. The steady-state is achieved when the annealing time is sufficiently long. For a given annealing temperature there is a maximum possible activation level, which depends on the implanted dopant concentration C_x . Figure 3.4 shows the characteristic saturation for As dopants in Si. The experimental data available for GaN and 4H-SiC has been collected in an extensive data study. In the following sections the transient, temperature, and concentration dependent characteristics are presented for implantation of various dopants into GaN and 4H-SiC.

4.3.1. 4H-SiC

The annealing process has been investigated for the most important dopant elements Al, B, P, and N. The collected results are visualized using two types of plots. The first plot characterizes the activation state in equilibrium (steady-state activation) assuming sufficient annealing time, resulting in the maximum possible electrical activation for the given implanted dopant concentration and annealing temperature (Figure 4.2a for implanted Al). The second plot illustrates the transient activation behavior for a constant implanted concentration (Figure 4.2b for implanted Al).

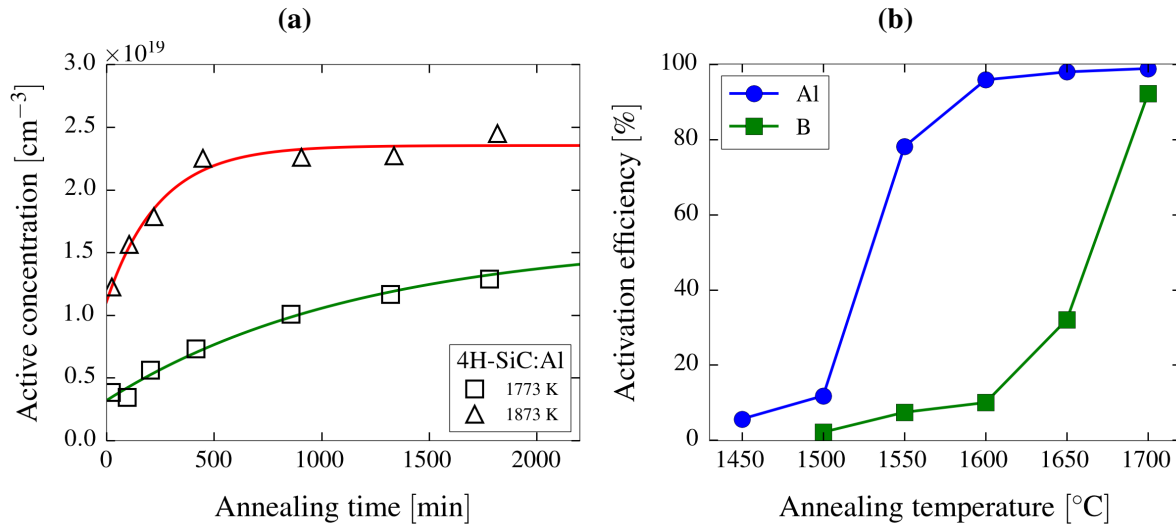


Figure 4.1.: **(a)** Typical transient of the active dopant concentration during a thermal annealing process. The activation rate is high at the beginning and subsequently is reduced as the equilibrium activation is approached. The illustrated data has been presented by Nipoti *et al.* [62] for Al-implanted 4H-SiC. **(b)** Activation efficiency of Al- and B-implanted 4H-SiC as function of the annealing temperature. The implanted dopant concentration for both species is 2×10^{18} cm⁻³. Reproduced from data presented in [2].

The most commonly implanted acceptor material for SiC, Al, is a prominent example for the general annealing behavior that is similar to Si. Figure 4.2a shows the steady-state activation of implanted Al, and Figure 4.2b shows the transient behavior for two constant implanted acceptor concentrations. The transients presented by Nipoti *et al.* [62] with an effective acceptor concentration 6×10^{18} cm⁻³ demonstrate that the time constant associated with the activation process is in the order of several hours. The data for the alternative acceptor, B, is visualized in Figure 4.3. Because B implantation presents the challenges described in Section 2.2.3, the number of studies available in the literature is considerably smaller than for Al. In particular, no comprehensive studies of the transient behavior have been conducted. Nonetheless, the steady-state experiments exhibit the characteristic saturation for high implanted concentrations [2], [72], [73].

Concerning the donors in SiC, the literature offers a multitude of investigations about P implantation. The available data is visualized in Figure 4.4a and Figure 4.4b. Being the less favorably employed donor the situation for N is comparable to B. The data for steady-state activation is significant and given in Figure 4.5 [74]–[77]. However, the activation kinetics have only been studied by Blanqué *et al.* [76], which is summarized in Table 4.1.

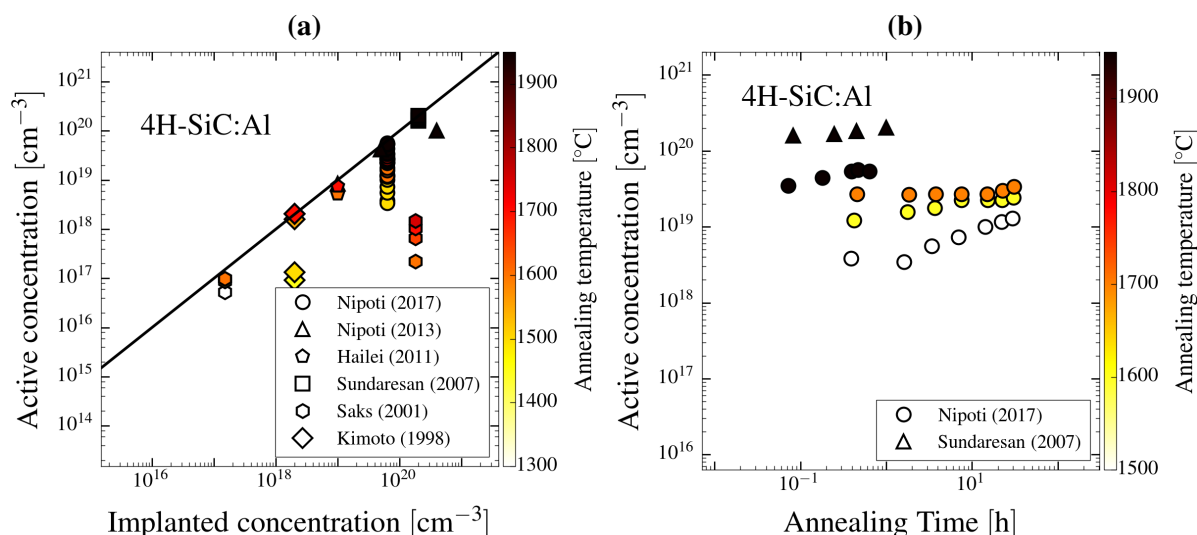


Figure 4.2.: **(a)** Experimentally observed active Al concentration after implantation into 4H-SiC and annealing in the steady-state [62], [73], [78]–[81]. **(b)** Activation transients for an effective implanted doping concentration of $6 \times 10^{18} \text{ cm}^{-3}$ implanted by Nipoti *et al.* and $2 \times 10^{20} \text{ cm}^{-3}$ by Sundaresan *et al.* The time constants are in the order of several hours and are significantly decreased for elevated annealing temperatures.

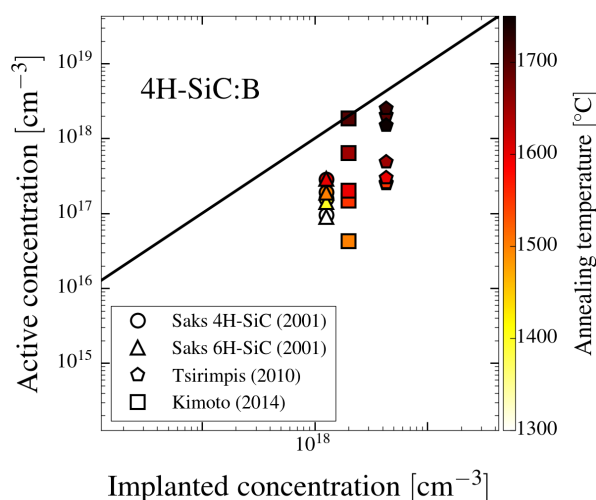


Figure 4.3.: Steady-state electrical activation of B-implanted 4H-SiC and 6H-SiC. The data is compiled from several publications [2], [72], [73]. The negligible difference between the activation states of 4H-SiC and 6H-SiC observed by Saks *et al.* [73] indicate that both hexagonal polytypes exhibit the same activation mechanisms.

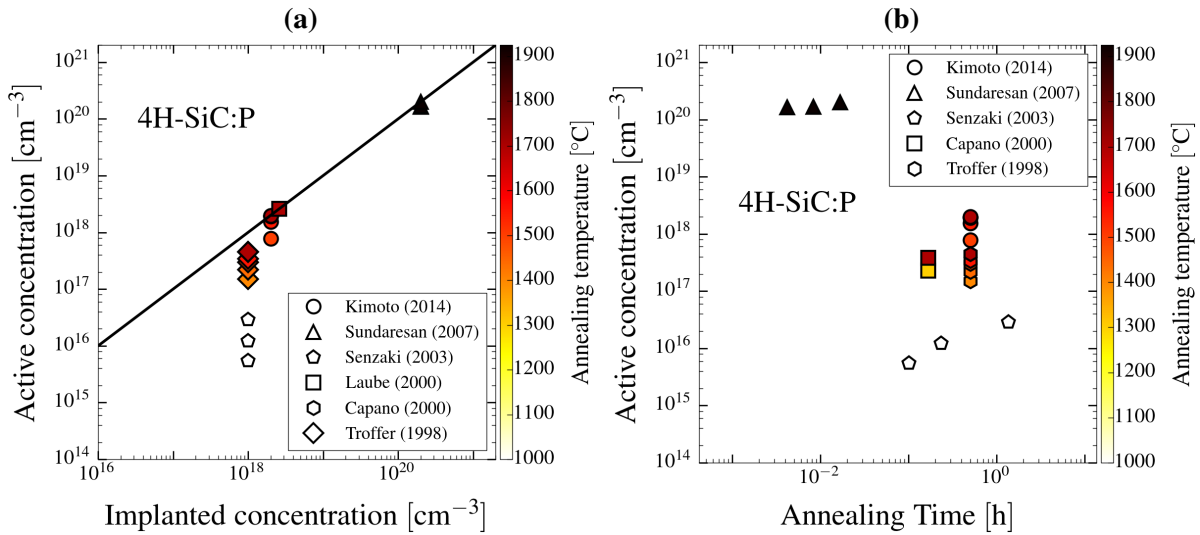


Figure 4.4.: **(a)** Steady-state electrical activation of P-implanted 4H-SiC [2], [77], [79], [82], [83]. **(b)** Activation transients for implanted P with a concentrations of $2 \times 10^{18} \text{ cm}^{-3}$ by Kimoto *et al.* and $1 \times 10^{18} \text{ cm}^{-3}$ by all others.

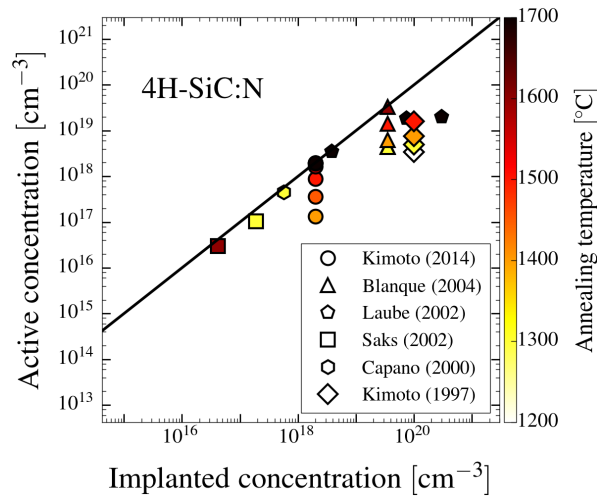


Figure 4.5.: Visualization of the experimentally examined N implantation into 4H-SiC [2], [74]–[77], [84]. The saturation of activation efficiency for high implanted concentrations can be observed.

Table 4.1.: Activation kinetics data for N-implanted 4H-SiC from Blanqué *et al.* [76]. The implanted concentration is $3.5 \times 10^{19} \text{ cm}^{-3}$.

Annealing Temperature [°C]	Annealing Time [h]	Activation Efficiency [%]
1300	0.30	0.013
1300	0.75	11
1300	1.5	13
1400	0.50	16
1400	1.0	18
1500	0.50	37
1500	1.0	40
1600	0.50	93

4.3.2. GaN

The implantation and annealing process poses a significantly more difficult challenge for GaN than for SiC (see Section 2.2.3 and Section 2.2.4). As a consequence the literature does not provide sufficient data for the acceptor dopant Mg. The challenges of the highly difficult annealing process are tackled with different procedures by different groups. Therefore, the provided experimental results cannot be used for a careful empirical modeling approach, as the limited available data cannot be directly compared.

The annealing process for Si-implanted GaN is challenging as well, however Fellows *et al.* [36] and Niiyama *et al.* [38] have independently presented comparable experimental results, which are visualized in Figure 4.6. As opposed to SiC a reduced activation efficiency for low and moderate doping concentrations has been observed (discussed in Section 2.2.4). The numerous experimental data sets allow to formulate an empirical model that can describe the activation kinetics and the steady-state behavior. In the next section the general objectives and requirements of such a model are stated. Employing this information, the mathematical model is presented and its implications are discussed.

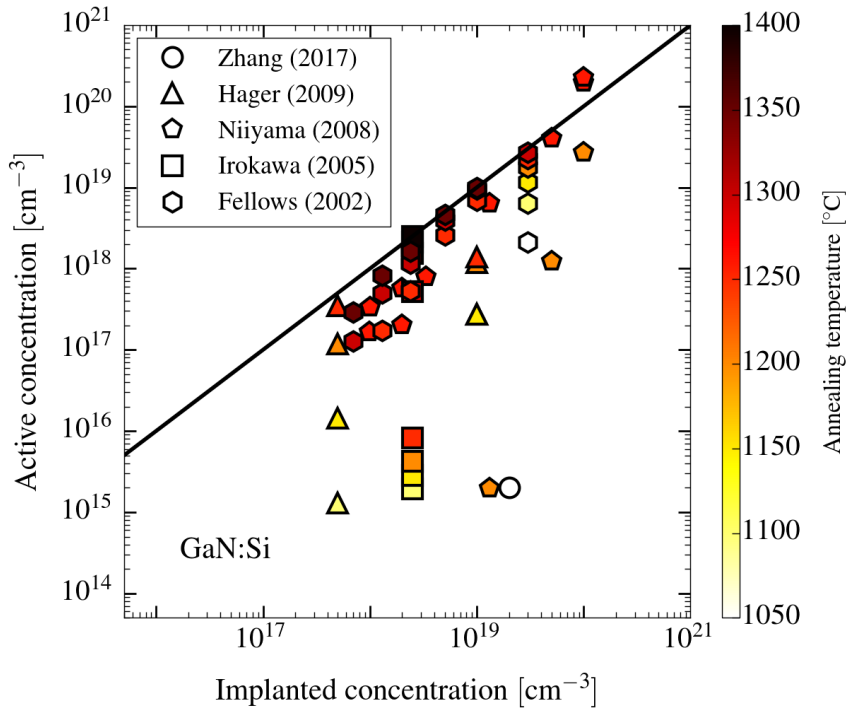


Figure 4.6.: Experimental electrical activation of Si-implanted GaN in the steady-state [36]–[38], [85], [86]. In contrast to implanted SiC, moderate implanted dopant concentrations ($< 1 \times 10^{18} \text{ cm}^{-3}$) are not fully activated.

4.4. Transient Electrical Activation Model

4.4.1. Model Objectives and Requirements

The experimental observations discussed in Section 4.3.1 indicate the following key characteristics of a well-suited electrical activation model for implanted GaN and SiC:

- Isothermal annealing is considered, i.e., the annealing process takes place at a well-defined annealing temperature T_A . In particular, the heating-up prior to reaching the stable temperature T_A is not considered.
- For extensive annealing times t_A the electrical activation efficiency reaches a saturation value $R_{\text{act}}(t_A \rightarrow \infty)$:
 - If the implanted dopant concentration C_x is kept constant, elevated annealing temperatures T_A allow for enhanced equilibrium activation $R_{\text{act}}(t_A \rightarrow \infty)$. The functional dependence of the electrical activation on temperature resembles a logistic growth (4.2).
 - A constant annealing temperature T_A , a high dose implantation, and the consequently high implanted concentrations C_x lead to a saturation of the activation efficiency. This has been clearly observed for Si and SiC. Even though saturation for high-dose implantation has not been observed for GaN, yet the limited solid solubility of every solid material suggests the same behavior for GaN.

- Dopants in SiC can be fully activated ($R_{\text{act}} = 1$) for low dose implantation (provided sufficiently long t_A and elevated T_A). For silicon implantation into GaN, incomplete activation for low implanted doses C_x were reported.
- The saturated active dopant concentration $C_{a,f}$ is related to the solid solubility of the implants in the host material.
- The annealing kinetics are accelerated by high annealing temperatures t_A . If the annealing temperature is too low, even a very long annealing time t_A does not lead to full activation.
- The initial activation efficiency $R_{\text{act}}(t_A = 0)$ serves as the initial condition for the model that aims to describe an isothermal process. It does not depend to the specific heating-up behavior of the annealing equipment.

In the following section an empirical model that is capable to describe all these features is presented. First, the model is formulated in a way that is directly applicable to SiC. Second (Section 4.5), a model modification that accounts for the peculiarities of Si-implanted GaN is presented.

4.4.2. Activation Model for SiC

The activation process is described as a chemical reaction. The reaction rate is assumed to be directly proportional to the inactive dopant concentration. However, the maximum active dopant concentration is limited. The upper bound corresponds to the (electrically) active dopant concentration in thermal equilibrium $C_{a,f}$ and is related to the implanted concentration C_x using the expression

$$C_{a,f}(T_A, C_x) = \frac{C_x}{1 + \frac{C_x}{C_{ss}(T_A)}}. \quad (4.3)$$

The saturation behavior is incorporated by introducing the parameter $C_{ss}(T_A)$, which is a function of the annealing temperature T_A . $C_{ss}(T_A)$ is linked to the solid solubility of a dopant material in the host crystal. High solid solubility refers to high values of $C_{ss}(T_A)$.

The annealing kinetics is modeled as a simple first order process with the upper limit $C_{a,f}$ (see Figure 4.7). The reaction rate R is given by

$$R = \frac{dC_a}{dt_A} = k_r(T_A) (C_{a,f}(T_A, C_x) - C_a), \quad (4.4)$$

where $k_r(T_A)$ is the temperature dependent reaction rate coefficient. $k_r(T_A)$ is assumed to follow an Arrhenius law, consistent with common practice in chemical kinetics [87]. Likewise, $C_{ss}(T_A)$ is expected to follow an Arrhenius equation,

$$k_r(T_A) = A^{k_r} \exp\left(-\frac{E_a^{k_r}}{k_B T_A}\right), \quad C_{ss}(T_A) = A^{C_{ss}} \exp\left(-\frac{E_a^{C_{ss}}}{k_B T_A}\right). \quad (4.5)$$

In both cases the activation energy E_a is a positive quantity. The analytical solution of (4.4) is

$$C_a(t_A, T_A, C_x) = A \exp[-k_r(T_A)t_A] + C_{a,f}(T_A, C_x), \quad (4.6)$$

with $A < 0$. Incorporating the initial condition $C_{a,0} = C_a(t_A = 0)$ yields

$$C_a(t_A, T_A, C_x) = [C_{a,0} - C_{a,f}(T_A, C_x)] \exp[-k_r(T_A)t_A] + C_{a,f}(T_A, C_x). \quad (4.7)$$

$C_{a,0}$ is not related to the physical situation immediately after implantation. Thus, the initial condition can not be derived from measurements. Keeping in mind that the proposed model is only valid for t_A somewhere in the order of a few seconds, the initial condition $C_a(t_i)$ can be shifted to a specific $t_A = t_i \neq 0$. The analytical solution is then

$$C_a(t_A, T_A, C_x) = [C_a(t_i) - C_{a,f}(T_A, C_x)] \exp[k_r(T_A)(t_i - t_A)] + C_{a,f}(T_A, C_x). \quad (4.8)$$

The important difference compared to (4.7) is the fact that $C_a(t_i)$ can be directly determined from annealing measurements. With $C_a(t_A, T_A, C_x)$ established, the electrical activation efficiency is given by

$$R_{\text{act}}(t_A, T_A, C_x) = \frac{C_a(t_A, T_A, C_x)}{C_x}. \quad (4.9)$$

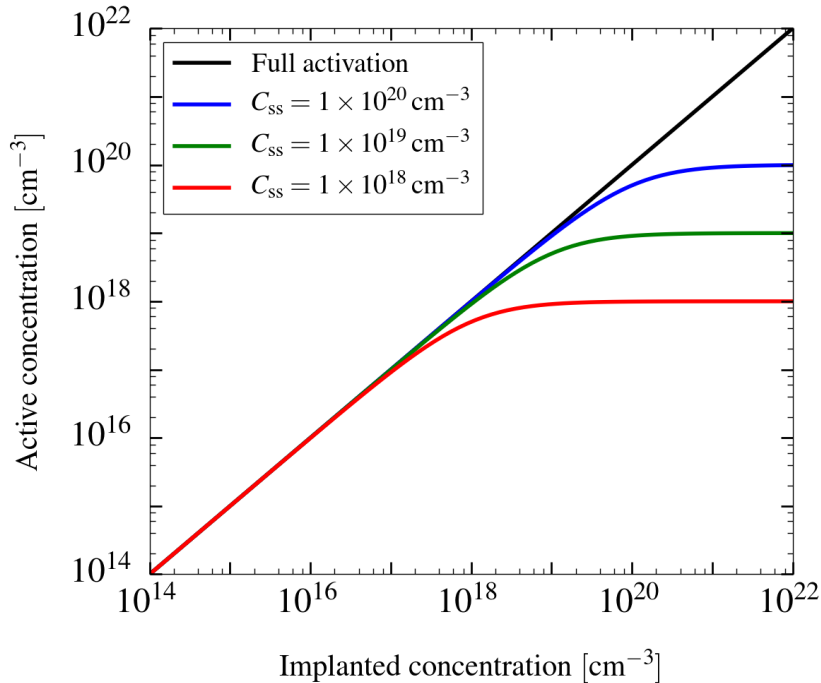


Figure 4.7.: Active dopant concentration in thermal equilibrium $C_{a,f}(T_A, C_x)$, as modeled by (4.3). For low implanted concentrations, i.e., $C_x \ll C_{ss}(T_A)$, the implanted dopants can be fully activated. Saturation occurs for high implantation concentration, i.e., $C_x \gg C_{ss}(T_A)$. The black line represents full activation.

(4.7) is capable to describe the isothermal annealing process according to the main objectives given in Section 4.4.1. Two phase diagrams, as given in Figure 4.8, visualize the model predictions. In accordance with the objectives a combination of elevated annealing temperatures and sufficiently long annealing times leads to full activation, i.e., $R_{\text{act}} > 0.95$. On the one hand, full activation cannot be achieved even after hours if the annealing temperature is too low (e.g. 1500 °C in Figure 4.7). On the other hand, the annealing process can be considerably shortened ($t_A < 1$ min) if the equipment allows to raise the annealing temperature above 1800 °C. The concentration dependence is appropriately modeled as well. Low dopant concentrations can be fully activated even at low annealing temperature. In contrast, implanted concentrations close to the solid solubility limit (see also Section 2.2.3) cannot be fully activated even when employing extreme annealing temperatures ($T_A > 2200$ °C).

For a specific annealing time $t_A = \text{const.}$, the temperature dependence implied by the model is illustrated in Figure 4.9. The model can qualitatively reproduce a logistic-function type growth that is evident from measurements (Figure 4.1b). From a mathematical point of view, this is a direct consequence of the assumption that $C_{\text{ss}}(T_A)$ follows an Arrhenius law. Therefore, the Arrhenius assumption is confirmed to be in accordance with the experimental observations.

The steady-state activation $R_{\text{act}}(t_A \rightarrow \infty)$ is determined by the active dopant concentration in thermal equilibrium $C_{\text{a,f}}(T_A, C_x)$, which depends on the ratio $C_x/C_{\text{ss}}(T_A)$. The definition of (4.3) implies that a doping level equal to $C_{\text{ss}}(T_A)$ is only 50% activated. Therefore, the experimental data indicates that $C_{\text{a,f}}$ is necessarily smaller than the chemical solid solubility¹.

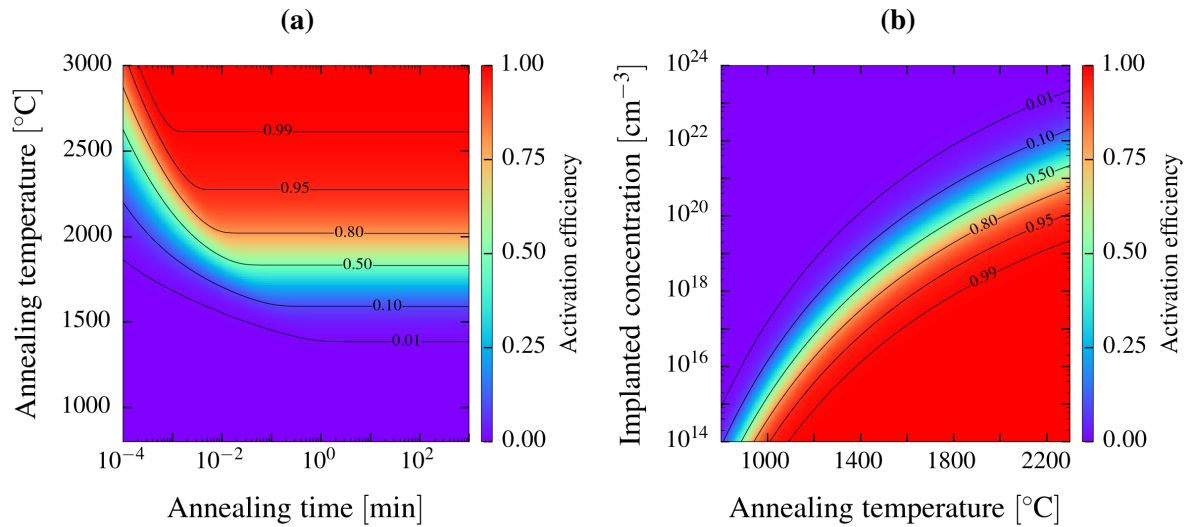


Figure 4.8.: Phase diagrams illustrating the impact of the annealing process parameters on the electrical activation of Al-implanted 4H-SiC ($C_x = 1 \times 10^{18}$ cm⁻³). **(a)** Electrical activation efficiency as a function of annealing time and **(b)** steady-state activation efficiency as a function of annealing temperature.

¹It is important to differentiate the physical/chemical quantity 'solid solubility', the annealing temperature dependent function $C_{\text{ss}}(T_A)$, and the active dopant concentration in thermal equilibrium $C_{\text{a,f}}(T_A, C_x)$. The definition (4.3) shows that $C_{\text{a,f}}(T_A, C_x)$ depends not only on the annealing temperature, but also on the implanted dopant concentration. The maximum electrically active dopant concentration is thus not only determined by the annealing temperature. This is due to the observation that in an environment of high chemical dopant concentration, dopant atoms can form bonds to other dopant atoms. In this way, clusters and defect-configurations involving bulk crystal vacancies and interstitials can be formed.

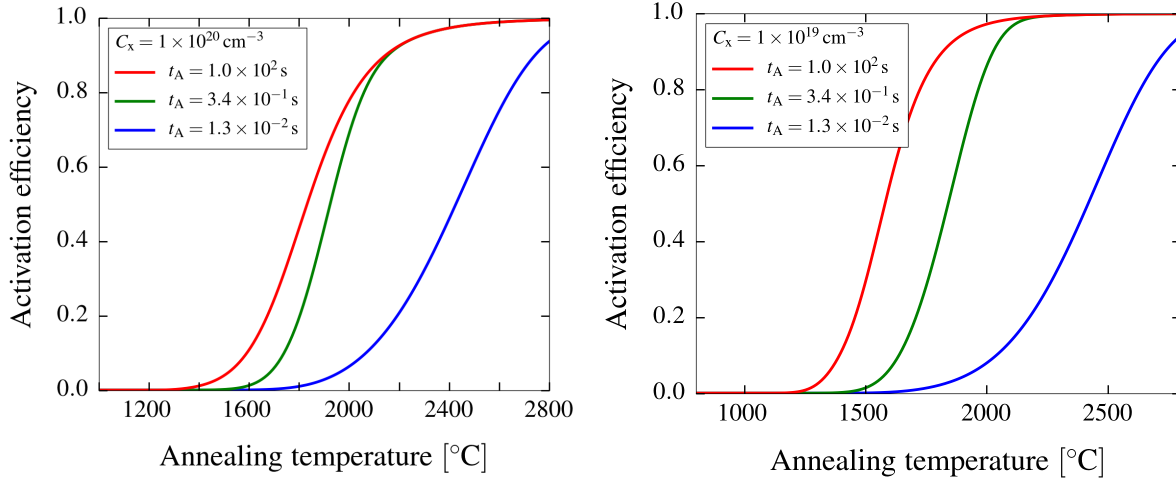


Figure 4.9.: Calculated active dopant concentration as a function of annealing temperature for specific annealing times and implanted dopant concentrations, **(a)** $C_x = 1 \times 10^{20} \text{ cm}^{-3}$ and **(b)** $C_x = 1 \times 10^{19} \text{ cm}^{-3}$. The empirical activation model (4.4) reproduces the abrupt raise of activation efficiency observed in experiments as shown in Figure 4.1b.

Even though it is possible to use the time-shifted solution (4.7) to determine the kinetic model parameter $k_r(T_A)$ from the measurement data, the choice of initial activated dopant concentration $C_{a,0}$ in (4.6) turns out to have only minor impact. As long as the initial dopant concentration is considerably smaller than the steady-state value ($C_{a,0} \ll C_{a,f}$) the reaction coefficient $k_r(T_A)$ is not significantly influenced. This assumption is justified for the wide-bandgap semiconductors SiC and GaN, because an active dopant concentration prior to the annealing step is not measurable. Thus, (4.6) can also be employed if $C_{a,0}$ is set to a relatively small value (compared to $C_{a,f}(T_A, C_x)$). A straightforward relation can be used:

$$C_{a,0} = F C_{a,f}(T_A, C_x) \quad (4.10)$$

where F is as an empirical parameter that is typically $\approx 10^{-3}$.

The model presented above accurately reproduces the activation characteristics observed in implanted SiC. In order to describe implanted GaN's divergent behavior, a model extension is proposed in the following section.

4.5. Activation Model Extension for GaN

For low doping concentrations $C_x \ll C_{ss}(T_A)$ the definition (4.3) assumes full activation $C_a = C_x$ in the steady-state case ($t_A \rightarrow \infty$). The divergent behavior for Si-implanted GaN, which is characterized by a reduced activation efficiency, cannot be described. However, the addition of the factor $(C_x/C_{ss}(T_A))^\alpha$ with the empirical parameter $\alpha > 0$ allows to reproduce this behavior

$$C'_{a,f}(T_A) = \frac{C_x \left(\frac{C_x}{C_{ss}(T_A)} \right)^\alpha}{1 + \frac{C_x \left(\frac{C_x}{C_{ss}(T_A)} \right)^\alpha}{C_{ss}(T_A)}}. \quad (4.11)$$

Figure 4.10 illustrates that the modified model reproduces the original transient activation model for $\alpha = 0$. Increasing the empirical factor α gradually tilts $C'_{a,f}$ away from full activation $C'_{a,f} = C_x$. The maximum active concentration is still governed by the solid solubility related parameter C_{ss} .

The reason for the low activation level prevalent for small implanted concentration is controversially discussed (see Section 2.2.4) in the literature. Assuming the very likely case that unintentionally introduced compensating dopants play an important role, α is related to the compensating species concentration. The higher the concentration, the higher is α . For this work, the experimental data (Figure 4.6) suggests that α obeys an Arrhenius law, which is further discussed in Section 4.7.2. However, governed by an Arrhenius law α attains very high values for annealing temperatures below the typically employed temperatures ($< 1200^\circ\text{C}$). As a consequence, (4.11) degenerates to a function similar to a step function, which is unphysical². Limiting the maximum value of α avoids this problem. A reasonable upper limit for α , which is consistent with the available data is 2. Thus, the valid range is $0 \leq \alpha < 2$.

For empirical models the calibration with respect to the experimental data is crucial. The next section examines the numerical techniques that are employed to estimate the model parameters.

4.6. Model Parameter Estimation - Nonlinear Regression

The proposed transient annealing model features three parameters for electrically active dopants: the reaction rate k_r , the solid solubility related parameter C_{ss} , and the initial active concentration $C_{a,0}$ (for the modified model there is also the empirical exponent α). If (4.10) is applied the number of independent parameters is reduced by one. The remaining two (three) parameters are estimated from the experimental data employing regression analysis.

The model parameter estimation procedure consists of two steps. In the first step the annealing data for constant annealing temperature $T_A = T_A^0$ is considered. For constant annealing temperature the active concentration depends only on the annealing time and the implanted dopant

²At low annealing temperatures and $C_x > C_{ss}(T_A)$ the modified model predicts the active concentration to be equal to the solid solubility coefficient $C_{ss}(T_A)$. This is a consequence of α assuming high values, i.e., $\lim_{\alpha \rightarrow \infty} C'_{a,f}(T_A) = C_{ss}(T_A)$. For $C_x < C_{ss}(T_A)$ extremely low activation efficiencies are achieved, $\lim_{\alpha \rightarrow \infty} C'_{a,f}(T_A) = 0$.

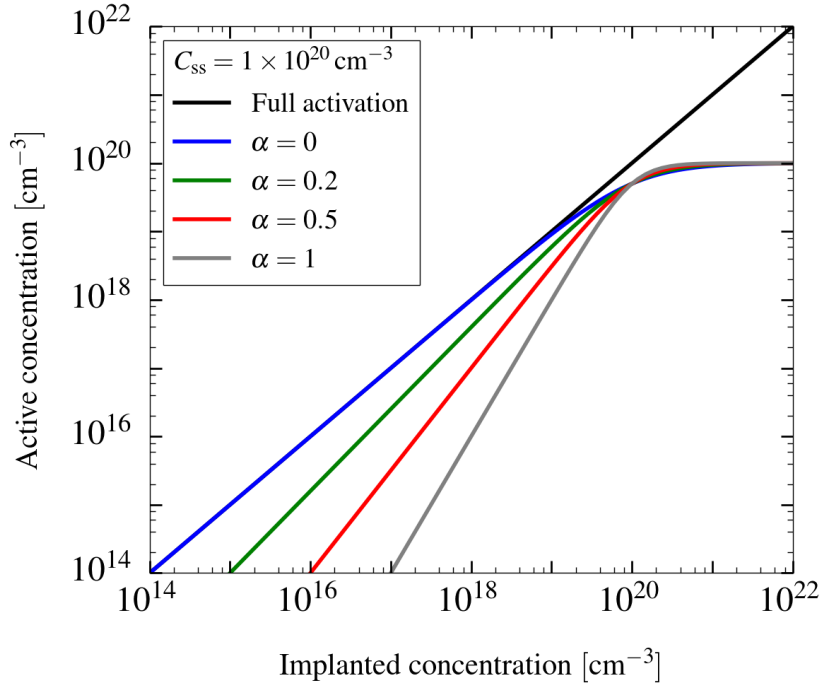


Figure 4.10.: The empirical modification of (4.3) given in (4.11) allows to describe the characteristic low activation level for small implanted dopant concentrations found in GaN.

concentration $C_a(t_A, C_x)|_{T_A=T_A^0}$. $k_r(T_A^0)$ and $C_{ss}(T_A^0)$ are estimated by solving a least squares problem in order to achieve the best fit of (4.7) to the experimental data. This procedure is repeated for all available annealing temperatures T_A^i . The results are further processed in the second step, where the prefactors $A^{k_r, C_{ss}}$ and activation energies $E_a^{k_r, C_{ss}}$ are determined by solving a second least squares problem for (4.5).

The least squares problem is a commonly occurring problem in science and engineering and is mathematically stated in Definition 4.6.1 [88].

Definition 4.6.1 (*Least Squares Problem*)

Find a local minimizer $\mathbf{a}^* \in \mathbb{R}^n$ for

$$F(\mathbf{a}) = \sum_{j=0}^{m-1} f_j^2(\mathbf{a}),$$

with given functions $f_j : \mathbb{R}^n \rightarrow \mathbb{R}$, $j \in \{0, \dots, m-1\}$ and $m \geq n$.

The function $F : \mathbb{R}^n \rightarrow \mathbb{R}$ is called *cost function* or *score function*. The curve fit problem for a given data set can be solved by appropriately defining the cost function, see Definition 4.6.2.

Definition 4.6.2 *Cost Function for the Regression Analysis*

Let $D = \{(x_0, y_0), (x_1, y_1), \dots, (x_{m-1}, y_{m-1})\} \subseteq \mathbb{R}^2$ be a set of m data points and $g(x; \mathbf{a})$ an analytical one dimensional function $g : \mathbb{R} \rightarrow \mathbb{R}$ with parameters $\mathbf{a} \in \mathbb{R}^n$. The cost function for the non-linear regression analysis is

$$F(\mathbf{a}) = \sum_{i=0}^{m-1} [y_i - g(x_i; \mathbf{a})]^2.$$

In the discussed parameter estimation procedure the function $g(x; \mathbf{a})$ assumes the form of (4.7) in the first step and of (4.5) in the second step, respectively. Both functions are nonlinear functions of the parameters $\mathbf{a} = [k_r, C_{ss}, (\alpha)]^\top$. Consequently, iterative numeric schemes have to be employed to solve the least squares problem. One example is the Levenburg-Marquardt gradient method [88].

The parameter estimation procedure has been performed for all the dopant-host material combinations given in Section 4.3, resulting in a calibrated electrical activation model, as demonstrated in the following sections.

4.7. Calibration of Activation Models

In order to confirm that the proposed model can accurately reproduce the experimental data, Arrhenius plots of the reaction rate coefficient $k_r(T_A)$ and the solid solubility parameter $C_{ss}(T_A)$ are examined. First, implanted 4H-SiC, for which the plethora of experimental data for different dopants is available, is considered. Second, the modified activation model is calibrated for Si-implanted GaN.

4.7.1. Implanted 4H-SiC

Figure 4.11a shows the calibrated model for Al implantation versus the experimental data from Nipoti *et al.* [62] for different annealing temperatures. Similar curve fits for all available annealing temperatures result in the $k_r(T_A)$ and $C_{ss}(T_A)$ plots depicted in Figure 4.11b. The annealing temperature dependence of these parameters can be accurately described by an Arrhenius law.

The lack of comprehensive activation kinetics studies for implanted B only allows to calibrate the activation model for the steady-state activation. Thus, only the solid solubility parameter $C_{ss}(T_A)$ is determined (as shown in Figure 4.12a). Compared to implanted Al the significantly limited data causes higher uncertainty about the obtained parameter values. Nevertheless, $C_{ss}(T_A)$ follows an Arrhenius law (Figure 4.12b).

The steady-state activation data for implanted N indicates that the solid solubility parameters obeys an Arrhenius law (Figure 4.13a and Figure 4.13b). The activation kinetics in particular have been investigated by Blanqué *et al.* [76] (see Figure 4.5). Their measurements allow to

approximately estimated the activation rate $k_r(T_A)$ as a function of the annealing temperature, depicting an Arrhenius dependency as well. This is illustrated in Figure 4.13b.

Similar to Al, there is a multitude of data available for P implantation, allowing to accurately determine $k_r(T_A)$ and $C_{ss}(T_A)$. The corresponding Arrhenius plots are depicted in Figure 4.14.

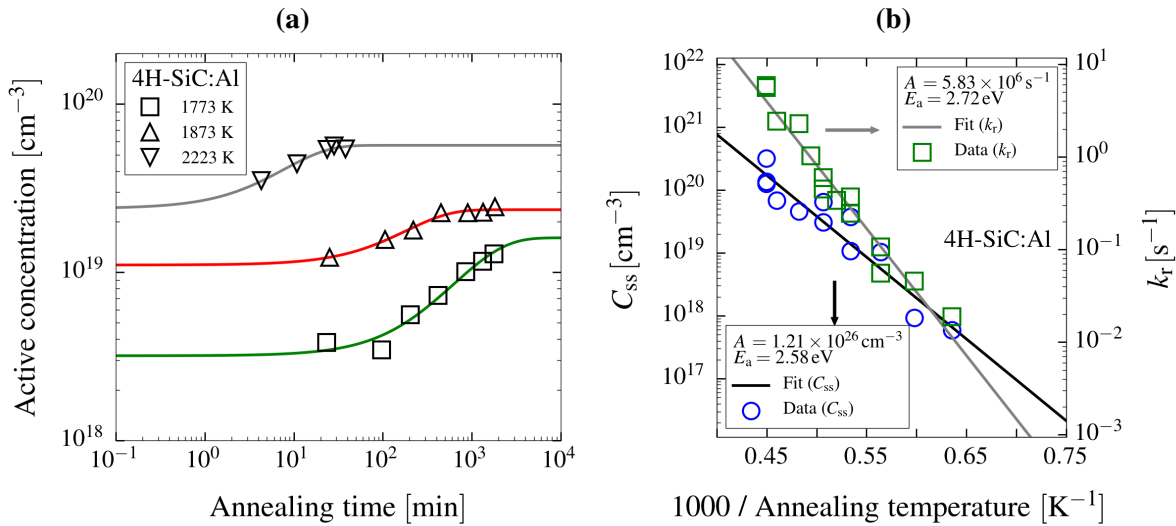


Figure 4.11.: **(a)** Transient electrical activation model fit to (4.6) for Al-implanted 4H-SiC. The data originates from Nipoti *et al* [62]. **(b)** The model parameters C_{ss} and k_r follow an Arrhenius law.

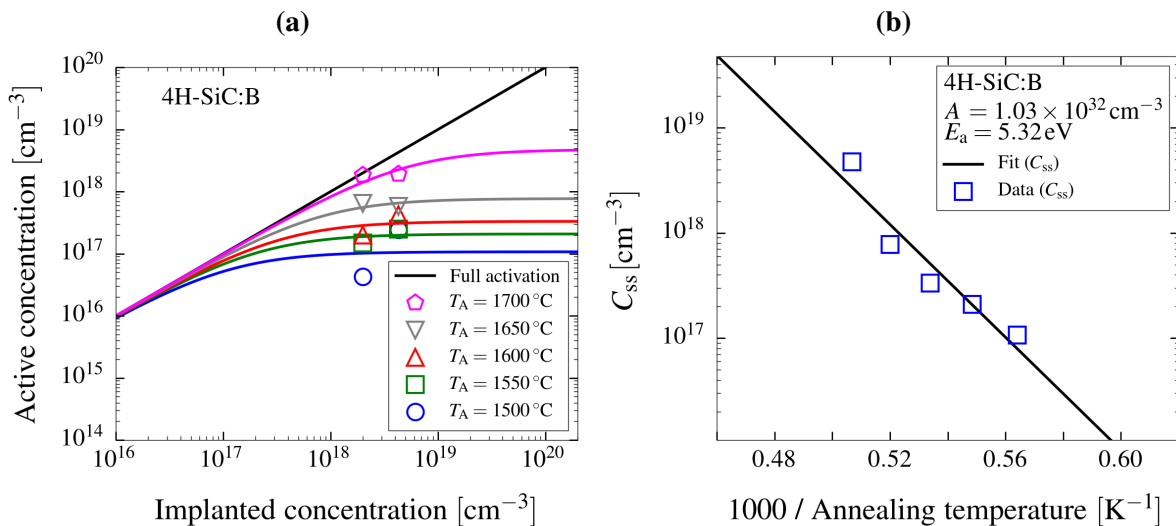


Figure 4.12.: **(a)** Fit of the steady-state activation model (4.3) to the B-implanted 4H-SiC data given in Figure 4.3. **(b)** Corresponding Arrhenius plots for the fits given in Figure 4.12a.

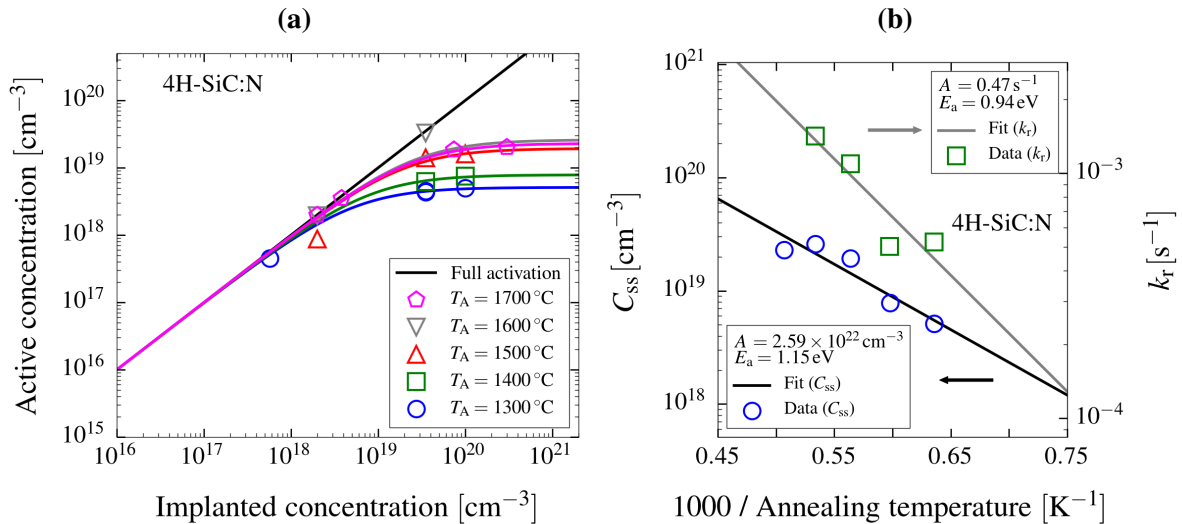


Figure 4.13.: (a) Fit of the steady-state activation model (4.3) to the N-implanted 4H-SiC data given in Figure 4.5. (b) Arrhenius plot of the model parameters C_{ss} and k_r , which are determined from the fits given in Figure 4.13a.

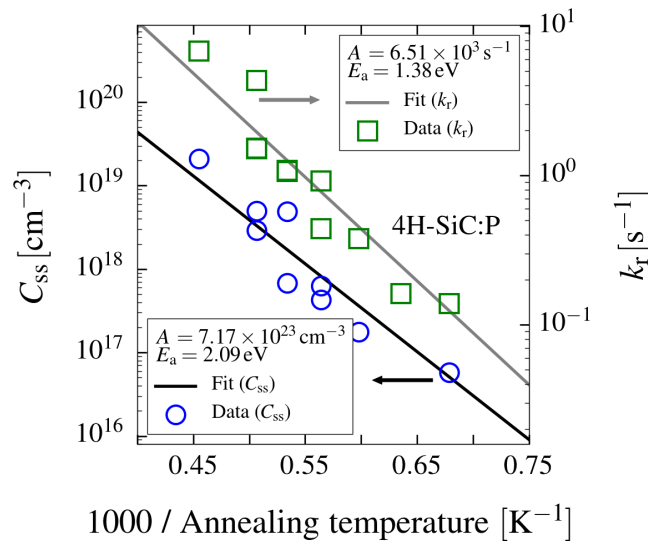


Figure 4.14.: Arrhenius plots of the model parameters C_{ss} and k_r for P-implanted 4H-SiC.

4.7.2. Implanted GaN

The modified activation model is employed for Si implanted GaN. Figure 4.15 demonstrates that the reduced activation efficiency for low concentrations is well reproduced. The corresponding solid solubility parameter $C_{ss}(T_A)$ follows an Arrhenius law in total analogy to its behavior for implanted SiC. The empirical exponent α is found to obey an Arrhenius law with negative activation energy. However, as pointed out in Section 4.5, α is only valid within the annealing temperature range that has been experimentally investigated. α can be assumed to have an upper limit, which is of importance for low temperatures. A further assumption is that the employed capping technology (e.g., AlN or SiO₂ caps) discussed in Section 2.2.4 does not

significantly influence the activation efficiency and, thus, the data from different experiments can collectively be considered in order to calibrate the activation model.

In conclusion, the proposed activation models have the capability to describe the impact of the annealing process parameters on the transient and equilibrium electrical activation of implanted dopants. The model parameters have been calibrated with respect to data from SiC and GaN annealing experiments. The activation models allow to accurately reproduce the experimental observations and can be employed within comprehensive semiconductor process simulations, which are discussed in the next chapter.

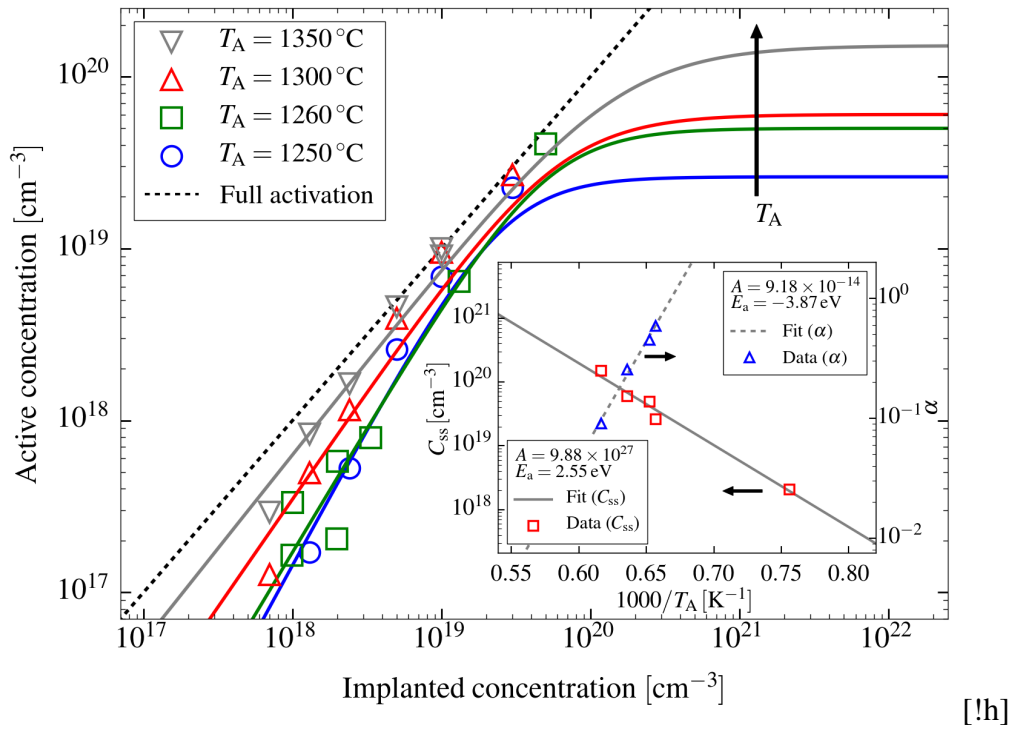


Figure 4.15.: Electrically active concentration $C_{a,f}$ for Si-implanted GaN as function of implanted concentration C_x for various annealing temperatures T_A . The solid lines show the fit of the modified activation model (4.11) (solid lines) to the experimental data [36]–[38], [85] (open symbols). The obtained model parameters C_{ss} and α are fitted with the Arrhenius equation, as shown in the inset figure.

5. Process and Device Simulations

The post-implantation annealing modeling discussed in the previous chapters plays a decisive role in semiconductor process simulations. Process simulations are an integral part of TCAD, which allows to harness the complexity of design and fabrication of semiconductor devices and systems. The challenging fabrication processes of SiC and GaN lead to significantly higher production costs compared to the Si technology. The predictive power of TCAD facilitates process integration and optimization and allows to examine the impact of process parameters on the device characteristics.

In this chapter the role of TCAD for wide-bandgap semiconductor device fabrication is discussed. The activation models presented in this work are integrated into comprehensive coupled process and device simulations of state-of-the-art power devices, the 4H-SiC DMOSFET and the GaN JBS rectifier. The simulation results provide valuable information about the influence of annealing parameters on device operation, which is essential for process optimization.

5.1. Technology Computer-Aided Design

In semiconductor fabrication, computer-aided modeling and simulations aim at supporting technology development and optimization and thus reducing development times and costs. Classical TCAD comprises front end process, device and interconnect modeling. However, in a broader context, the interplay between classical TCAD to equipment (e.g. lithography) and integrated circuit-scale (e.g., circuit elements and packaging) modeling is crucial for microsystem design. Therefore, the term extended TCAD has been established [89].

TCAD is highly valuable, because TCAD tools provide better insights in process and device characteristics. Additionally, TCAD allows to examine the optimum doping well width, peak doping concentrations, epitaxial layer, or oxide thicknesses in cost-effective way. After the calibration of the employed model to a set of experimental data, the model has predictive power, which allows to improve existing technology and investigate novel device structures [90]. The empirical activation model that is proposed in Chapter 4 part of process modeling on the feature scale. Hence, the annealing equipment is not modeled, but its impact on the sample is (by means of annealing temperature and time). Process simulations are especially useful when they are combined with device simulations, because the impact of process parameters on the device characteristics can be studied.

The impact of fabrication processes and their parameters on the device characteristics is in particular important for GaN and SiC, where the process steps have not yet been fully optimized. In the following sections the techniques that are employed to model the fabrication processes and operations of wide-bandgap power devices are discussed.

5.1.1. Process Simulations

Semiconductor process simulations deal with predicting the geometrical and physical impact of all process steps that are needed to fabricate semiconductor devices. During a process simulation both geometrical and physical problems have to be formulated and solved. The patterning of semiconductor structures is based on additive (e.g., thin film growth) and subtractive (e.g., etching) process, which are ultimately controlled by a sequence of lithography masks. For lithography the desired device geometry has to be specified by means of two-dimensional masks. Complex device structures (such as solid-state memories) require dozens of patterning steps and geometry-based simulations provide the tools to optimize them.

However, in order to account for the highly important non-ideal effects such as bird's peak, under-etching, or introduction of film stress, physical models are valuable for process simulations. The thickness of thermally oxidized or epitaxially grown films can be described as a function of time and further process parameters. The mechanical stress, which is introduced by lattice mismatch, impurity atoms, or electric fields is subject to continuum mechanisms. The multitude of processes occurring during ion irradiation (involving redeposition, surface diffusion and impurity cluster formation), require a combined geometrical and physical approach [91].

Continuous physical models typically assume the form of (3.15), where the dopant and defect diffusion is described with continuous distributions of physical quantities. However, the continuum approach has its limitations, which can be overcome by atomistic methods in some cases. One important example are probabilistic Monte Carlo ion implantation simulations (i.e., binary collision simulations), where the trajectory of individual ions as they enter the semiconductor is calculated. In order to accurately account for the lattice damage induced by the collision of ions with host atoms, the interatomic potentials and nuclear and electronic stopping mechanisms have to be modeled [92].

Physical models are often time-consuming (e.g., Monte Carlo ion implantation) or require information about micro-physical processes, which is often not available. As discussed in Chapter 3, the understanding of the micro-physics associated with annealing after an implantation step is not yet sufficient for most impurity-host material combinations. In such a case, empirical models come into play (as discussed in Chapter 4).

The examples given above corroborate that semiconductor process simulations solve multi-physics and geometrical problems. Several process simulation tools are available, however, in this work, Silvaco's Victory Process [91] simulator, which is capable of two- and three-dimensional simulations, is used. Process simulations are initiated by providing a list of statements that describe the processing steps and geometrical information via implantation masks. Victory Process implements various highly specialized numerical techniques, such as multi-material surface evolution and adaptive grid resolutions. These techniques are crucial for the demanding environment of multi-physics process simulation on a mutable geometry. The resulting device structure can be directly used to conduct device simulations, which are discussed in the next section.

5.1.2. Device Simulations

A semiconductor device simulation aims to describe the electronic transport enforced by externally applied voltages and currents. With accurate device simulations the most important device parameters, i.e., the figure of merits, can be optimized. Modern semiconductor devices rely on sophisticated doping profiles and complex current paths that cannot be easily modeled with simple one-dimensional compact-models.

A set of semi-classical differential equations, referred to as Drift-Diffusion equations has proven successful to calculate (charge) carrier and current density distributions in large-area Si devices. Even though these equations are insufficient for nano-scale devices [93], typical power device structures with dimensions in the μm regime can be accurately treated with them. The current densities in the semiconductor are determined via the continuity equations

$$\nabla \cdot \mathbf{J}_n - q \frac{\partial n}{\partial t} = qR, \quad (5.1)$$

$$\nabla \cdot \mathbf{J}_p + q \frac{\partial p}{\partial t} = -qR, \quad (5.2)$$

which result from conservation of electrical charge. A spatial gradient in the electron current density \mathbf{J}_n (hole current density \mathbf{J}_p) induces temporal change of the electron concentration n (hole concentration p). Additionally, charge carriers can be generated (e.g., optically or by charge injection), which is modeled with the generation/recombination rate R . q is the elementary charge. A distribution of carrier interacts with each other by Coulombic forces. Therefore, the Poisson equation

$$\nabla^2 \phi = \frac{q}{\underline{\epsilon}} (n - p + N_A^- - N_D^+) \quad (5.3)$$

is employed with the electric potential ϕ , the semiconductor's permittivity tensor $\underline{\epsilon}$, and the concentration of electrically active and ionized acceptors N_A^- and donors N_D^+ . The Drift-Diffusion equations [94]

$$\mathbf{J}_n = -q\mu_n(\nabla\phi - V_T\nabla n), \quad (5.4)$$

$$\mathbf{J}_p = -q\mu_p(\nabla\phi + V_T\nabla n) \quad (5.5)$$

state that the current densities are evoked by gradients in ϕ (drift component) and in the carrier density (diffusion component). V_T is the thermal voltage $V_T = (k_B T)/q$. The carrier's response to an applied electric field is described by the mobility $\mu_{n,p}$. In the case of the hexagonal semiconductor 4H-SiC, the mobility is anisotropic. The mobilities for current along the hexagonal c-axis (\parallel) and perpendicular directions (\perp) are different with the typical values [95]

$$\mu_{n,\perp} = \mu_n, \quad \mu_{p,\perp} = \mu_p, \quad (5.6)$$

$$\mu_{n,\parallel} = 1.2\mu_n, \quad \mu_{p,\parallel} = \mu_p. \quad (5.7)$$

In order to account for the special material properties of wide-bandgap semiconductors, the incomplete ionization and the mobility have to be accurately modeled. The former is linked to a phenomenon, which is referred to as freeze-out. Even if a dopant is electrically active (after an annealing step), electrons can be strongly bound to it, prohibiting the electrons to contribute to the conduction current (and consequently ionizing the dopant). Due to large ionization energies, partial freeze-out is observed in SiC even at room temperature. The relation between ionized

dopant concentrations $N_{D,A}^{+,-}$ and electrically active dopant concentrations $N_{D,A}$ can be modeled using the expression [94], [96]

$$N_{D,A}^{+,-} = \frac{N_{D,A}}{1 + g_{D,A} \frac{v}{N_{C,V}} \exp\left(\frac{E_B}{k_B T}\right)}, \quad v = \{n, p\}, \quad (5.8)$$

which can be derived from statistical mechanics [97]. Dopant ionization is a thermally promoted process with an activation energy $E_B = E_C - E_D$ in the donor case and $E_B = E_A - E_V$ in the acceptor case. E_C and E_V refer to the conductance band edge and valence band edge energy, respectively, and E_D and E_A characterize the dopant's energy level¹. Additionally, the degree of ionization depends on the degeneracy factors $g_{D,A}$ ². $N_{C,V}$ are the effective densities of states for the conduction and valence band, respectively. However, in 4H-SiC the dopants can reside on hexagonal and cubic lattice sites, which is accounted for by the two-level incomplete ionization model, which introduces one expression in the spirit of (5.8) for each type of lattice sites [98].

Mobility modeling is highly important for every semiconductor device, but in particular for MOSFETs. In a MOSFET, the carriers transversing the channel are subjected to high electrical fields and surface scattering, which reduces the mobility values compared to the bulk mobility. A comprehensive mobility model, which has been specifically proposed for 4H-SiC, is the Uhnevionak model [17]. In the Uhnevionak model, the mobility is constructed as the sum of individual influences according to Matthiessen's rule

$$\frac{1}{\mu_{n,p}} = \frac{1}{\mu_{\text{IMP}}} + \frac{1}{\mu_{\text{BP}}} + \frac{1}{\mu_{\text{C}}} + \frac{1}{\mu_{\text{SR}}} + \frac{1}{\mu_{\text{SP}}}. \quad (5.9)$$

The contributions from Coulomb scattering at ionized impurities (IMP), bulk-phonon scattering (BP), scattering at interface charges (C), surface roughness (SR), and surface phonon scattering (SP) allow to accurately model the electron mobility in the DMOSFET channel. For other device structures, such as the JBS rectifier, surface and interface effects can be neglected.

The generation rate R is another quantity that is strongly material dependent. It is important to correctly account for generation-recombination phenomena, because they critically affect leakage currents and device breakdowns [23]. Indirect generation-recombination, which involves electron and hole capture and emission processes via trap centers, is commonly modeled with the Shockley-Read-Hall (SRH) model. Auger-processes, which involve three particles that interact due to their high thermal energy, can also be described with additional generation terms.

Silvaco's Victory Device [96] is a commercially available general purpose device simulator, which, among others, solves the semiconductor equations discussed above. The simulation domain is subdivided into discrete elements (e.g. tetrahedrons in three dimensions), which allow to discretize the coupled differential equations. The resulting nonlinear system of algebraic equations is solved with the help of Newton's method. Victory Device allows to simulate the device structures originating from Victory Process, which thereby offering to model the entire workflow, from fabrication to the evaluation of the electrical characteristics. As far as mobility modeling is concerned, various models are available for both wide-bandgap semiconductors

¹(5.8) is commonly given in the form $N_D^+ = N_D / (1 + g_D \exp[(E_F - E_D)/(k_B T)])$ with the Fermi level E_F and the donor level E_D . Within the framework of Maxwell-Boltzmann statistics both formulations are equivalent, because $n = N_C \exp[(E_F - E_C)/(k_B T)]$. For ionization of acceptors similar equations hold.

²The degeneracy factors characterize the number of ways an electron can assume a localized state [97].

examined in this work. The model parameter can be flexibly chosen, allowing to accurately simulate power DMOSFETs and JBS rectifiers, as discussed in the next sections.

5.2. SiC Power DMOSFET

A DMOSFET is a vertical current device, which was first realized in Si technology. SiC-based DMOSFETs have been presented in the early 2000s and have been optimized since then [99]–[101]. In the following, the commonly employed DMOSFET structure with dimensions and doping profiles reported by Saha *et al.* [102] is considered. The fabrication process is simulated and the output characteristics of the resulting DMOSFET are calculated, allowing to study the impact of thermal annealing on the device properties.

5.2.1. SiC DMOSFET Structure

Figure 5.1 shows the schematic cross section of a 4H-SiC (n-type) DMOSFET. A n-type 4H-SiC epilayer is grown on a highly n-doped (n^+) substrate. In order to form the channel, a p-type well (referred to as bulk) is required. In Si technology, the p-type well is realized using doping by diffusion. However, the low diffusion coefficients of dopants in SiC require to employ the ion implantation technique. The p-type well is referred to as the DMOSFET's 'bulk'. Similar to a lateral MOSFET structure highly n-doped source regions are formed. The drain region is located at the wafer backside, enforcing a vertical current flow. The gate contact allows to control the surface carrier concentration in the channel via the gate oxide, which is also depicted in Figure 5.1. Strikingly, the electron current is guided along the wafer surface before it transitions into the vertical direction. This ensures excellent electrostatic control and enhances the drain current by reducing the channel length.

The highly doped p-type and the n-type region are shortened to turn off the parasitic bipolar junction transistor, which is formed by the p^+ -region, the n^+ -well, and p-type well. The p-well and the drain region form a pn-diode (referred to as bulk-drain diode), which is required to block the transverse current for positive drain-source voltages V_{DS} . Its breakdown voltage can be precisely controlled by the doping concentration. For negative V_{DS} the bulk-drain diode does not block the current and the DMOSFET operates as pn-rectifier, which can be beneficially utilized in power electronics [103].

The DMOSFETs device structure allows to realize power switches capable of controlling drain voltages in the kV regime with negligible leakage currents. The parallel circuit structure enables a favorable high input capacitance enabling fast switching speed (≈ 100 ns) and drain currents in the kA regime with on-state resistances R_{on} that are at least two orders of magnitude lower than for Si devices [99].

The main design goal is to minimize R_{on} and the chip area while maintaining a high blocking voltage. In order to achieve that, a heavily n-doped region, which is referred to as junction field effect transistor (JFET) region, has been proposed [2]. In particular, the JFET region allows to reduce the distance between two adjacent source regions and thus the chip area. However, this is at the cost of an enhanced on-resistance. A self-aligned sub-micron channel further reduces the channel length and current crowding is avoided by homogenizing the trapezoidal electron

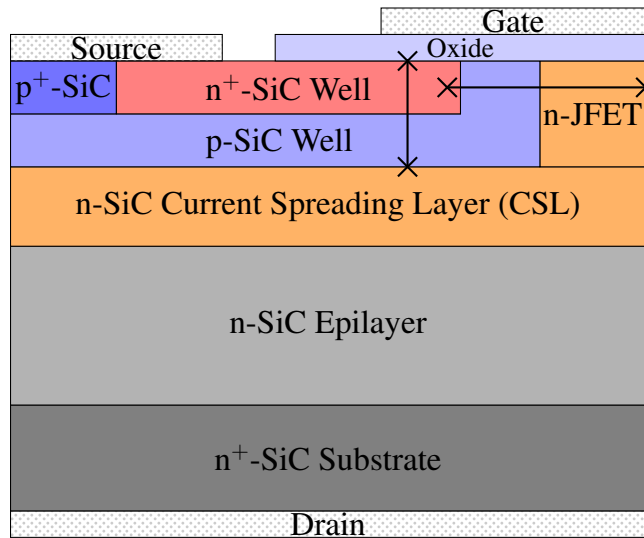


Figure 5.1.: Schematic cross-section of the examined 4H-SiC DMOSFET. The vertical line corresponds to the cut that is used for the doping depth profiles in Figure 5.3. Quantities along the horizontal line are discussed in Figure 5.6a.

flow from the JFET region into drift region with the help of an epitaxial n-type current spreading layer (CSL), which is also shown in Figure 5.1 [102].

5.2.2. SiC DMOSFET Process Simulations

Starting with a highly doped n-type 4H-SiC substrate the following process steps are simulated with Victory Process:

- Epitaxial growth of a lightly n-doped $6\ \mu\text{m}$ epitaxial layer ($N_D = 1 \times 10^{16}\ \text{cm}^{-3}$).
- Epitaxial growth of a $0.9\ \mu\text{m}$ n-doped layer ($N_D = 1 \times 10^{17}\ \text{cm}^{-3}$). This layer forms the CSL layer and the JFET region in the final device.
- Selective deposition of the implantation mask (SiO_2).
- Ion implantation of aluminum (p-type dopant) and P (n-type dopant) to form the p-well, highly doped n-well, and the highly p-doped region below the source contact. The implantation energies are chosen to produce a p-well with a depth of $0.6\ \mu\text{m}$.
- Annealing step employing the empirical activation model (discussed in Chapter 4). The surface is capped with SiO_2 .
- Thermal oxidation to form the gate oxide with a thickness of $50\ \text{nm}$.
- Metal deposition to form the contacts (source, gate, and drain).

These process steps result in the DMOSFET structure shown in Figure 5.2, where the active region near the surface is depicted in detail (Figure 5.2). Only one half-cell of the complete device is shown. This is sufficient for device simulations, because the total cell can be constructed by mirroring the half-cell along the vertical axis. The geometrical dimensions are chosen to reproduce the device presented by Saha *et al* [102].

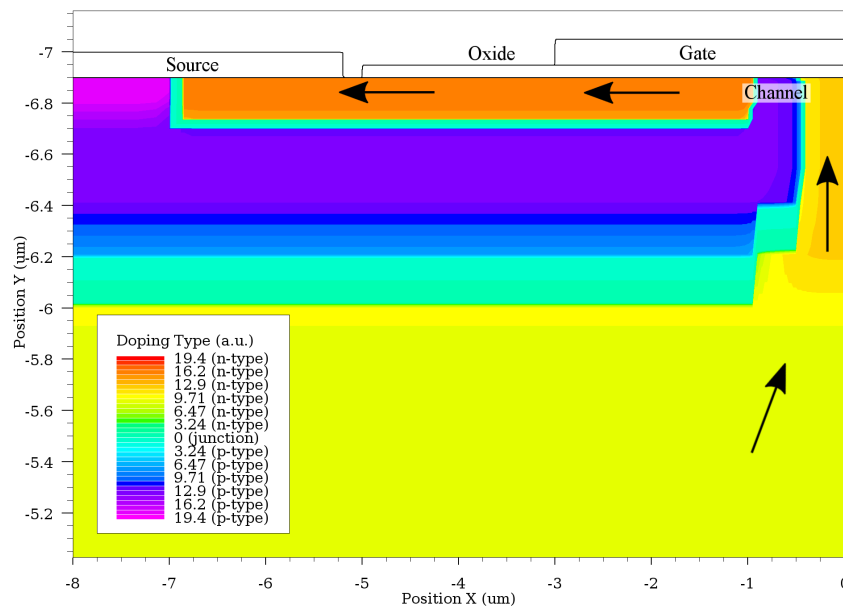


Figure 5.2.: Victory Process cross section of the investigated 4H-SiC DMOSFET. The colors illustrate the (electrically active) net doping concentration $N_{\text{Net}} = N_{\text{D}} - N_{\text{A}}$. The arrows show that the conduction current flows vertically from the drain to the channel and transitions to lateral flows along the surface to leading to the source contact.

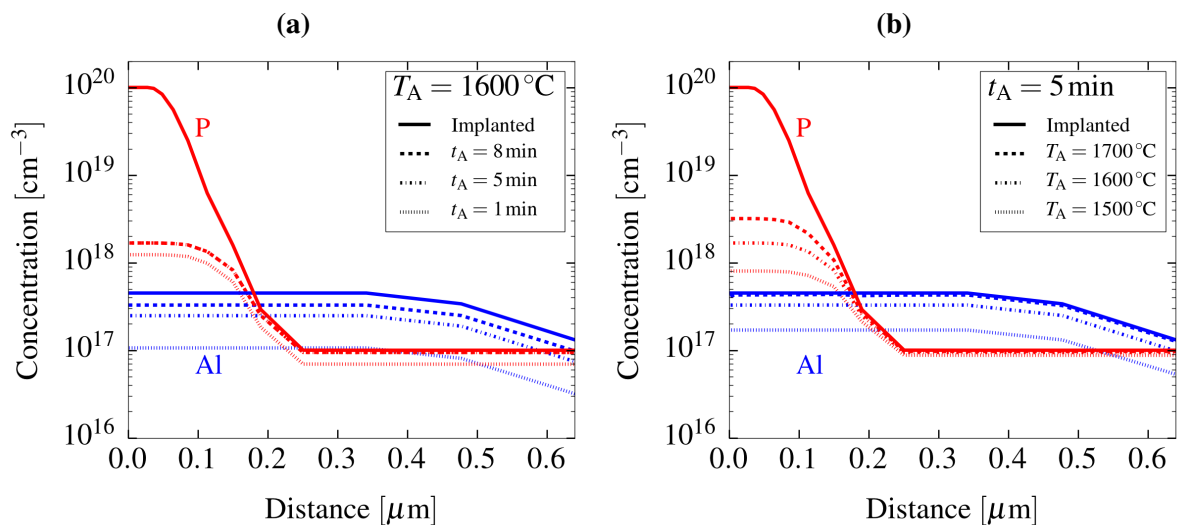


Figure 5.3.: DMOSFET doping depth profiles along the line given in Figure 5.2. **(a)** The maximum active P concentration is limited by the annealing temperature $T_{\text{A}} = 1600^{\circ}\text{C}$. Even extending the annealing time from $t_{\text{A}} = 5$ min to 8 min does not increase the activation efficiency. For implanted Al this is not the case, because the total implanted concentration is two orders of magnitude lower. **(b)** For constant annealing time the strong impact of annealing temperature on the maximum activation efficiency is observed for the highly P-doped regions. The low Al-implanted concentration can be nearly fully activated even at reduced temperatures.

The n^+ source region is modeled to exhibit a peak donor concentration of $1 \times 10^{20} \text{ cm}^{-3}$ in accordance with Saha *et al.* The Al implantation doses forming the p-well are chosen to produce a fully functional DMOSFET device under the assumption of fully activated implanted dopants. However, the electrical activation ratio depends on annealing time t_A , annealing temperature T_A , and implanted concentration C_x as stated by the empirical activation model (see Section 4.4). Figure 5.3 illustrates the depth doping profiles (vertical cut through n^+ -well and p-well) and demonstrates the predictions of the empirical activation model for several annealing temperatures and annealing times. Saha *et al.* employed $T_A = 1600^\circ\text{C}$ and $t_A = 5 \text{ min}$, also shown in Figure 5.3.

For a constant annealing temperature a transient saturation can be observed. While the active aluminum concentration is increased threefold by extending the annealing time from 1 min to 5 min, a 8 min annealing steps only results in an further improvement of 30%. The high concentration of implanted P causes a drastically reduced activation efficiency compared to the implanted aluminum profile. Furthermore, the activation kinetics of implanted P is faster with the maximum activation already reached after 5 min. The maximum activation efficiency of only approximately 2% is noticeably small, indicating that higher annealing temperatures are needed to activate P doping profiles with concentrations in the order of 10^{20} cm^{-3} . In contrast, the annealing temperature $T_A = 1600^\circ\text{C}$ allows to achieve an aluminum activation of $\approx 85\%$ after 8 min.

Figure 5.3b illustrates the impact of T_A for a constant $t_A = 5 \text{ min}$ on the doping profile. In particular, elevated annealing temperatures ($T_A = 1700^\circ\text{C}$) allow to increase the aluminum activation ratio from 73% to 93%. The achievable P activation ratio is limited by solid solubility and thus only amounts to approximately 3% of the implanted peak concentration.

5.2.3. SiC DMOSFET Device Simulations

Silvaco's Victory Device simulator [96] allows to simulate the device characteristics for device structures obtained by Silvaco's Victory Process simulator. The considered 4H-SiC DMOSFET is a large-area device, which enables a semi-classical modeling approach.

The models discussed in Section 5.1.2 enable an accurate description of the carrier transport in the DMOSFET. Additionally, interface states have to be considered. The high density of interface states at the SiC-SiO₂ interface strongly impacts the MOSFET's sub-threshold slope, because charge carriers are trapped at the interface, which affects the electrostatics in the channel. Sze [104] analytically determined that the presence of interface states raises the sub-threshold slope $S = V_G / (\log I_D)$, which is detrimental for device performance (I_D and V_G refer to the drain current and the gate voltage, respectively). The charge trapping process depends on the trap's energy level and the possible charge states. In 4H-SiC acceptor-like traps, which can assume a neutral or a negatively charged state, are dominating. A simple approach to model the impact of interface traps on the device characteristics is to adapt the SRH generation-recombination formalism, which has been originally established for bulk Si, for the 4H-SiC-SiO₂ interface [105]. Appendix A provides a comprehensive table that summarizes the employed models and parameters as they were set in Silvaco Victory Device simulator. The well calibrated device simulator allows to study the output characteristics (I_D vs. V_G) of the considered DMOSFET, which is presented in the following.

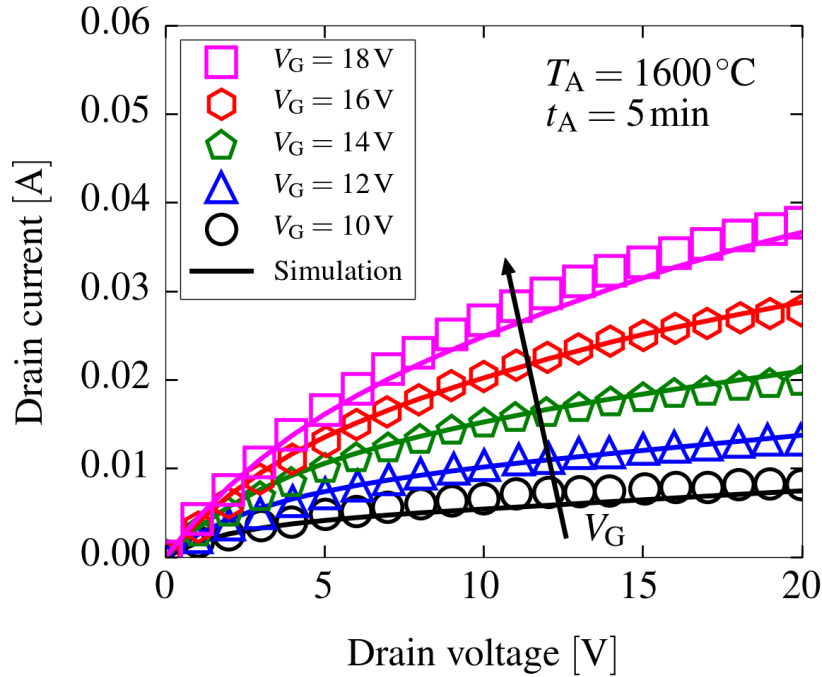


Figure 5.4.: Simulated and experimentally observed DMOSFET output characteristics for the annealing process parameters and device geometry as presented by Saha *et al* [102]. The simulations accurately reproduce the gate voltage control.

Figure 5.4 shows the DMOSFET's output characteristics. The simulations accurately reproduce the data presented by Saha *et al.* [102] in the range from 10 V to 18 V. The experiment data has been obtained by annealing the implanted regions at 1600 °C for 5 min. The combined process and device simulations allow to examine the influence of the annealing time and temperature on the output characteristics. Figure 5.5 shows the output characteristics for several annealing conditions. If the annealing time is not sufficiently long ($t_A = 1$ min), a purely resistive behavior that cannot be controlled by the gate voltage is observed (as shown in Figure 5.5a). Extending the annealing time to 8 min results in enhanced values of the small signal output resistance R_{out} in the saturation region. Figure 5.5b demonstrates that a similar behavior for different annealing temperatures can be observed.

The resistive output characteristics that occurs for insufficient annealing times and temperatures is caused by low active acceptor concentrations in the channel region. In order to form a functional DMOSFET, a clearly defined p-type channel region is necessary. This is the case if the active Al concentration exceeds the CSL epilayer's donor concentration. In particular, the n^+ -well, the channel, and the JFET region are required to form a lateral n^+pn sequence. The DMOSFET's operation principle relies on the depletion of holes directly at the SiC-SiO₂ interface, which results in a narrow area with high electron concentrations and defines the conductive channel. The depletion is controlled by the gate voltage, which provides electrostatic control of the surface potential. Figure 5.6a illustrates the electron concentration and potential for a lateral cut that is 0.1 μm separated from the SiC-SiO₂ interface (as shown in Figure 5.2). For this distance from the interface a negligible electron concentration is expected within the channel region. However, for bias conditions $V_G = 18$ V and $V_D = 16$ V the simulations yield electron concentrations around $1 \times 10^{16} \text{ cm}^{-3}$ for the 1 min annealing step. This can be attributed to the missing potential barrier between the n^+ -well (source) and the channel region. Due to the small

active Al concentration for this annealing steps, the channel region is flooded with electrons from the n^+ -region. Consequently, electrons assume the role of the majority carrier, which effectively results in a continuous n-doped path from source to drain, giving rise to resistive output characteristics.

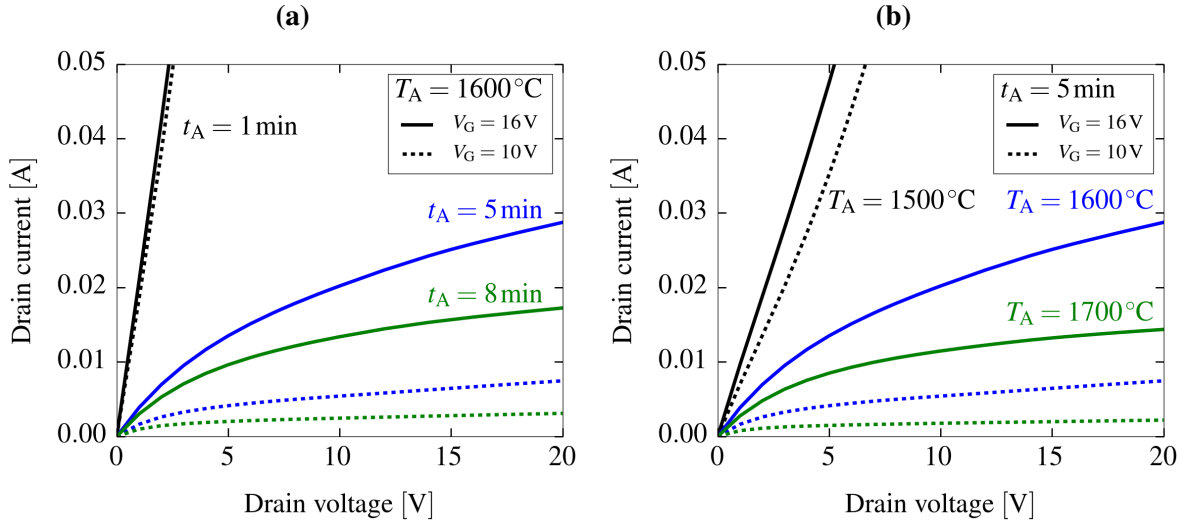


Figure 5.5.: DMOSEFET output characteristics for different annealing process parameters with constant (a) $T_A = 1600^\circ\text{C}$ and (b) $t_A = 5$ min. If the annealing time or temperature is insufficient, the purely resistive behavior that cannot be controlled by the gate voltage is observed (black lines). Extended annealing times and elevated annealing temperatures results in enhanced output resistances R_{out} .

The enhanced output resistances for elevated annealing temperatures is caused by a shift of the threshold voltage. Figure 5.6b illustrates the transfer characteristics (drain current I_D vs. gate voltage V_G) for $V_D = 16$ V. The characteristics is shifted to higher gate voltage for enhanced annealing temperatures, which corresponds to a threshold voltage shift. This is caused by the enhanced active acceptor concentration in the channel region, which determines the depletion circumstances. Extended annealing times also lead to a threshold voltage shift.

The combined process and device simulation demonstrate that the annealing process parameters have a strong impact on the device characteristics. In a device that is based on multiple implanted donors, such as the DMOSEFET, an accurate description of the electrical activation efficiency is highly beneficial for the device design. Annealing modeling is also crucial for a diode structure, as it is demonstrated in the next section for a GaN JBS rectifier.

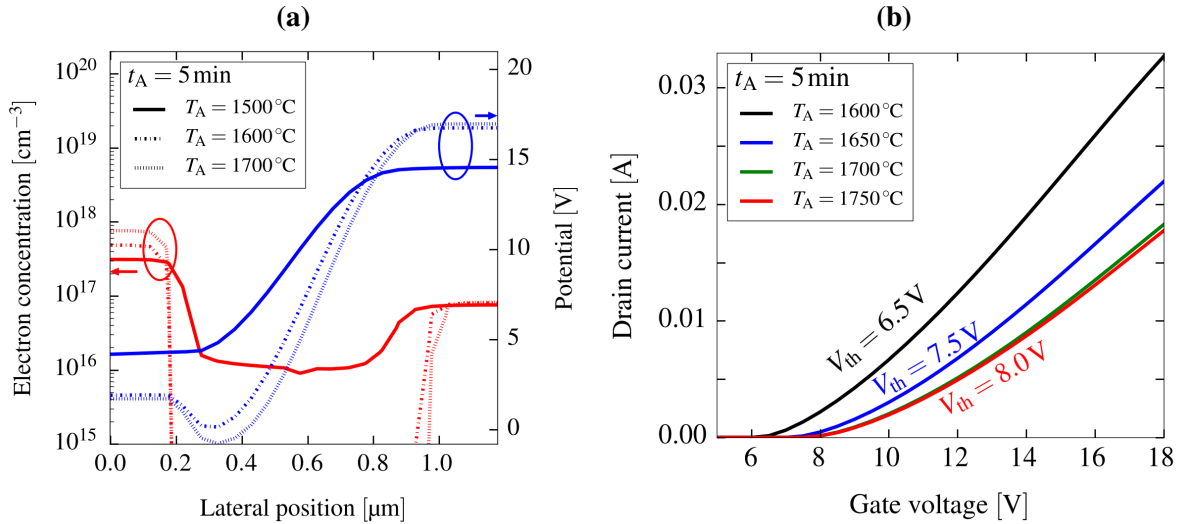


Figure 5.6.: (a) Electron concentration and potential distribution along the lateral cut shown in Figure 5.2. The bias conditions are $V_G = 18\text{V}$ and $V_D = 16\text{V}$. If the annealing time is not sufficiently long the consequent low active acceptor concentration in the channel region is too small to form a n^+pn sequence. Hence, a potential barrier between the n^+ well and the channel is missing and the channel regions is flooded with electrons. (b) Transfer characteristics for different annealing temperatures. Elevated annealing temperatures result in higher electrically active acceptor concentration in the channel, which causes a threshold voltage shift.

5.3. GaN JBS Rectifier

A JBS rectifier combines a Schottky rectifier with a PIN diode. Originally proposed by Baliga for Si substrates, the metal-semiconductor interface that forms a Schottky barrier is augmented with a finely spaced junction grid [106]. Starting with a metal-n-semiconductor Schottky barrier diode, several small p-doped wells are fabricated with ion implantation. Under forward bias conditions the junction depletion layers do not pinch off the current flow, which is guided through multiple conductive channels. When reverse bias is applied, the depletion layers intersect under the Schottky metal. The Schottky barrier is shielded, which reduces the detrimental Schottky-barrier lowering effect prohibiting a hard breakdown characteristics. This is essential for high power rectifiers, which also benefit from the negligible diffusion capacitance of the underlying Schottky diodes structure. Switching losses are significantly reduced (compared to pn rectifiers) for high frequency operation ($f > 20\text{kHz}$) and the forward voltage drop is minimized [103].

5.3.1. GaN JBS Structure

For SiC JBS rectifiers usually a lightly doped epitaxial layer is grown on top of the highly doped substrate [2]. The GaN JBS rectifier presented by Zhang *et al.* [86] uses the same principle with

a n-doped GaN substrate. A schematic cross section of the device structure is illustrated in Figure 5.7. Therefore, a $7\ \mu\text{m}$ layer with a donor concentration of $N_D = 2 \times 10^{16}\ \text{cm}^{-3}$ is grown on top of the highly n-doped substrate. In order to fabricate the original JBS rectifier structure, Mg is implanted to form the p-doped wells. Zhang *et al.* reported an additional inverse structure that relies on Si implantation. A p-doped epitaxial layer ($N_A = 2 \times 10^{18}\ \text{cm}^{-3}$) is added on top of the n-doped epitaxial layer. By implanting Si, the p-doped background is locally inverted to n-type, leaving the unaffected regions as effective p-well behind.

Combining concepts of a Schottky rectifier and a PIN diode, the choice of the contact materials is essential for a JBS rectifier. While the cathode forms an Ohmic contact to the n-doped substrate, the anode metal is required to form a Schottky contact. The contact type is determined by the metal workfunction. For n-doped GaN aluminum can be employed for the Ohmic contact and nickel or gold for the Schottky contact.

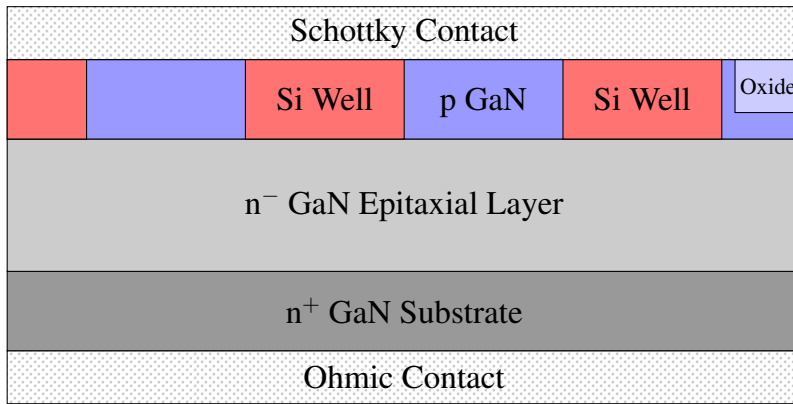


Figure 5.7.: Schematic cross section of the investigated GaN JBS rectifier. The oxide is deposited to achieve edge termination.

5.3.2. GaN JBS Process Simulations

The successfully calibrated modified empirical activation model (4.11) for implanted Si (Section 4.7.2) allows to simulate the fabrication of the Si implanted JBS rectifier. Regarding the implantation and annealing step, the major technological challenge is to ensure that the active Si concentration exceeds the acceptor concentration in the p-doped epitaxial layer. Otherwise, the conductive channels are not formed, prohibiting the intended operation of the JBS rectifier. Furthermore, the net doping concentration $N_{\text{Net}} = N_D - N_A$ determines the on-state resistance. Zhang *et al.* report a conversion (p-type to n-type GaN) efficiency of $\approx 1\%$ for the implanted Si concentration $C_x \approx 2 \times 10^{19}\ \text{cm}^{-3}$ for a subsequent $t_A = 2\ \text{min}$ annealing step at $T_A = 1050^\circ\text{C}$. In particular, the approximate net doping difference $N_{\text{Net}} = 5 \times 10^{16}\ \text{cm}^{-3} \dots 1 \times 10^{17}\ \text{cm}^{-3}$ has been determined using chemical CV measurements [86]. Assuming a fully activated p-doped epilayer, the active Si concentration amounts to $C_a = 2.1 \times 10^{18}\ \text{cm}^{-3}$. The high concentration of implanted Si indicates that the annealing process operates in the saturation regime $C_x \gg C_{\text{ss}}(T_A)$ (see Figure 4.10), for which $C_a \approx C_{\text{ss}}(T_A)$. Consequently, the modified empirical model is required to have $C_{\text{ss}}(1050^\circ\text{C}) = 2.1 \times 10^{18}\ \text{cm}^{-3}$, which is in accordance with the Arrhenius law established in Figure 4.15.

The calibrated modified empirical activation model allows to determine the spatial profile of active dopants during the simulation of the process steps (employing Silvaco's Victory Process simulator) required to fabricate the considered GaN JBS rectifier:

- Epitaxial growth of the n-doped and p-doped layer.
- Deposition and selective etching of an implantation mask (SiO_2) to define the well geometry.
- Ion implantation of Si.
- Annealing step employing the modified empirical activation model. The surface is capped with SiO_2 .
- Etching and SiO_2 deposition to achieve edge termination.
- Metal deposition to form the contacts (top and bottom).

The resulting JBS structure is shown in Figure 5.8. A periodic implantation mask enables spatially selective ion implantation forming a regular grid of implanted Si wells that locally converts the p-doped epilayer to conductive n-type channels. The resulting n-type and p-type regions have both a nominal width of $3\ \mu\text{m}$. Figure 5.9a depicts the doping profile for a vertical cut through the Si well. The electrically active acceptor concentration introduced by the p-doped epilayer is assumed to be $N_D = 2 \times 10^{18}\ \text{cm}^{-3}$. For the annealing time $t_A = 1050^\circ\text{C}$ that is employed by Zhang *et al.*, the modified empirical model gives a mean net doping concentration $\langle N_{\text{Net}} \rangle = 5 \times 10^{16}\ \text{cm}^{-3}$, which is in accordance with experimental observations. The electrical activation is strongly promoted by thermal energy. Therefore, elevated annealing temperatures significantly improve the activation efficiency of the implanted Si dopants. In particular, the net doping concentration can be raised by up to three orders of magnitude, which is shown in the inset of Figure 5.9a.

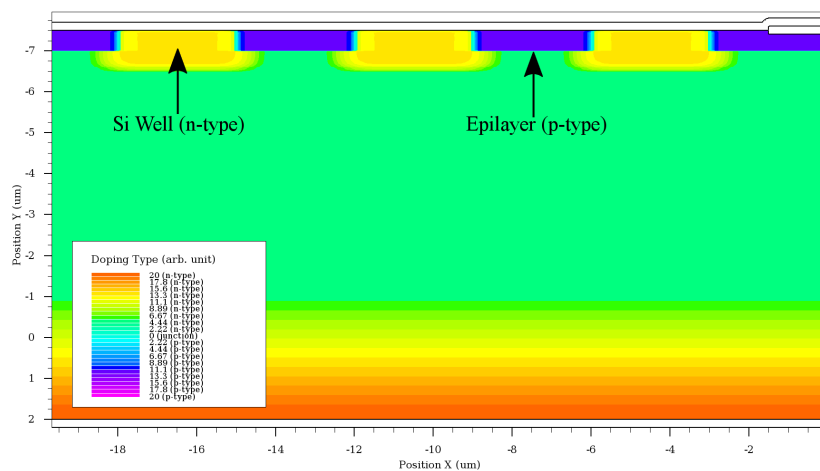


Figure 5.8.: Cross section from Victory Process simulator of the investigated GaN JBS rectifier annealed at $T_A = 1100^\circ\text{C}$. The implanted Si wells locally convert the p-type epilayer to n-type regions.

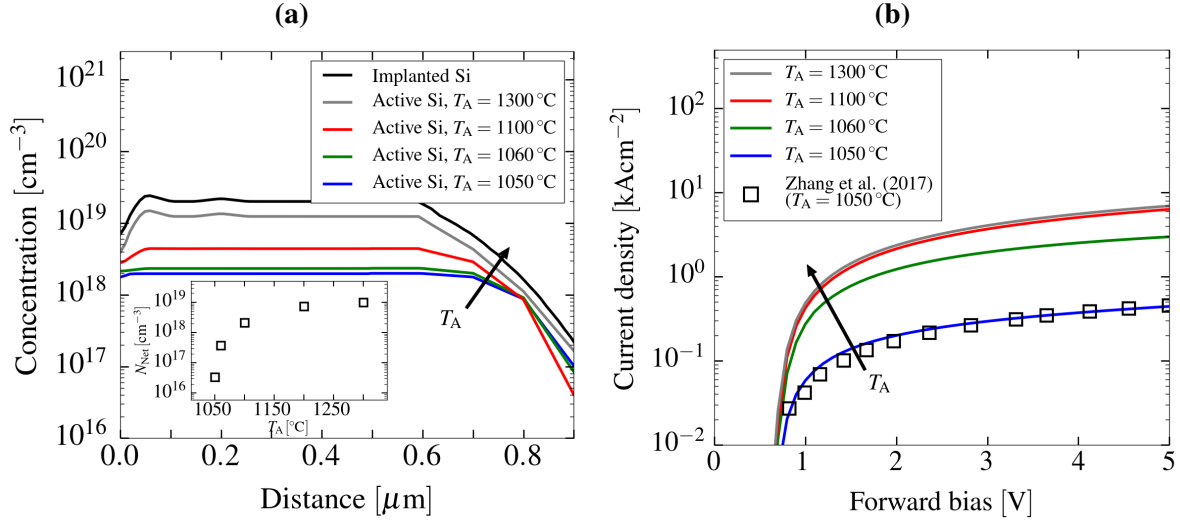


Figure 5.9.: (a) Doping depth profiles for the Si-implanted wells of the GaN JBS rectifiers. The dashed line refers to the acceptor concentration of the p-type epilayer. Elevated annealing temperatures T_A enhance the activation of Si and thus increase the net doping concentration N_{Net} , as shown in the inset figure.

(b) GaN JBS rectifier forward characteristics. The experimental device characteristics reported by Zhang *et al.* [86] is reproduced with high accuracy. Elevated annealing temperatures allow to reduce the on-state resistance by approximately one order of magnitude ($R_{\text{on}}^{T_A=1060^\circ\text{C}} \approx 0.97 \text{ m}\Omega$, $R_{\text{on}}^{T_A=1300^\circ\text{C}} \approx 0.58 \text{ m}\Omega$).

5.3.3. GaN JBS Rectifier Device Simulations

The JBS rectifier device simulations are also investigated using Silvaco's Victory Device simulator. As described in Section 5.2.3 the semi-classical drift-diffusion approach (5.1), (5.3), and (5.4) is employed. However, GaN differs from 4H-SiC in several carrier-transport related properties. In contrast to 4H-SiC, incomplete ionization can be accurately described with the single-level model (5.8). In the recent literature [107], highly specialized models and parameters concerning generation/recombination, bandgap narrowing, and carrier mobility have been summarized. The impurity concentration-dependent mobility for low electric fields is described with the Thomas Caughey model. For the high field mobility, the 'GaNsat High-Field Mobility Model' proposed by Farahmand *et al.* [108] is available in Victory Device.

The JBS rectifier structure relies on two different types of metallic contacts: a Schottky contact at the anode and an Ohmic contact at the cathode. At Schottky contacts the Fermi level of the metal is not aligned with the quasi-Fermi level of the semiconductor (GaN). In Victory Device this is taken into account by including the Schottky barrier for the calculation of the potential boundary condition (Dirichlet). The Schottky barrier is determined by the difference of the metal's and semiconductor's workfunction. For Ohmic contacts the Fermi levels are aligned and no Schottky barrier has to be overcome by the carriers. All employed models and the associated parameters are summarized in Appendix B.

The simulation of the forward characteristics of the considered GaN JBS rectifier reproduces the experimentally obtained forward voltage $V_{\text{on}} = 0.7 \text{ V}$ and the specific on-state resistance

$R_{\text{on}} = 7.6 \text{ m}\Omega\text{cm}^{-2}$. Figure 5.9b illustrates the strong impact of the annealing temperature on the device operation. Enhancing the annealing temperature from $T_{\text{A}} = 1050^\circ\text{C}$ to 1300°C results in a decrease of the on-state resistance by one order of magnitude. The electrical activation efficiency passes from the weakly activated state ($R_{\text{act}} < 0.05$) through medium activation to reach nearly full activation ($R_{\text{act}} > 0.95$) within a small annealing temperature band $\Delta T_{\text{A}} = 50^\circ\text{C}$. This phenomenon has also been experimentally observed in implanted SiC [37], [85]. The empirical activation model is capable of describing this distinctive property, as illustrated in Figure 4.9. Furthermore, the characteristic high temperature saturation behavior of activation efficiency directly translates to a current saturation as the annealing temperatures are raised. The remarkable impact of the active dopant concentration on the actual device characteristics confirms the high relevance of modeling capabilities for semiconductor processing steps, in particular post-implantation annealing.

6. Summary and Outlook

The wide-bandgap semiconductors SiC and gallium nitride GaN are highly attractive for application in power electronics due to their excellent material properties. However, both are challenging for process technology, in particular due to the issues in ion implantation and the subsequent thermal annealing steps, which strongly impact the final device's operation. In order to achieve high electrical activation efficiency of implanted SiC and GaN, remarkably high annealing temperatures (SiC: $> 1500^{\circ}\text{C}$, GaN: $> 1300^{\circ}\text{C}$) are necessary. In the course of this thesis, the micro-physical mechanisms that define the electrical activation of implanted regions were investigated. The formation of native and impurity related point defect clusters and agglomerates were found to limit the activation efficiency for high implantation doses.

A comprehensive study of annealing experiments in the literature culminated in developing an empirical model that predicts the electrical activation efficiency as a function of the main process parameters, namely annealing temperature, annealing time, and implanted dopant concentration. The presented model was calibrated for implantation and annealing of 4H-SiC with the acceptor species Al and B and the donor species N and P. Si-implanted GaN exhibits reduced activation efficiencies in the steady-state for low ($< 10^{17} \text{ cm}^{-3}$) and moderate ($\approx 10^{18} \text{ cm}^{-3}$) doping concentrations. A modified activation model and its calibration, which accurately describes this phenomenon, were presented and calibrated.

The activation models were incorporated into Silvaco's Victory Process simulator, enabling the optimization of the annealing parameters for semiconductor fabrication processes. Process simulations were coupled with device simulations utilizing Silvaco's Victory Device simulator, which allowed to investigate the full workflow of state-of-the-art power device structures: from fabrication to determining the electrical characteristics. The impact of the annealing parameters on the electrical behavior of 4H-SiC DMOSFETs and GaN JBS rectifiers was examined employing process and device simulations: Annealing temperature and annealing time strongly influence the threshold voltage of the 4H-SiC DMOSFET and is thus crucial for the final device characteristics. The on-state resistance of a Si-implanted GaN JBS rectifier was found to be reduced by more than one order of magnitude when employing elevated annealing temperatures. These results corroborate the high relevance of the annealing and the modeling capabilities of these fabrication steps and therefore underline this work's importance.

Even though the empirical models predict the electrical activation with high accuracy, the micro-physical mechanisms associated with implantation damage and activation are not yet fully understood for both GaN and SiC. Further investigations have to address the reasons for the reduced activation of Si-implanted GaN as well the generally low activation efficiency of acceptors. Furthermore, the impact of the annealing ambient, self-diffusivity of C, and complex RTA techniques on the activation processes of implanted SiC have to be examined. The simulation results suggest that elevated annealing temperatures allow to significantly shorten the annealing times. However, this requires further improvements of the surface capping technology.

A. Modeling Parameters for SiC DMOSFETs

Table A.1.: Victory Device (VD) simulator setup for 4H-SiC-DMOSFETs.

Model	VD Statement	VD Parameters	Comment
<i>General Setup</i>			
Drift Diffusion	(Default)	(Default)	
Fermi-Dirac Statistics	MODELS FERMDIRAC	None	
Two-Level Incomplete Ionization	(Default for SiC)	calibrated in VD	Do not set INC.ION in MODELS
<i>Contacts</i>			
Ohmic Contacts	CONTACT VOLTAGE	None	
Lumped Contact Resistance	CONTACT RESISTANCE=value OHMS	value is fit parameter	
<i>Bandgap Modeling</i>			
Universal Energy Bandgap Model (Varshni)	(Default)	EG300 = 3.235 EGALPHA = 3.3e-2 EGBETA = 1e5	Parameters set in MATERIAL
Bandgap Narrowing	MODELS BGN	calibrated in VD	
<i>Mobility Modeling</i>			
Uhnevionak Combined Mobility Model for 4H-SiC	MOBILITY ALTCVT.N ALTCVT.P	calibrated in VD for electrons MOBILITY: ALT.N.DELTA = 1.5e12 ALT.P.MUBP1 = 125 ALT.P.MUBP2 = 0 ALT.P.MUMIN = 15.9 ALT.P.ALPHA = -0.5 ALT.P.EXP1 = -2.15 ALT.P.EXP3 = 1 ALT.P.EXP4 = 0.34 ALT.P.NREF = 1.76e19	Low Carrier + Transverse-Electric-Field p values chosen to reproduce Caughey Tomas Model
High-Field Mobility (Canali)	MODELS FLDMOB	MATERIAL: VSATN = 2.2e7 VSATP = 1.0e7 MOBILITY: BETAN = 1.2 BETAP = 1.0	For simulations at T = 300 K
Anisotropic Mobility	MOBILITY	N.ANIOSTROPIC=1.2	
<i>Generation and Recombination</i>			
Shockley-Read-Hall	MODELS SRH	MATERIAL: TAUN0 = 1e-9 TAUP0 = 1e-9	
Auger Recombination	MODELS AUGER	MATERIAL: AUGN = 1e-29 AUGP = 1e-29	
Impact Ionization - Selberherr	IMPACT SELBERHERR	IMPACT: AN1 = 3.44e6, AN2 = 3.44e6 AP1 = 3.5e6, AP2 = 3.6e6 BN1 = 2.5e7, BN2 = 2.5e7 BP1 = 1.7e7, BP2 = 1.7e7 BETAN = 1.0 BETAP = 1.0	
Interface Traps	INTTRAP	ACCEPTOR: DENSITY = 3e+12 DEGEN = 12 E.LEVEL=0.075 SIGN=1-14 SIGP=1e-14	One effective acceptor-like trap

B. Modeling Parameters for GaN JBS Rectifiers

Table B.1.: Victory Device (VD) setup for GaN JBS rectifiers.

Model	VD Statement	VD Parameters	Comment
<i>General Setup</i>			
Drift Diffusion	(Default)	(Default)	
Fermi-Dirac Statistics	MODELS FERDIRAC	None	
Incomplete Ionization (Single level)	MODELS INCOMPLETE	MATERIAL: GCB=2 GVB=2 A.EAB=0.240 A.EDB=0.017 B.EAB=3.14e-8 B.EDB=3.4e-9	
<i>Contacts</i>			
Ohmic Contact	CONTACT VOLTAGE	None	
Schottky Contact	CONTACT WORKFUNCTION	5.25	
<i>Bandgap Modeling</i>			
Universal Energy Bandgap Model (Varshni)	(Default)	EG300 = 3.46 EGALPHA = 9.09e-4 EGBETA = 830	Parameters set in MATERIAL
Bandgap Narrowing	BGN	(Default)	
<i>Mobility Modeling</i>			
Caughey Thomas Model	MODELS ANALYTIC	MOBILITY ALPHAN.CAUG=-1.5 BETAN.CAUG=1.5 DELTAN.CAUG=0.81 GAMMAN.CAUG=3.02 MU1N.CAUG=115 MU2N.CAUG=1800 NCRITN.CAUG=7e16 ALPHAP.CAUG=2.0 BETAP.CAUG=-2.34 DELTAP.CAUG=-2.311 GAMMAP.CAUG=0.869 MU1P.CAUG=12.0 MU2P.CAUG=167 NCRITP.CAUG=3e17	Low field doping-dependent
High-Field Mobility for Electrons	MOBILITY GANSAT.N	(Calibrated in VD, only for electrons)	GaNsat High-Field Mobility Model
High-Field Mobility for Holes	MOBILITY FLDMOB.P	MOBILITY: BETAP=0.725 MATERIAL: VSATP=7e6	Caughey and Thomas High Field Model
<i>Generation and Recombination</i>			
Shockley-Read-Hall	MODELS SRH	MATERIAL: TAUN0=0.7e-9 TAUP0=2e-9	
Auger Recombination	MODELS AUGER	MATERIAL: AUGN=3e-31 AUGP=3e-31	

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Own Publications

Journal Articles

- [1] V. Šimonka, **A. Toifl**, A. Hössinger, S. Selberherr, and J. Weinbub. "Transient Model for Electrical Activation of Aluminium and Phosphorus-Implanted Silicon Carbide". *Journal of Applied Physics* (2018), accepted.

Conference Contributions

- [1] **A. Toifl**, V. Šimonka, A. Hössinger, S. Selberherr, and J. Weinbub. "Steady-State Empirical Model for Electrical Activation of Silicon-Implanted Gallium Nitride". *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)* (2018), submitted.
- [2] **A. Toifl**, V. Šimonka, A. Hössinger, S. Selberherr, and J. Weinbub. "Effects of Post-Implantation Annealing on Silicon Carbide DMOSFET Characteristics". *International Conference on Solid State Devices and Materials (SSDM)* (2018), submitted.

Erklärung

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct, insbesondere ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet. Die Arbeit wurde bisher weder im In- noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Wien, 22.5.2018

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