at the

Institute for Microelectronics
Vienna University of Technology

Two Year Report 2015-2016

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Contents

1   Introduction and Overview

As in the previous reporting periods, the Christian Doppler Laboratory for Reliability Issues in Microelectronics covered a number of the topics highly relevant for reliability of modern semiconductor devices and interconnects in the final two years of the project.

Recently, three-dimensional (3D) integration technology has become a major avenue of research to the fabrication of integrated circuits in the microelectronics industry. Although interconnect technologies for 3D integration show significant advantages, there are several reliability concerns. A key reliability issue in modern conducting structures is the influence of electromigration (EM) on interconnect lifetimes. The prediction of the EM lifetime becomes crucial for the assessment of interconnect reliability. In the reporting period, a particular focus of the works carried out in Module 1 was put on the modeling and simulation of EM in the through-silicon-vias (TSVs) and flip-chip solder bumps.

The research activities performed in Module 2 evolved around the reliability of transistors based on III-V nitride materials. The focus was put on were gallium nitride (GaN) devices which, according to numerous studies, represent the most promising solution for high-power, high-frequency, and high-temperature applications. In order to understand the degradation processes in GaN devices, the physics and morphology of different types of GaN defects were investigated.

In Module 3 reliability issues related to the mechanical stability and reliability of lined open TSVs, based on the tungsten metallization technology, were addressed. The cracking and delamination in the multilayer TSV structures are among the most important mechanical reliability issues for 3D integration interconnects. The different aspects of these phenomena and their influence on the overall reliability of the TSV interconnects were examined.

Regarding device reliability, both bias temperature instability (BTI) and hot carrier (HC) degradation mechanisms have been intensively studied. In 2010, the four-state non-radiative multiphonon (NMP) model was proposed to describe and explain experimentally observed degradation of MOSFET devices. Since the last report in 2014 an additional defect feature has been reported which is not covered by the original model. This observation required further development from four-state to a six-state NMP model which was carried out in the scope of Module 4.

Already known as a phenomenon difficult to understand and describe, HC degradation has become even more challenging to model for the case of LDMOS transistors. Here we have to deal with large device dimensions, high operating voltages, non-planar interfaces, and other design peculiarities. In Module 5, state-of-the-art physical models were successfully applied to study HC degradation of nLDMOS transistors.

Since the research activities of the Christian Doppler Laboratory are closely related to research activities at the Institute for Microelectronics, a smooth integration of the Christian Doppler Laboratory into the Institute for Microelectronics is achieved. This has been done by a close cooperation in common activities, by direct knowledge transfer, and by using the same simulators in a shared infrastructure.

2 CDL Members and Contributions

During the three year period 2012-2014 twelve scientists were supported by the Christian Doppler Laboratory:

1. Alexander Grill (01.03.2013 - 31.10.2016, Module 2)

2. Andreas Morhammer (01.05.2014 - 31.10.2014, Modules 4, 5)

3. Markus Jech (01.02.2016 - 31.03.2016, Module 5)

4. Santo Papaleo (30.10.2013 - 29.10.2016, Module 3)

5. Marco Rovitto (01.01.2015 - 31.10.2015; 01.01.2016 - 30.11.2016, Module 1)

6. Prateek Sharma (01.04.2013 - 31.03.2015, Module 5)

7. Wolfhard H. Zisser (14.11.2011 - 31.12.2013, Module 1)

8. Yannick B. Wimmer (01.10.2012 - 31.10.2016, Modules 4, 5)

The starting date of students' engagment in CDL is also the starting date of their Ph.D. thesis. Since the last report in October 2014 there have been no master thesis students in CDL.

Within the scope of the Christian Doppler Laboratory for Reliability Issues in Microelectronics the participants have been engaged in the following five projects:

Electromigration reliability of TSVs and solder bumps (Module 1)

EM modeling can significantly contribute to the understanding of the mechanisms governing the EM failure. It represents a multiphysics problem which can be divided into two phases, namely, the early phase of void nucleation and the late phase of void growth. The development of the two-phase model for EM and its implementation in a commercial software, based on the finite element method, allows to carry out numerical simulations in an efficient way. In the work reported here, EM simulations are performed in realistic interconnect geometries for 3D integration architectures in order to assess their reliability. Case studies of particular interest are open TSVs and flip-chip solder bumps. For the first case, EM failure is observed to initiate close to the metallization barrier between the via and the adjacent metal level. Once the void has nucleated, its growth is caused by the EM-induced-vacancy flux along the void surface. The combination of kinetics of both phases of failure provides a good estimation of the interconnect lifetime. In flip-chip solder bump technologies, EM enhances material composition changes which leads to a void nucleation at the bump/intermetallic compound interface. The analysis shows that the solder bump lifetime is dominated by the early phase failure. Simulations are capable of reproducing the EM phenomenon in diverse structures and ensure meaningful results for the evaluation of their reliability.

Threshold voltage drift in gallium gitride based MIS-HEMTs (Module 2)

III-V nitride based materials, especially GaN-based devices have been found to be good candidates for high-power, high-frequency and high-temperature applications. Despite superior material properties compared to conventional semiconductor material, widespread application of GaN based devices is currently limited by severe reliability issues like current collapse, hot carrier effects and threshold voltage (V_{th}) instabilities under forward bias conditions. To gain further insight into the cause of these degradation mechanisms, a detailed knowledge of the involved defect properties is substantial.

Unfortunately, due to the complicated electrostatics and the relatively high defect densities, experimental characterization of the responsible defects is extremely challenging. One reason is that for large area devices only ensembles containing a large number of defects can be assessed by measurement. The large trap densities involved in V_{th} drift complicate the analysis even more, since the Coulomb feedback of the traps as well as the stress history has to be taken into account for a correct understanding of the observed degradation.

To overcome this problem, nanoscale devices are very promising because they allow to investigate individual single-defect properties. Extracting their voltage and temperature behaviour allows to extract their vertical position as well as their electrical properties. We were able to extract four individual defects from random telegraph noise measurements in a nanoscale Fin metal-insulator-semiconductor high electron mobility transistor. The extracted properties suggest two strongly coupled pairs within the barrier, each couple sharing approximately the same vertical position and the same trap level. We think this could be a first step towards understanding the morphology of the defects involved into charge trapping in GaN/AlGaN based devices.

Mechanical reliability of open TSVs (Module 3)

During 3D IC stacking devices such as open TSVs can be subjected to unintentional extra forces leading to a failure of the structure. By simulating an external force acting on an open TSV the highest probability of a failure due to material cracking or delamination was found at the corner of the TSV bottom.

Subsequently the critical areas were localized, a delamination analysis was performed for the material interfaces of the multilayer structure at the TSV bottom. Delamination prediction is formulated by using the energy release rate generated during delamination propagation. If the energy release rate exceeds a critical value delamination propagates. Conditions such as the thicknesses of the layers, applied forces, and residual stresses of the involved material layers were varied to investigate which factor increase the probability of delamination propagation. SiO_2/W was found to be the most critical interface; when the W layer was assumed to carry a large value of intrinsic tensile stress, high values of energy release rate were obtained.

High values of intrinsic stress, in particular in the W conducting layer of the open TSV, increase the probability of delamination-induced failure. Therefore, a model was implemented to predict the stress build-up in thin metal film during deposition process. The model was

calibrated by using measured data for several materials and was used to investigate the film stress evolution during film growth on a scalloped surface. During TSV fabrication, due to the etching process used, a scalloped surface is formed along the TSV sidewall. Thin films grown on a scalloped surface develop a smaller intrinsic stress when compared to flat samples. Therefore, by controlling the process parameters during etching the intrinsic stress in the film can be minimized.

Extending the NBTI model to include volatility (Module 4)

In the previous reports, we have shown that BTI defects can be well described using our four-state non-radiative multiphonon (NMP) model. However, we have recently reported an additional defect feature [31] which is not covered by this model: Defects can become electrically inactive in our measurement window and then become active again randomly over a wide range of time scales. This behavior is observed for a majority of the defects and can be triggered by stress or by annealing at elevated temperatures. Therefore we suggest expanding the four-state model to a six-state model adding the inactive state 0 in a positively charged and neutral version. Using density functional theory (DFT) calculations in a-SiO$_2$, we recently have demonstrated that the Hydrogen Bridge and the Hydroxyl-E$'$ center are two likely defect candidates [27]. Removing the hydrogen atom from the defect site would make both candidates inactive. In the case of the Hydroxyl-E$'$ center, removing the hydrogen leaves a plain silicon-oxygen-silicon bridge. For the Hydrogen Bridge this would create an oxygen vacancy, which can be assumed to be an inactive state, since its defect level lies too low to be charged under our experimental conditions [27].

Reaction barriers for the hydrogen moving away from the defect site are expected to be close to the reverse-barriers for the formation of these defects. For the neutral case, these were calculated in [17], being too high (minimum 1.25 eV, average 2.4 eV) to explain the observed behavior. Therefore, we focused on the transitions starting from the positive states. We investigated the energy barriers of a hydrogen atom moving from the positively charged defect site to one neighboring oxygen atom, resulting in the new configurations. Due to the amorphous nature of the oxide, the properties of these defects are statistically distributed. A comparison can therefore only be made on a statistical basis. The data obtained from density functional theory calculations in a-SiO$_2$ were compared to the statistical properties deduced from experiments and good agreement was found.

Hot-carrier degradation modeling in high-voltage devices (Module 5)

We propose two different approaches to describe carrier transport in n-laterally diffused MOS (nLDMOS) transistor and use the calculated carrier energy distribution as an input for our physical hot-carrier degradation (HCD) model. The first version relies on the solution of the Boltzmann transport equation using the spherical harmonics expansion method, while the second uses the simpler drift-diffusion (DD) scheme. We compare these two versions of our

model and show that both approaches can capture HCD. We, therefore, conclude that in the case of nLDMOS devices, the DD-based variant of the model provides good accuracy and at the same time is computationally less expensive. This makes the DD-based version attractive for predictive HCD simulations of LDMOS transistors.

3   Scientific Cooperations

Scientific cooperations of CDL in the reporting period were:

- Research group of Prof. Peter Blaha, Institute of Materials Chemistry, Vienna University of Technology, Austria

- Research groups of Dr. Ben Kaczer and Dr. Kristof Croes, IMEC, Belgium

- Research group of Prof. Alex Shluger, University College London, UK

4   Project Reports

IN the following a more detailed description of the projects mentioned above is given. A detailed technical description can be found in the attached published papers.

4.1   Electromigration reliability of TSVs and solder bumps

EM-induced failure has been one of the main reliability issues in interconnects for 3D integration technologies since its potential degradation mechanism in metallization of integrated circuits is initiated by the transport of atoms due to the high current density which passes through the metal film. EM becomes a limiting factor for high current density flow in interconnects because it affects the long term interconnect behavior. EM failure mechanism is characterized by the development of the resistance as a function of time in the interconnect line, as depicted in Fig. 1. Two periods are observed in the EM resistance trace: a first flat constant part, followed by a sudden non-linear increase period. During the first period a small void nucleates and does not influence the current flow in the interconnect. As soon as the void size becomes larger, a measurable resistance increase with time begins. Thus, the complete EM failure time evaluation of the given interconnect requires both void nucleation and void evolution times. The contribution of each component in the EM time-to-failure (TTF) estimation depends on different kinetic and physical effects. The analysis of both failure phases is necessary for a better understanding of the EM problem in interconnects. In the following text, the EM modeling of each phase of failure development and their impact on the interconnect lifetime evaluation is presented in detail.
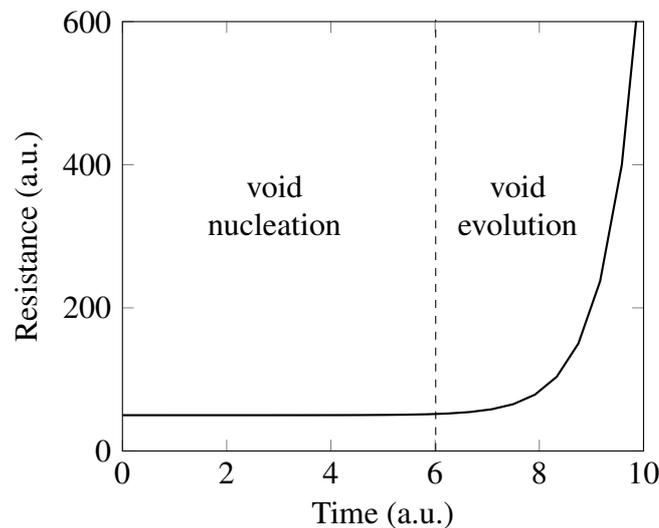

Figure 1

Typical EM resistance change with time for a given interconnect. Two EM failure modes are shown.

EM refers to the migration of atoms in the direction of the electron flow in a metal line. The atomic flux creates material accumulation on one end of the line and material depletion on the opposite side. Material depletion is generally described by vacancy accumulation, which is due to the transport of vacancies in the opposite direction of the electron flow in the line. The accumulation of vacancies leads to void nucleation and to the beginning of the wear-out failure mechanism in the interconnect. The vacancy flux $\vec{J}_v$ responsible for EM void nucleation failure in the conductor is induced by different driving forces [62] and can be written as

$$\vec{J}_v = D_v \left(\frac{e|Z^*|C_v \rho \vec{j}}{k_B T} - \nabla C_v - \frac{f \Omega C_v \nabla \sigma}{k_B T} - \frac{C_v Q^*}{k_B T^2} \nabla T \right), \tag{1}$$

where e is the elementary charge, Z^* is the effective valence, k_B is the Boltzmann constant, T is the temperature, D_v is the vacancy diffusion coefficient, C_v is the vacancy concentration, ρ is the metal resistivity, $\vec{j}$ is the electrical current density, f is the vacancy relaxation factor, Ω is the atomic volume, and σ is the hydrostatic stress. The first flux term on the right-hand side represents the flux induced by EM, while the other terms are components of the back-flux [3]. The temperature distribution is determined by the solution of the heat equation as

$$\nabla^2 T - \frac{\rho_m c_p}{k_t} \frac{\partial T}{\partial t} = -\frac{\gamma_E}{k_t} (\nabla \psi)^2, \tag{2}$$

where ρ_m is the metal mass density, c_p is the metal specific heat capacity, k_t is the metal thermal conductivity, γ_E is the electrical conductivity, and ψ is the electric potential. The change of vacancy concentration caused by the vacancy flux in the metal structure can be commonly expressed by the continuity equation

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G, \tag{3}$$

where G is the Rosenberg-Ohring function [61] that models creation and annihilation of vacancies at particular sites inside the line. In addition, the flux and the creation/annihilation of vacancies are accompanied by the development of inelastic strain in the line, which is the connection to the solid mechanics simulation [62]. The inelastic strain ε_v dynamics due to the pile up and the generation/annihilation of vacancies is given by

$$\frac{\partial \varepsilon_v}{\partial t} = \Omega \left[(1-f) \nabla \cdot \vec{J}_v + fG \right]. \tag{4}$$

Metal responds to inelastic strains by deformations or the build-up of stresses. The development of mechanical stresses in the structure is calculated by solving (3) and (4) together with the mechanical equilibrium equation, and also by coupling the standard electro-thermal equations [15]. The time evolution of the EM induced stress in a metal interconnect typically follows a square root time dependence [43]. As soon as the stress build-up due to EM reaches a threshold magnitude σ_{thr}, void nucleation can occur at the sites of weakest adhesion in the structure. Gleixner *et al.* [23] derived a simple equation for the prediction of the threshold stress value for a given interconnect, which is dependent on material interfacial properties and initial nucleus radius. The time required to reach the threshold value is called void nucleation time. It should be pointed out that the interconnect resistance change is practically

negligible for the whole void nucleation time period because small initial nucleus radii do not affect the electrical performances of the interconnect.

Once the location of void nucleation is identified in the interconnect structure, EM induced failure is ultimately caused by the growth of the fatal void. During this step, the void growth is governed by vacancy diffusion. It has been shown that the electron wind is the most dominant driving force in the vacancy flux responsible for the EM void evolution failure [56]. Therefore, in this context, the back-flux term in (1) can be neglected. The EM flux increases the void volume by feeding it with vacancies. The EM flux induces the void nucleation in the section of the interconnect, where the highest vacancy flux divergence is expected. The flow of electric current transports the vacancies towards this region, where they are captured at the void surface. They may diffuse along the void surface, causing the void to grow. The void volume V_v change in time, due to the captured vacancies at the void surface, is given by

$$\frac{\partial V_v}{\partial t} = f\Omega A_i \vec{J}_v = f\Omega A_i \frac{e|Z^*|D_v C_v \rho \vec{j}}{k_B T}, \tag{5}$$

where A_i is the cross sectional area of the given interconnect. Considering the case of an initial spherical void spanning the line, it is possible to approximate its evolution and local geometric features; a quarter-spherical void grows as

$$\frac{\partial V_v}{\partial t} = \pi r_v^2 \frac{\partial r_v}{\partial t}, \tag{6}$$

where r_v is the void radius. Using (5) and (6), the void radius change in time is written as

$$\frac{\partial r_v}{\partial t} = f\Omega A_i \frac{e|Z^*|D_v C_v \rho \vec{j}}{\pi r_v^2 k_B T}. \tag{7}$$

The flux of vacancies captured by the void surface strongly depends on the void size, additionally influencing the changes in current density and vacancy concentration distributions around the void itself [16]. Assuming a variable vacancy flux and integrating (7), the analytical model describing the time t necessary to grow a void of a given void radius becomes

$$t = t_0 + \frac{\pi}{\alpha} \int_{r_0}^{r} \frac{r_v^2}{A_i(r_v)C_v(r_v)\vec{j}(r_v)} dr_v, \tag{8}$$

where α includes all the constants and r_0 is the initial void radius corresponding to the time t_0. For each void size, the interconnect resistance is calculated by coupling numerical solutions of the current density and electrical potential distributions in the structure, respectively obtained from Ohm's law

$$\vec{j}(r_v) = -\gamma_E \nabla \psi(r_v), \tag{9}$$

and Laplace equation

$$\nabla \cdot (\gamma_E \nabla \psi(r_v)) = 0. \tag{10}$$

During the void evolution phase, the resistance of the interconnect rises by following nonlinear time dependence leading to an abrupt open circuit failure. Typically, the interconnect is considered failed when a resistance increase of 20% is reached. The time necessary to achieve the maximum tolerable resistance value is defined as void evolution time.

The two aforementioned failure phases give important contributions to the total EM lifetime estimation of an interconnect. The EM interconnect failure time can be expressed as the sum of void nucleation time t_N and void evolution time t_E

$$TTF = t_N + t_E. \tag{11}$$

The void nucleation time is defined as the time needed to reach the threshold stress for void nucleation, while the void evolution time is related to the time elapsed until the achievement of the maximum resistance failure criterion. Normally, Black's law is used to link the EM TTF and stress conditions of temperature and current density [15] as follow

$$TTF = A j^{-n} \exp\left(\frac{E_a}{k_B T}\right), \tag{12}$$

where A is a constant, n is the current density exponent, and E_a is the vacancy activation energy. Therefore, a comparison with Black's equation provides a more precise reliability assessment by determining the most dominant mechanism in EM failure.

Following this approach, the fully mathematical model for EM is implemented in a TCAD tool which allows one to carry out numerical simulations. Simulations start with solving the electro-thermal model in order to obtain the current density $\vec{j}$, electric potential ψ, and temperature T distributions in the interconnect from (9), (10), and (2), respectively. Then, the vacancy dynamics model has to be solved in order to determine the distribution of vacancy concentration C_v in the structure. This step is important because it solves the vacancy balance equation (3) which takes into account all the various driving forces for vacancy transport (1). The vacancy dynamics problem is followed by the solution of (4) of the solid mechanics model to obtain the stress σ distribution due to EM in the interconnect. The simulation continues until the threshold stress for void nucleation is reached at some location in the interconnect. Reaching the threshold stress implies void nucleation and the beginning of the second phase of failure development at this location. Once the void is formed, the void evolution phase begins. In a typical simulation procedure for void evolution, it is convenient to assume an initial small void located at the site of void nucleation. The method is based on the assumption that the radius r_v of the initial small void is increased for each time step in (7). Performing numerical simulations of the vacancy flux around the void as a function of void size, it is possible to obtain the time necessary to grow a void of a given radius from (8). EM simulations are performed in different case studies, which vary in the way the EM failure is triggered, such as an open copper TSV structure and a solder bump.

EM reliability is assessed for an open copper TSV structure, which represents one of the most common interconnect technologies employed for 3D integration, as depicted in Fig. 2(a). For this purpose a two-step approach based on the full EM model is followed. Operating conditions for EM simulations are set by imposing boundary conditions over appropriate regions of the case studied. All external surfaces of the structure are assumed to be under isothermal conditions. The outer materials surrounding the copper lines are taken to be rigid while the inner surface of the TSV (silicon nitride layer) is free to move. For the electrical loading, the left side of the copper at the TSV top is maintained at $J_0 = 1$ MA/cm^2 and the right side of the copper rerouting layer under the TSV bottom is set at ground.
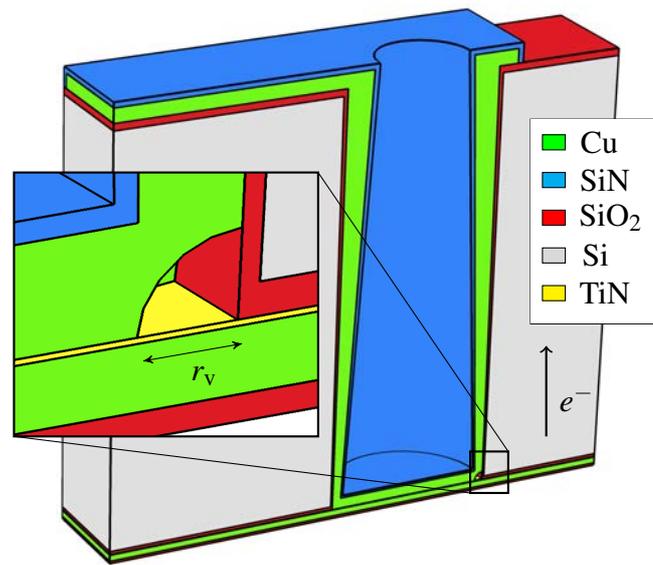
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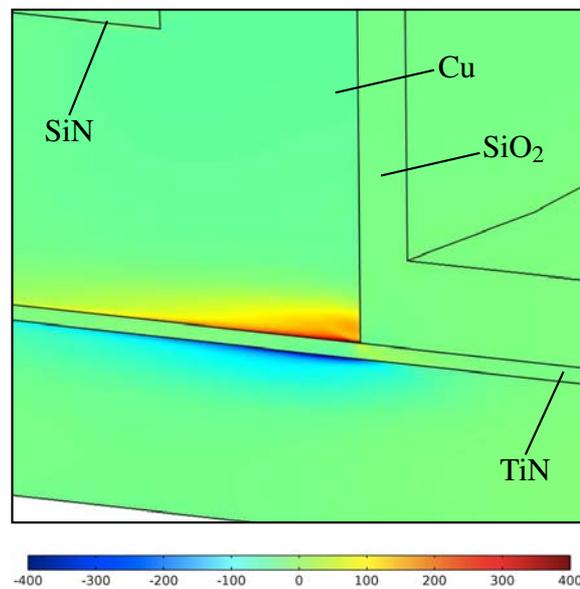
(b)

Figure 2

(a) Profile view of the analyzed open copper TSV structure. The arrow shows the direction of the current flow. The zoomed-in detail view of the TSV bottom depicts the location of the initial spherical void. (b) Profile view of the mechanical stress distribution (MPa) at the open copper TSV bottom after 10000 hours of current flow. The maximum tensile stresses are located at the Cu/TiN/SiO$_2$ layer intersection.

In the first step, the locations with the highest probability of void nucleation are identified in the TSV by monitoring the stress build-up due to EM in the structure. The identification of void nucleation sites in the open copper TSV is related to the primary material transport path

along which EM acts, namely the fast diffusivity path, which is recognized to be the surface of the nucleated void close to the metal-barrier layer interface. Simulation results show that vacancy accumulation and the consequent development of mechanical stress are recognized to be close to the interface between the copper line and titanium nitride layer at the TSV bottom, as illustrated in Fig. 2(b). This interface acts as an EM blocking boundary and prevents the vacancies from propagating into the barrier layer while current flows through the copper line. Therefore, vacancies accumulate at this location and lead to volume contraction of the structure resulting in the build-up of tensile stress. The stress distribution at such sites in the structure is monitored by increasing the current density of 30%. From the simulation results, it is possible to obtain the time evolution of the stress build-up due to EM for a total of four current densities (Fig. 3(a)). As expected [43], the maximum tensile stress increases with the square root of time, until it reaches the threshold value for void initiation. By following [23], the threshold stress σ_{thr} calculated for the particular case study is 0.33 GPa. The EM void nucleation time t_N for a given applied current density is determined as the time needed to reach the limit. The void nucleation time obtained for the case study varies between about one year and 80 days under accelerated conditions of current density j from 1MA/cm^2 to 2.2MA/cm^2, respectively. Furthermore, during this time period the TSV resistance does not change. The void has been nucleated and its small size is not able to produce a significant increase of the electrical interconnect resistance.

The second step of the analysis is characterized by the evolution of the void. The method described above is developed for numerically studying the time evolution of voids due to EM in the open TSV structure. An initial spherical small void of radius $r_v = 10$nm is placed at the void nucleation site in the structure, and its evolution is traced, including the current-crowding effect and the resistance increase. When a current loading is applied to the edge of a conducting metal line, the EM force leads to the growth of the void, which spans the line, and triggers electrical failure. It has been shown that the EM driving force increases the void by feeding its surface with vacancies. Electron wind therefore plays a key role in the dynamics of EM void evolution. From the simulation observations, it can be found that current crowding is more pronounced as soon as the void becomes larger. Fig. 3(b) shows the current density distribution close to the void nucleation location for different void sizes in the simulated structure. Electron flow leads to current crowding at the TSV bottom, towards the corner between void, copper, and barrier layer, even if the radius of the void is small in size (Fig. 3(b)(1)). Current crowding arises especially at the TSV bottom close to the sites of void nucleation because of the diverse layers' different geometries and values of electrical conductivity. Current flow tends to feed the void surface with vacancies, implying vacancy transport along it and consequently increasing the volume of the void. As soon as the void becomes larger, current density divergences are more prominent around the void surface as shown in Fig. 3(b)(2). The average current density over the void surface can be monitored at every point along the surface itself. Fig. 3(b)(2) shows that the main driving force affecting the diffusion of vacancies along the void surface is observed to be proportional to the tangential component of the current density to the surface. Peak values of j_{es} are located at the metal-void interface where current crowding is higher. The EM driving force causes significant void growth as the void propagates through the line. The growing void reduces the effective TSV conducting area at the bottom of the TSV leading to higher current crowding in these regions. Under these circumstances, it is obvious that
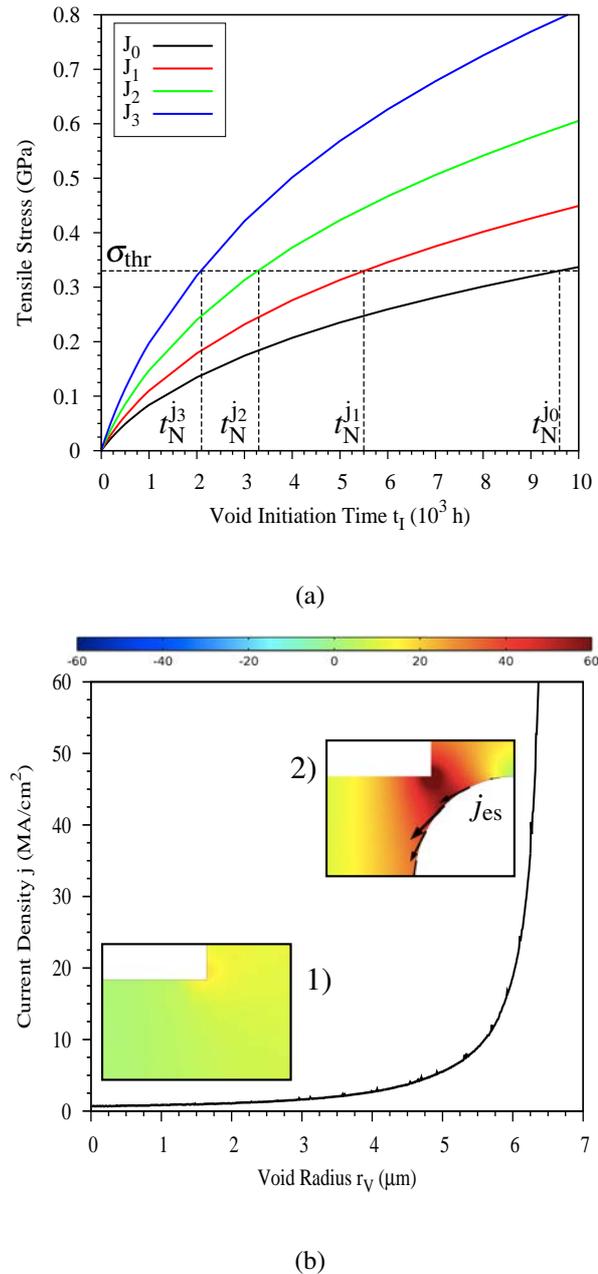
(a)

(b)

Figure 3

(a) Time evolution of the maximum tensile stress in the analyzed structure for different applied current densities. The EM void nucleation times t_N obtained for each curve profile are shown in the x-axis. (b) Current density dependence on void radius for the initial applied electrical loading j_0. Cross section views of the current density distribution are shown for two different void radii r_v: 1) 10nm and 2) 6μm. Current crowding increases as soon as the void becomes larger. The distribution of the average current density over the void surface is represented by the arrows.

as the line nears complete failure, the resistance of the interconnect rises non-linearly with time. The resistance change with time is associated to the growth of the void located at the Cu/TiN/SiO$_2$ layer intersection at the TSV bottom. The open TSV fails after the maximum tolerable resistance level is exceeded, typically a resistance increase of 20%. The EM void evolution time t_{E} is determined as the time needed to reach the maximum tolerable resistance value. The resistance increase of the given interconnect is monitored by increasing the initial current loading by 30%. The numerical simulation results of the flux of vacancies captured by the void surface which produce current density and vacancy concentration distributions changes around it are inserted into (8). By performing a numerical integration, it is possible to obtain the time necessary to grow a void of a given volume. Furthermore, numerical solutions of the electrical problem (9)-(10) allow to determine the interconnect resistance change during the void evolution period. In this way a relationship between the open copper TSV resistance and time for different initial electrical loadings can be shown in Fig. 4(a). Interconnect resistance changes in time until it reaches the common failure criterion of a 20% increase in resistance. EM void evolution time is related to the time elapsed until this value is reached.

Once both void nucleation and void evolution times were obtained, the evaluation of the complete EM lifetime was completed, as presented in (11). Finally, simulation results were fitted to Black's equation (12) and the current density exponent n is estimated, as depicted in Fig. 4(b). The result yields a value between 1 and 2 which confirms that both void nucleation and void evolution are important mechanisms in EM failure. A comparison of the simulation results with Black's equation reveals that the model based on the combination of kinetics of void nucleation and void evolution provides a good tool for the estimation of EM TTF in open copper TSV structures.

Another case study of particular interest was a flip-chip solder bump technology. A key feature of this structure is that EM failure is primarily determined by the void nucleation mechanism combined with the formation of an IMC at the interface between the Sn solder bump and the Ni UBM layer [10]. From the initiation of EM stressing, under accelerated conditions of increased temperature and current density, a continuous increase in the bump resistance is observed. After a certain period of EM stressing, the bump resistance starts to increase with a significantly steeper slope. Chen *et al.* [10] assume that the two slopes of the resistance growth represent two different stages of failure development: void nucleation combined with IMC growth and void evolution with IMC dissolution. Since interconnect EM resistance change with time is primarily determined by the void nucleation mechanism, the understanding of the early failure mode becomes decisive for a precise reliability assessment. The solder bump lifetime is influenced by the early phase of failure due to the presence of the IMC layer. Consequently, the prediction of the void nucleation time provides a realistic EM lifetime estimation of a given interconnect. Therefore, EM analysis was carried out by using the model describing void nucleation in order to simulate the mechanical stress build-up driven by the dynamics of vacancies in the solder bump depicted in Fig. 5(a). Pure tin (Sn) has been identified as the best material for ultra fine pitch solder bumps, due to its baseline advantages of being electrodeposited and due to its low melting temperature [10]. The top and the bottom of the spherical bump contact the cathode and the anode copper metallization, respectively. On the top, the Sn solder bump is connected to the cathode through an UBM,
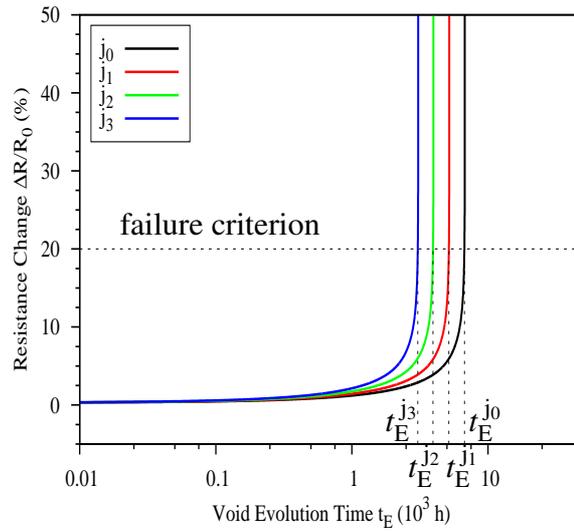
(a)
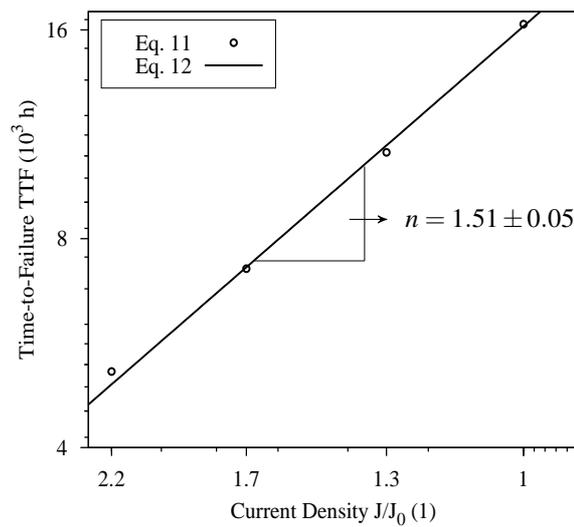
(b)

Figure 4

(a) Interconnect resistance change as a function of time for different applied electrical loadings. The failure criterion is a 20% increase in resistance. The EM void evolution times t_E obtained for each curve profile are shown on the x-axis. (b) Time-to-failure dependence on current density. The line indicates the fitting according to Black's equation and n is its angular coefficient.

which consists of a nickel (Ni) barrier layer. At the interface between Ni and Sn, an IMC will form due to EM and this region plays a key role when it comes to understanding the mechanism by which EM failure proceeds in solder bumps.

cathode

Cu
Ni
Sn

e^-

anode

(a)

-10   -5   0   5   10

Cu

Ni

Sn

Cu

(b)
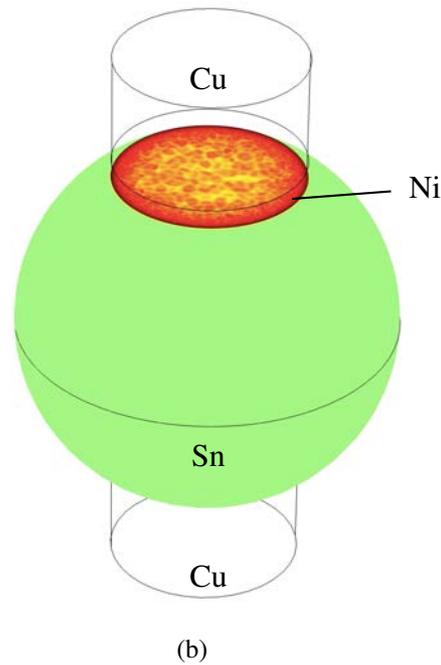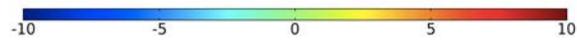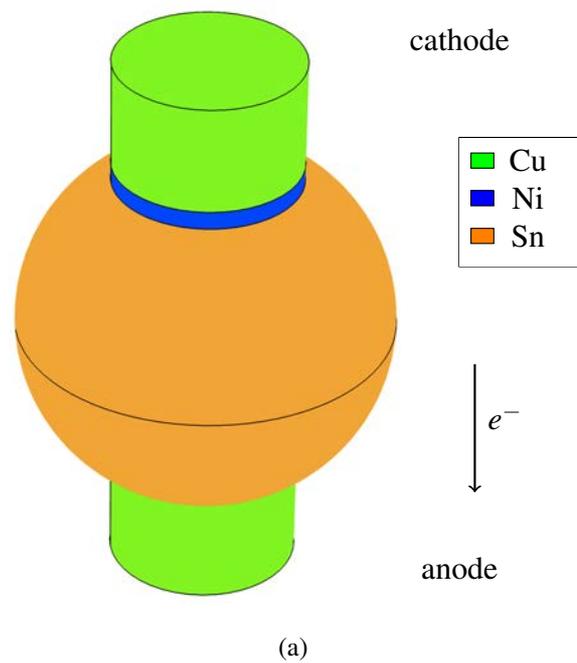
Figure 5

(a) Profile view of the solder bump geometry used for simulations. On the top of the Sn bump, a Ni UBM layer is placed. The arrow shows the direction of the electron flow. (b) Profile view of the mechanical stress (MPa) distribution in the Sn solder bump geometry after 14 hours of current flow. The maximum tensile stress is located at the top of the Sn bump beneath the UBM layer.

EM simulations are carried out under accelerated test conditions, which are set by imposing the following boundary conditions to the solder bump structure in Fig. 5(a). The temperature is kept constant at $T_0 = 473K$ for all external surfaces of the structure and the initial electric current density $j_0 = 0.003MA/cm^2$ is set at the anode end (copper metallization at the bottom of Fig. 5(a)). In turn, the zero electric potential condition is set at the top side of the cathode end (copper metallization at the top of Fig. 5(a)). For the mechanical problem, all outer surfaces of the structure are mechanically fixed.

From the simulation results, the location of void nucleation was identified close to the interface between the solder and UBM layer by monitoring the EM-induced stress build-up in the structure (Fig. 5(b)). During the formation of the IMC, the interaction between Cu, Ni, and Sn causes hydrostatic stress because of the resulting volume change. The accumulation of atoms may give rise to compressive stresses within the solder or at the solder/UBM interface and consequent hillock formation. In turn, at the specular side of the interface, vacancy accumulation would produce tensile stress and subsequent void nucleation. The hydrostatic stress distribution in the structure is monitored as can be seen in Fig. 5(b). A tensile stress increases from the center towards the periphery of the interface between the bump and the UBM layer, which leads one to the conclusion that a void most probably nucleates at the bump/UBM interface.

The time evolution of the stress built-up due to EM for a total of six applied current densities is shown in Fig. 6(a). As expected, at the initial stage the maximum stress exhibits linear growth with time. Subsequently, the stress increases in proportion to the square root of time, until it reaches the threshold value for void nucleation [43]. When a threshold stress in the order of 8MPa was reached at this site, the time necessary to nucleate a void was estimated in the range between 7 hours and 1 hour under stress conditions of current density from $0.003MA/cm^2$ to $0.008MA/cm^2$, respectively. At higher current densities the threshold stress for void nucleation is obtained in less time than at lower current densities. This implies that under higher current density stress conditions, the EM-induced vacancy transport at the bump/UBM interface is more efficient, since more vacancies are available in a cross section of the bump.

The scope of this study was the development of an analytical compact model for the estimation of the lifetime of the solder bump. An analytical solution of Korhonen's model [43] describes the time evolution of the stress σ build-up due to EM in a 1D structure as follows

$$\sigma(x,t) = \frac{2|Z^*|e\rho\, j\pi}{\Omega_a}\sqrt{\frac{kt}{\pi}}. \tag{13}$$

In the case of a 3D geometry, more vacancies are available in the cross section of the structure and $\sigma \sim jR^2\sqrt{t}$. By following (13) the compact model describing the time needed to reach the threshold stress σ_{thr} value in a solder bump, which depends on its radius, is obtained as follows
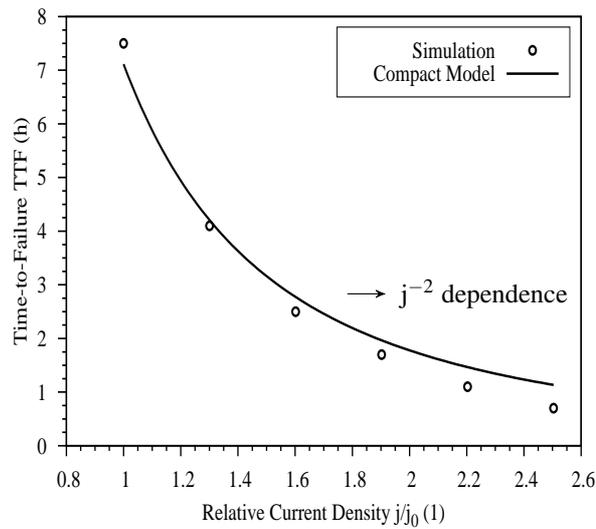
$$TTF = \frac{A\sigma_{thr}^2}{j^2R^4}, \tag{14}$$

where the constant A contains several material properties related to the solder bump. Lifetimes are extracted from the stress/time curves and are fitted to the compact model for

lifetime prediction presented in (14). The results obtained from simulations are in good agreement with the compact model.
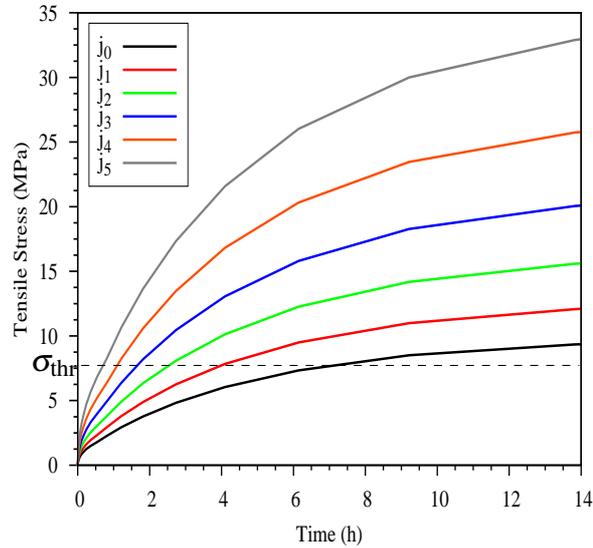
(a)

(b)

Figure 6

(a) Time evolution of the maximum tensile stress in the analyzed structure for six applied current densities. The threshold stress σ_{thr} for void nucleation is shown in the y-axis. (b) TTF depends on the current density. The solid line indicates the fit according to the compact model for lifetime prediction presented in 14.

Furthermore, similar to Black's equation (12), the failure time in (14) follows a j^{-2} dependence, which indicates that the void nucleation is the dominant mechanism of EM failure in the bump. Therefore, the development of a compact model for the prediction of the void nucleation time is beneficial for the estimation of the TTF for solder bump technologies.

The results obtained from the simulations of EM failure in the different case studies demonstrated the validity and capabilities of the EM model for the prediction of the EM lifetime of modern interconnects for 3D integration technology.

4.2 Threshold voltage drift in gallium nitride based MIS-HEMTs

When compared to other wide-bandgap materials like SiC, the GaN/AlGaN material system offers superior electronic properties in terms of on-state resistance, breakdown voltage or switching behaviour [38]. One important reliability issue currently limiting exploitation of the theoretical capabilities of GaN/AlGaN MIS-HEMTs amongst others is the V_{th} drift at forward gate-bias stress [53, 45, 46].

4.2.1 Charge feedback effects on threshold voltage drift in GaN/AlGaN MIS-HEMTs
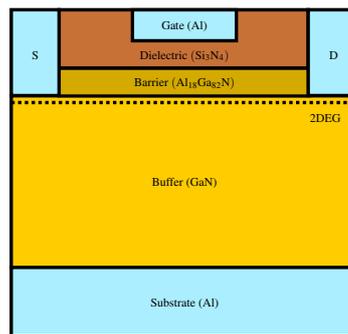
Figure 7

Simplified device geometry of our devices. A 10 nm thick AlGaN barrier is placed on top of a 1 µm thick GaN layer. The the gate dielectric is 25 nm thick and the gate length is 1 µm. For the simulations, the access regions as well as the source and drain lengths are scaled to 500 nm.

In this work, we showed that for large-area devices as shown in Fig. 7, the observed V_{th} drift can be understood as charge capture and emission events following a non-radiative multi-phonon mechanism with widely distributed parameters. Due to the large amount of traps present in the device, charge trapping has to be taken into account self-consistently for a correct description of their Coulomb-feedback on the device electrostatics. We also explained, how this feedback influences the individual trap properties and the observed ΔV_{th} drift [33].

Fig. 8 shows the simulated and measured recovery curves for measure-stress-measure sequences at different gate-stress conditions. The observed recovery behaviour can be described by two sets of Gaussian-distributed sets of NMP trap parameters in the vicinity of the dielectric interface. The influence of the trap occupancy on the degradation dynamics

can be seen in Fig. 9. This is in contrast to silicon devices, where this effect usually is negligible. The main reason for this is the barrier layer, which separates the trap sites from the main channel under recovery conditions. This leads to a very strong influence of the surface potential on the trap occupancies, equivalent to a decrease of the effective stress field applied to the device at a certain gate voltage. Another reason in the observed change of recovery dynamics can be found by changes in the local potential caused by the captured charges, changing the recovery behaviour of each trap individually.
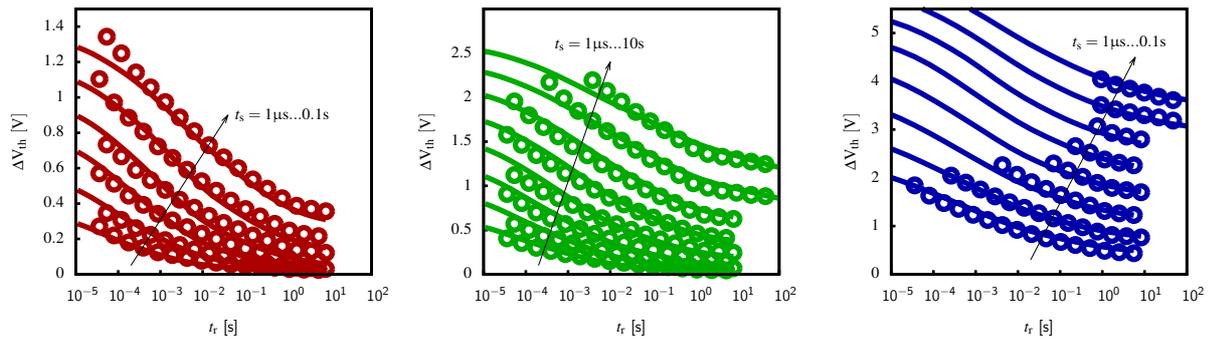
Figure 8

Simulated and measured ΔV_{th} recovery curves for measurement-stress-measurement sequences with stress voltages of 4 V (red), 5 V (green) and 10 V (blue). Note that the measured forward drift behaviour and its stress time and bias dependency is described by two sets of NMP trap parameters.
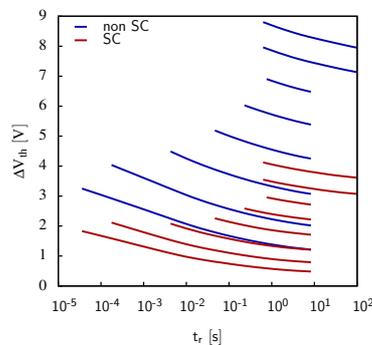
Figure 9

A comparison between self-consistent (SC) and non self-consistent simulation at Vg = 10 V. It can be seen that the influence of the trap occupancy on the degradation dynamics is very strong, which is in contrast to silicon based devices. For self-consistent simulations, the inhomogeneous potential in the oxide leads to changes in the shape of the recovery transients.

Due to these reasons, the observed degradation kinetics are strongly influenced by the stress history of the device. An accurate description of the degradation behaviour is thus only possible using transient, self-consistent simulations with an accurate replication of the measurement conditions.

4.2.2 Single-defect characterization in GaN/AlGaN fin-MIS-HEMTs

As mentioned in the last section, the GaN/AlGaN material system possesses superior electronic properties compared to conventional semiconductors. Unfortunately, the fabrication of normally-off devices, which are essential for switching applications, is still challenging. Recently a promising approach was presented by using nano-sized Fin-MIS-HEMT structures [36]. Just like in conventional MIS-HEMTs, charge trapping is a severe reliability issue also for these devices. The broad distribution of capture and emission times as well as their Coulomb feedback further complicate the analysis of trap properties in large-area devices, where only ensembles of defects can be measured [33, 47, 48]. In contrast to that, nano-scaled devices possess larger step-heights, which allow the investigation of single-defect properties based on the analysis of stochastic capture and emission events [24].
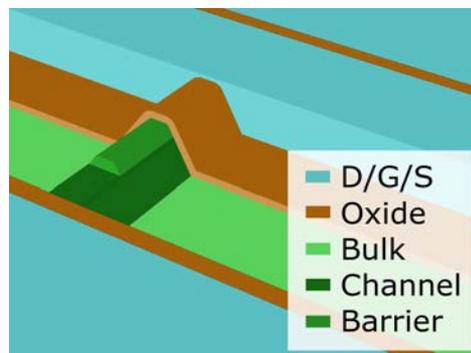
Figure 10

The simplified device geometry used for our simulations. A 30 nm thick AlGaN barrier is placed on top of a 80 nm thick GaN channel layer. The thickness of the Al_2O_3 gate oxide is 20 nm and the fin length is 1 μm [36].

To study charge trapping at the single-defect level we probe a 50 nm x 1 μm Fin-MIS-HEMT [36] shown in Fig. 10. We were able to identify four defects producing correlated RTN using our TDDS measurement instrument (TMI) [51] as shown in Fig. 11. In order to extract their defect properties, we collected the charge capture and emission events across several voltages and temperatures. The bias and temperature dependence of the four extracted defects is given in Fig. 12.

Given the voltage and temperature behaviour of the four individual defects, we were able to extract their vertical position as well as their trap level using a two-state NMP model [24]. The reaction barriers for capture and emission times, $\mathscr{E}_c$ and $\mathscr{E}_e$, were calculated from the Arrhenius equation. With the surface potential $\varphi_{s,0}$ and the band offset of the AlGaN layer at the hetero-interface φ_{ch} taken from TCAD simulations, they can be calculated using equations (15) and (16):

$$y_{trap} = \left(t_{bar} + t_{ox} \frac{\varepsilon_{bar}}{\varepsilon_{ox}} \right) \left(\frac{\partial \mathscr{E}_c}{\partial V_g} - \frac{\partial \mathscr{E}_e}{\partial V_g} \right) \tag{15}$$

$$E_T = \left(\frac{\partial \mathscr{E}_c}{\partial V_g} - \frac{\partial \mathscr{E}_e}{\partial V_g} \right) V_{g,int} + (\varphi_{s,0} - \varphi_{ch}) \frac{y_{trap}}{t_{bar}} + \varphi_{ch} \tag{16}$$

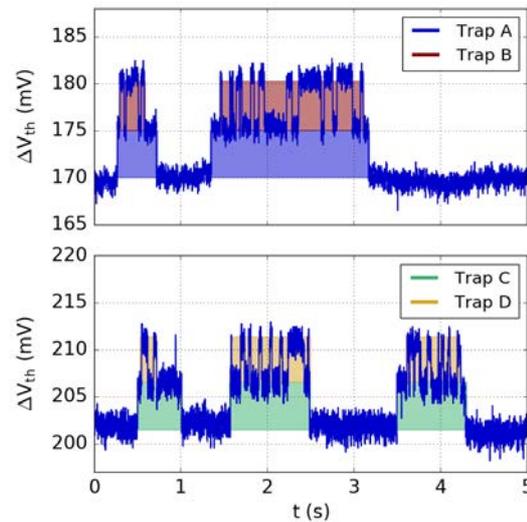The results of the parameter extraction of all four defects are given in Table 1. The trap positions of the correlated trap pairs 'AB' and 'CD' are in close vicinity to each other. Since the intersection points also match, they share a similar trap level although their absolute time constants have a difference of at least one order of magnitude. The relaxation energy $E_R \approx 4E_A$ of the NMP process can be calculated from the activation energy extracted from the Arrhenius plot (not shown) [24]. The explanation for the observed behaviour, namely (i) the correlated RTN behaviour, (ii) the similar trap levels and (iii) the similar voltage behaviour, can be the local surrounding seen by the defects 'B' and 'D', which obviously changes if defects 'A' and 'C' capture a charge.

Trap	y_{trap} (nm)	E_T (eV)	k_0 (s^{-1})	E_R (eV)
A	6.7	0.63	1.1×10^7	0.63
B	5.8	0.59	5.5×10^9	0.61
C	9.2	0.68	7.3×10^6	0.59
D	9.8	0.72	5.2×10^9	0.62

Table 1

The defect properties extracted from Fig. 12. The extracted trap levels of the defect pairs match closely, confirming their similar positions within the barrier. Their similar intersections, their voltage dependence and their correlated behaviour suggest that the potential energy surface around defects 'B' and 'D' changes once if defects 'A' and 'C' have captured an electron.
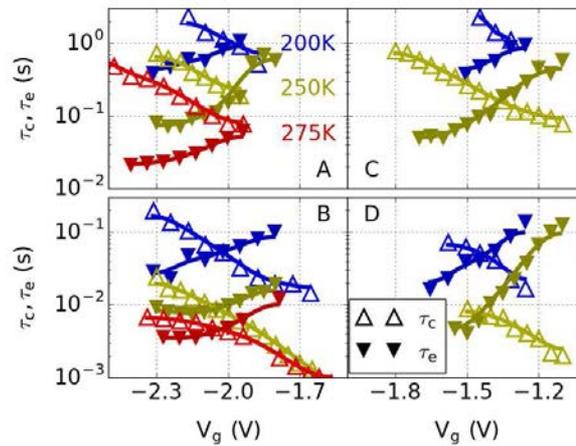
Figure 12

The weak voltage dependence of the capture times of the four individual defects suggests a defect location close to the channel. Further evidence for this assumption is given by the fact that the RTN occurs at negative gate voltages, where electron trapping through the barrier into oxide defects is very unlikely. The defect pairs share the same intersections and voltage dependency, suggesting a strong electrostatic coupling.

4.3   Mechanical reliability of open TSVs

The mechanical reliability of open W-lined TSVs was analyzed by performing mechanical simulations. Different sources of mechanical stress can be identified during 3D-IC stacking [22]: mechanical stress generated due to bonding pressure and temperature [35, 11] or due to unintentional indenters and loads (for example due to the presence of dust particles in a contaminated environment) [41]. We have considered these stresses as an external load acting on an open TSV. During the stacking process mechanical stress can evolve in the TSV structure, generating mechanical instability through cracking or delamination in the device. COMSOL Multiphysics FEM [12] was used to simulate the application of an external load (indenter) on an open TSV, as shown in Fig. 13. From the simulation results, information regarding the development of mechanical stress in the device are obtained. The bottom of the TSV under consideration consists of a multilayer structure which corresponds to the Al based interconnect structure for CMOS technology [44]. In the simulations the bottom part of the open TSV was mechanically fixed laterally at the Si sidewall. The bottom area was thereby "free" to bend in the *y*-axis direction (red arrow in Fig. 13). In the following, the many-layered structure is diagrammatically depicted as a single layer, denoted as "multilayer" in Fig. 13 and it corresponds to oxide, nitride, and aluminium layers. These layers are materials with different thicknesses and mechanical properties. In the implemented model, the elastic-plastic behavior of the materials was considered. The elastic behavior was reproduced with Hooke's law. The plastic behavior was described by employing an isotropic hardening law [12, 50]. An elastic-plastic material is usually modeled under the assumption that the strains ε and strain increments $d\varepsilon$ formed by the elastic and plastic part can simply be added together. By coupling the elastic part ε_e, described by Hooke's law, and the plastic part ε_p,

the stress σ in a material can be described as [5, 34, 58]

$$\sigma = \mathbf{C} : \varepsilon_e = \mathbf{C} : (\varepsilon - \varepsilon_p), \tag{17}$$

where $\mathbf{C}$ is the elasticity tensor. In the theory of plasticity, it is possible to describe yielding in the terms of σ only by means of a yield function. Therefore, a yield function can be used to define the onset of the plastic behavior. Given a yield function $F_y(\sigma, \sigma_{ys})$, which defines the limits of the elastic regimes, when $F_y(\sigma, \sigma_{ys}) < 0$ the material reacts elastically and when $F_y(\sigma, \sigma_{ys}) \geq 0$ it begins to deform plastically [50].

$\sigma_{ys}(\varepsilon_{pe})$ is the current yield stress which evolves during plastic flow and is described by an isotropic hardening law. The isotropic hardening law under consideration is a linear equation described by

$$\sigma_{ys}(\varepsilon_{pe}) = \sigma_{ys0} + \frac{E_{Tiso}}{1 - \frac{E_{Tsio}}{E}} \varepsilon_{pe}, \tag{18}$$

where σ_{ys0} is the initial yield stress (a material property), which indicates the stress level at which plastic deformation occurs. As can be seen in (18) $\sigma_{ys}(\varepsilon_{pe})$ is determined by the isotropic tangent modulus E_{Tiso} and the effective plastic strain ε_{pe}. The yield level increases proportionally with the effective plastic strain ε_{pe} [12, 50]. The yield function is defined as

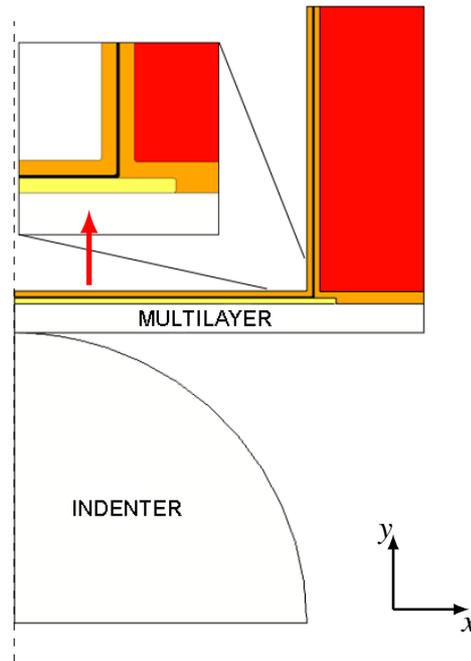$$F_y = \sigma_{mises} - \sigma_{ys}(\varepsilon_{pe}), \tag{19}$$

Figure 13

Two-dimensional representation of a TSV structure and an indenter. The dashed line indicates the axis of symmetry. Only a quarter of the system is represented. Al is shown in yellow, W in black, SiO$_2$ in orange, and Si in red. The multilayer consists of different materials. The indenter is spatially external to the TSV (the via height and width of the TSV in the figure do not represent the real size, under consideration).
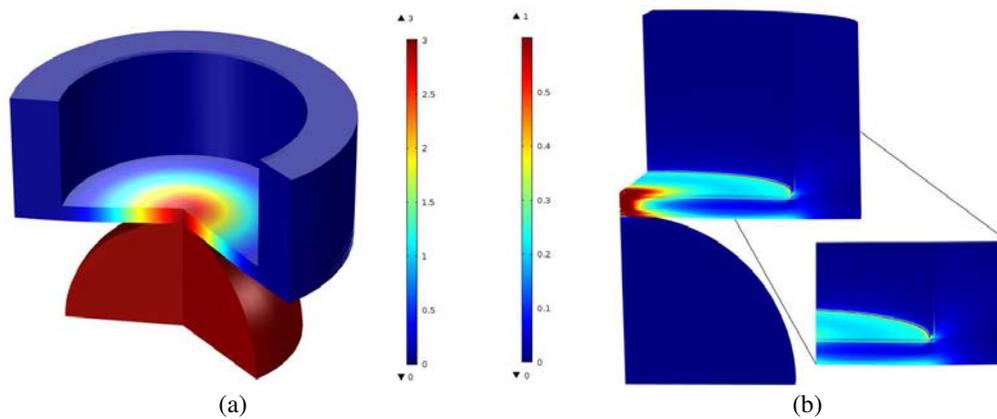
(a)　　　　　　　　　　　　　　　　(b)

where σ_{mises} is the Von Mises stress. The presented model was calibrated using experimental data from an industrial partner. The experimental data were obtained for a displacement of an indenter into the surface up to approximately 3 μm. In Fig. 14 (a) the simulation result shows the indenter at the highest prescribed indentation displacement. From the experimental data it was possible to obtain the load-displacement curve (cf. Fig. 15). The loading plot provides information about the mechanical properties, as well as the failure of the device.

In Fig. 15 the red and black lines indicate the experimental and simulation, respectively. Due to the complex, multilayered architecture of TSVs, the experimental results do not represent the behavior of only one material, but rather the behavior of a multilayer structure. The plastic response of plastic materials during loading was described in (18), where the yield stress and isotropic tangent modulus are the fitting parameters [19, 20, 57]. By changing the material parameters, a good match with the experimental data was found. It is particularly important to have a good fit for low loads of the indenter, in the range of 0 to $0.1 \times F/F_0$ because, in this range, only the elastic behavior of the materials influences the result.

Fig. 14 (b) depicts the normalized Von Mises stress due to the penetration of the indenter in the TSV. Two locations with high mechanical stress can be seen. The first is above the indenter and the second is located at the bottom corner around the TSV sidewall. The first interaction with the indenter generates a critical mechanical stress only at this location. As the indenter penetrates into the TSV, the mechanical stress develops and becomes high at the bottom corner around the TSV sidewall. The inset in Fig. 14 (b) depicts in detail the distribution of the Von Mises stress in the W layer.

In the areas with high concentration of mechanical stress the probability of device failure, such as cracking or delamination, is highest. Therefore a delamination analysis was performed at the material interfaces that compose the TSV bottom. The effects of external
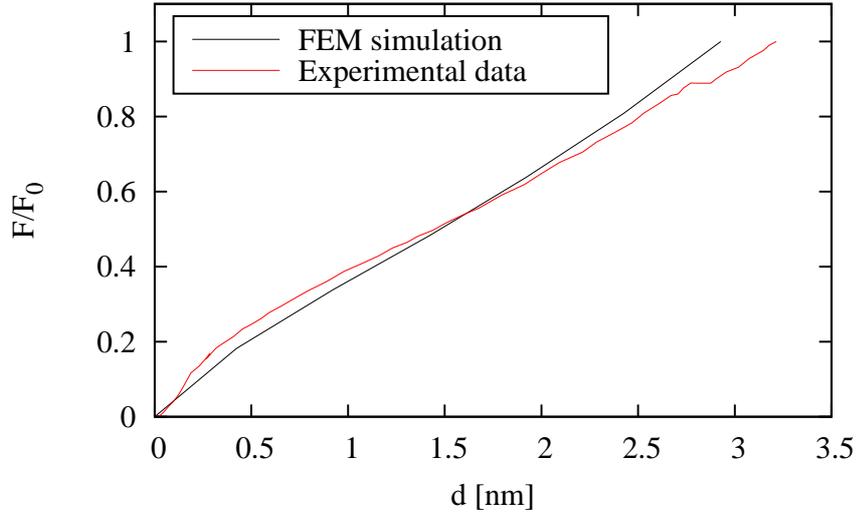
forces, thickness of the layers, and residual stress of the layers on the delamination propagation were investigated.

The critical energy release rate G_c is used as condition for a fracture (crack or delamination) to propagate. When the energy release rate G exceeds the G_c a fracture propagates.

The G_c is calculated by measurements and G_c values for different interfaces can be as well found in literature. The energy release rate G is the released energy during an infinitesimally small crack advance dA (A indicates a crack area in 3D and a crack length in 2D)

$$G = -\frac{d\Pi}{dA}, \tag{20}$$

where Π is the total potential energy composed by the total strain energy and by the potential due to external forces.

We calculated the energy release by using the *J*-Integral method [60, 6, 70]. The *J*-Integral is evaluated along a path Γ around the crack-tip of a cracked body. The path thereby can be arbitrary chosen as long as the crack-tip is inside the region surrounded by the path [70].

The definition of the *J*-Integral is given by

$$J = \int_{\Gamma} \left(W\,dy - T_i \frac{\partial u_i}{\partial x} ds \right) = \int_{\Gamma} \left(W n_x - T_i \frac{\partial u_i}{\partial x} \right) ds, \tag{21}$$

where W is the strain energy density, T_i are the components of the traction vector, u_i are the components of the displacement vector, and n_i are the components of the unit vector perpendicular to the integration path.
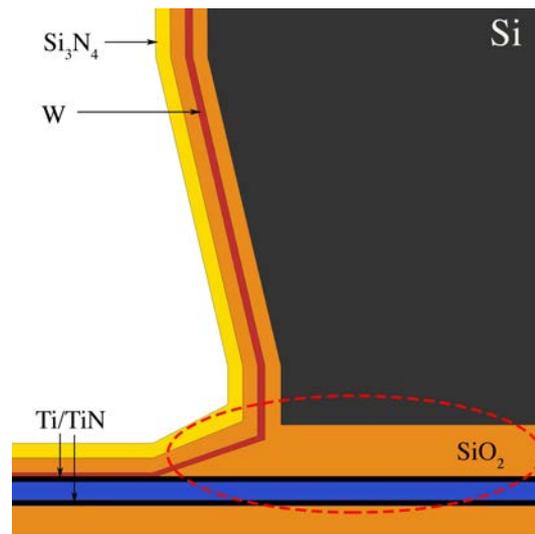
The energy release rate G was calculated for the different interfaces at the bottom of the TSV by using COMSOL Multiphysics FEM [12]. Considering the bottom of an open TSV free to bend, cracking or delamination of the layers has to be expected under the sidewall (cf. red circled region Fig. 16).

The four interface systems found in the open TSV are Ti/Al, SiO_2/TiN, SiO_2/W, and Si/SiO_2. For the prediction of failure due to delamination, the values G were compared with critical values G_c taken from [81, 82, 40, 13].

Two-dimensional simulations for the structure shown in Fig. 17 were carried out. All the layers have a length w of 20 μm and the thicknesses of the layers was varied.
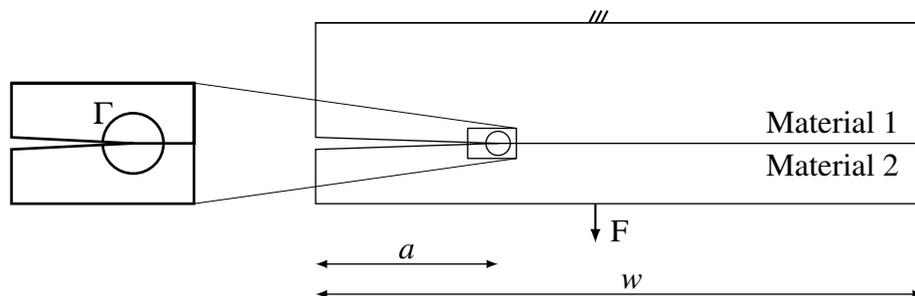
By varying the following factors their influence on G was investigated:

- **Residual stress:** It was simulated adding the initial stress in each considered layer. It was introduced by setting σ_{xx} and σ_{yy} to the assumed stress values. The residual stress in the layer is due to the deposition process and thermal processes. Small changes in residual stress influence the value of G.

- **Thicknesses of the layers:** The thickness of the layer influences the G and different values were employed to find the critical condition for the delamination.

- **External force:** It represents extra mechanical stress during the 3D-IC stacking [22].

The effects of the factors described above on the G can be summarized as.

- **Residual stress:** In the SiO_2/W interface, the probability of delamination propagation occurs when: high values of initial stress in the W are used or high crack lengths are assumed (cf. Fig. 18 (a)). For these conditions G exceeds G_c (0.2-0.5 J/m^2 [81]). The SiO_2/TiN interface shows the possibility of delamination propagation only for high values of compressive initial stress in the TiN layer. The variation of initial stress in the SiO_2 does not produce high G values decisive for mechanical failure. The Si/SiO_2 interface remains stable for every crack length and initial stress chosen. Critical energy release rates are not available in literature for the interface Ti/Al. A qualitatively estimation of the delamination can be given. As the obtained energy release rate is very small, no delamination propagation in this interface is supposed.

- **Thicknesses of the layers:** Different values of thicknesses of the layer change the value of G. From simulations it is possible to suppose that for long crack lengths the thickness of the layer has an important effect on the stability of the interface (cf. Fig. 18 (b)). Usually a thickness decrease strongly increases G. This is not applicable for the interface SiO_2/W where as well at high thicknesses a high G was obtained.

- **External force:** The increase of the force leads clearly to an increase of G. This effect is not valid for every interface. The force has a stronger effect at the interface SiO_2/TiN than the interface Si/SiO_2 where a small increase of G in function of the load is observable. The stability of these interfaces was demonstrated up to a force of 210 mN.

The main critical factor for the mechanical stability of open W-lined TSV is the residual stress of the W film which have a strong impact on the interfaces which are part of the TSV. By reducing the residual stress of the W film the probability of delamination propagation can be reduced in open TSV. Therefore through modeling and simulations we investigated the mechanisms behind stress development during film growth. This is essential to understand how the mechanical reliability of interconnects can be improved. Typically, in materials used for interconnects in microelectronic circuits, the growth process follows the Volmer-Weber (V-W) mechanism. We have implemented a model describing the stress evolution during the three steps of V-W growth for materials with a low adatom mobility using COMSOL
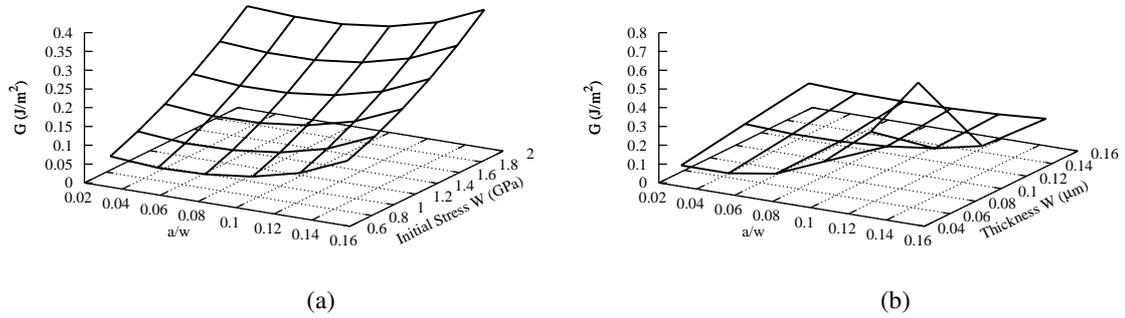
Figure 18

In (a) the energy release rate G for different initial stresses (W) and crack lengths in the interface SiO2/W. In (b) the energy release rate G for different thicknesses (W) and crack lengths in the SiO2/W interface.

Multiphysics FEM. During the V-W mode three unique growth steps can be distinguished (Fig. 19). Each step affects the film microstructure and consequently the physical properties of the film. The first growth step consists of the nucleation of islands in the film deposition process as shown in Fig. 19 (a). In this step a compressive stress is generated and is described [63] by

$$\sigma_{\text{comp}} = f \left(\frac{1}{R} - \frac{1}{R_{\text{fr}}} \right), \tag{22}$$

where f is the surface stress, R is the island radius, and R_{fr} is the frozen-in radius. This equation is used in our model to describe the initial compressive stress observed at the early stage of film growth prior to island coalescence.

During the second growth step the islands grow larger in size and start to impinge on each other, forming a continuous polycrystalline film. This step is commonly referred to as the island coalescence process (illustrated in Fig. 19 (b)). In recent years, several approaches for the computation of the tensile stress generated by island coalescence have been formulated [63, 55, 21]. For our chosen model's geometry, we consider the approach described by Seel [63], where the generated average tensile stress in the continuous film is given by

$$\langle \sigma \rangle = \sqrt{\frac{1}{9} \left(\frac{E}{1-\nu^2} \right) \frac{(2\gamma_{\text{s}} - \gamma_{\text{gb}})}{r}}, \tag{23}$$

where E is the Young's modulus, ν is the Poisson's ratio, γ_{s} is the surface energy, γ_{gb} is the grain boundary energy, and r is the radius of the island R at the coalescence point. In this study (23) was used to describe the tensile stress generated during the island coalescence process. The equation can be applied to predict the average film stress by using parameters γ_{s} and γ_{gb} from literature [80].

After island coalescence film thickening takes place. In this third step the formed film continues to thicken and gain volume until the deposition process is interrupted; this step
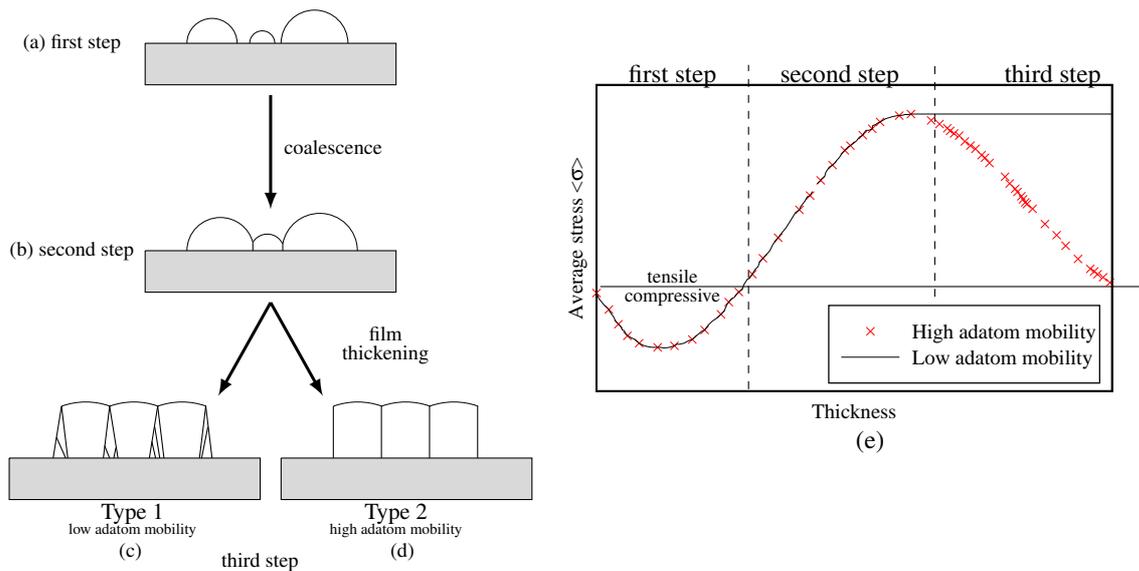
Figure 19

Three steps of the V-W growth process on the left-hand side of the picture. (a) Indicates the nucleation of the islands where compressive stress occurs, (b) indicates the coalescence process where the islands impinge upon each other, and (c)-(d) is the thickening process where a homogeneous film is formed. The properties of the deposited material distinguish two kinds of microstructure: Type 1 (for low adatom mobility materials) or Type 2 (for high adatom mobility materials). (e) Depicts stress evolution during the deposition process for both types of materials.

is shown in Fig. 19 (c)-(d). During the thickening process the structure of the grains and their evolution are strongly influenced by the adatom diffusivity of the material employed in the deposition process. There are two different types of grain-structure evolution. Materials with low adatom mobility (high melting temperature) exhibit a columnar grain structure with increasing grains during thickening referred to as Type 1; this type is depicted in Fig. 19 (c). In these materials (e.g. Si, W, Fe), the adatom diffusivity is relatively low even at high processing temperature. In materials with high adatom mobility (low melting temperature), the microstructure forms equiaxed grains which continue to evolve during film thickening. This process is typically found in Al, Ag, Au, and Cu, depicted in Fig. 19 (d), and is referred to as Type 2. Usually, materials with low adatom mobility exhibit a large tensile stress which remains constant throughout the thickening process [7, 42] (cf. Fig. 19 (e)). For these materials, we consider the third step under the assumption that the stress generated during the second step remains constant throughout. By using the described theories the intrinsic stress generated during the deposition processes of W were investigated.

By applying (22), compressive stress generation in the islands during the first growth step was simulated. The estimation of the magnitude of the stress is a very challenging task due to the lack of experimentally confirmed parameters. Nevertheless qualitatively information regarding the stress distribution in the substrate before the coalescence of the islands can be obtained.
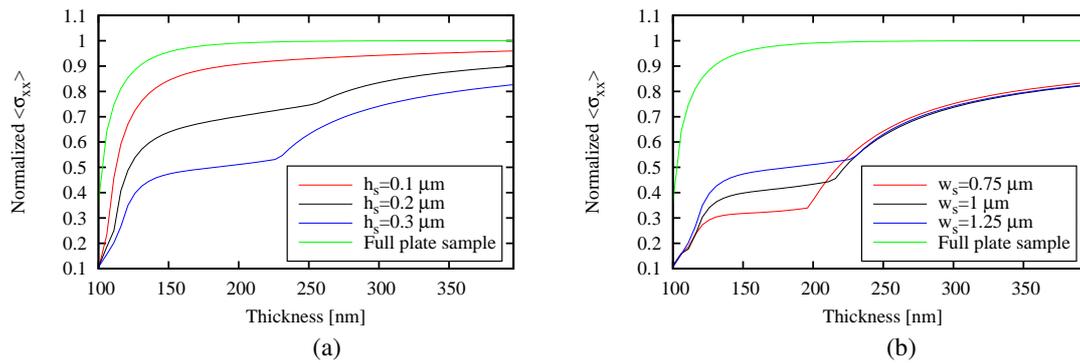
Using (23) the second step regarding the process of island coalescence was examined. At small thicknesses, the shape of the island, grain sizes, and film roughness are factors which influence the stress build-up in a film. For a thin film the island shapes change the stress distribution and thereby the average stress in the film; smaller grains exhibit higher stresses, whereas bigger grains produce lower stress in the film.

The stress behavior during W growth on a scalloped structure and on a full plate sample was as well analyzed (cf. Fig. 20). The results demonstrated that the substrate shape influences the stress in thin films. Due to the curved substrate the thickness necessary to reach a homogeneous film increases leading to a small intrinsic stress generation for very thin films. During the film growth, the height h_s and width w_s of the scallops influence the contact areas between grains and consequently the generated tensile stress.

We have identified a new phase in the stress evolution during film thickening on scalloped surfaces. The first phase indicates thin film growth at the stage before the overtaking of grains, while the second phase occurs after grain overtaking and is similar to the traditional V-W thickening during deposition on flat surfaces. This information can be used during deep reactive ion etching for TSV fabrication. By controlling the etching parameters, the appropriate scallop size necessary to minimize mechanical failure can be achieved. Scallops having a larger height/width ratio induce small intrinsic stress generation.

Deposition on scallops having the largest simulated height/width ratio (h_s=0.3μm/w_s=0.75μm) produce ~70% less film stress compared to a full plate sample. On the other hand, films grown on scallops having the smallest hight/width ratio (h_s=0.1μm/w_s=1.25μm) produce ~20% less stress compared to a full plate sample (cf. Fig. 20). Scallops influence the stress evolution between the coalescence process and the overtaking of grains, but as the film becomes homogeneous and continues to thicken, the scallop geometry cedes its impact on the stress evolution.
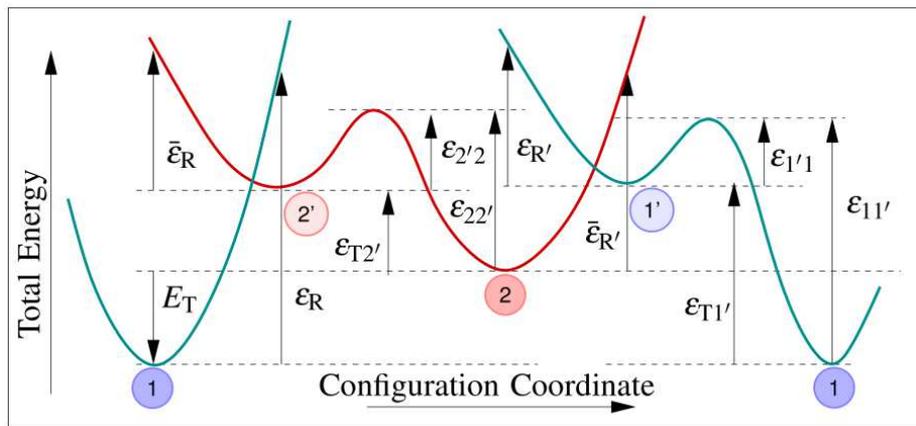
4.4 Extending the NBTI model to include volatility

As discussed in the previous reports, our model for NBTI (see Fig. 21) is based on potential energy surfaces for a defect in its neutral (blue lines) and positive (red lines) charge state [28]. The minima of the potential energy surfaces correspond to the stable and metastable states of the defect structure. The defect can exist in two different structural states, where each again can be either neutral or positively charged. The charged states affect the device characteristics of the MOS transistor, the neutral states are invisible to electrical measurements. Even though each state of the model is related to a specific atomic configuration of a defect, the model itself can be formulated in an 'agnostic' fashion so that it is suitable for different defect candidates.

In Fig. 22 the defect candidates analyzed are shown. As already mentioned in the previous report, the Oxygen Vacancy (OV) defect is not able to satisfactorily explain the NBTI behavior seen in experiments. RTN and TDDS analysis have provided a deep insight into the trapping dynamics of oxide defects. However, one additional feature that is observed during these measurements has not yet been addressed in detail. Namely the *volatility* that is repeatedly observed in the measurements.

4.4.1 Defect volatility

Defects have been found to frequently dis- and re-appear in the measurements (see Fig. 23), and can sometimes even disappear completely from our observation window [30, 31]. This so called *volatility* is not a rare event, but can potentially occur for a majority of the defects, particularly when electrons are injected into the oxide. A consistent model of oxide defects must therefore not only describe their behavior when electrically active, but also allow for them to dis- and re-appear during measurement cycles. In our TDDS measurements we
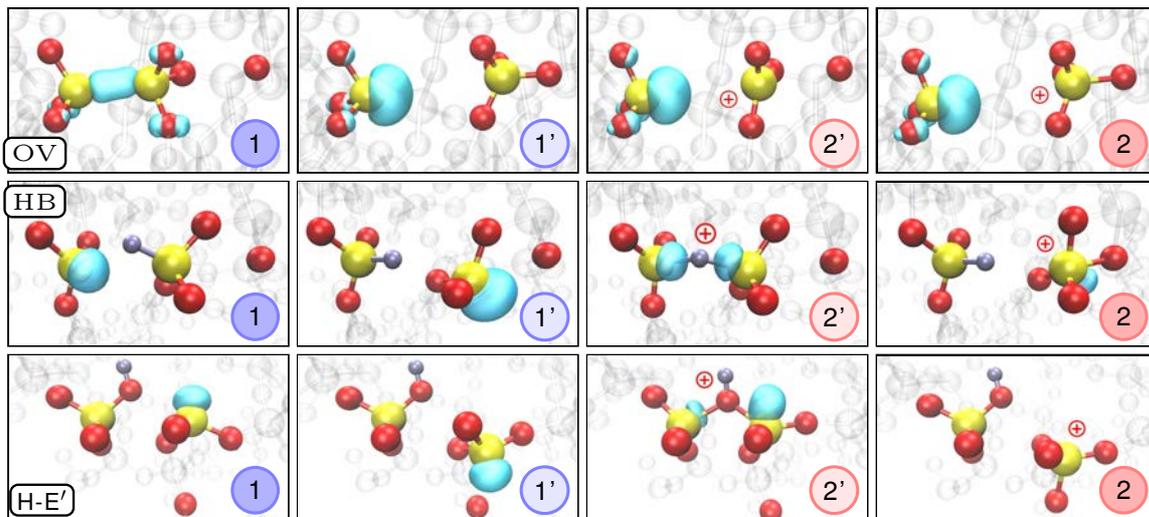
Figure 22

Atomic configurations corresponding to states 1, 1', 2' and 2 for the oxygen vacancy (OV, top) hydrogen bridge (HB, middle) and the hydroxyl-E' center (H-E', bottom). H atoms are shown as silver, Si atoms - yellow and O atoms - red. The turquoise bubble represent the localized highest occupied orbitals for the neutral charge states and the lowest unoccupied orbital for the positive charge states. Upon hole capture the defect can go into state 2' and the Si atoms move closer together in all the defects. Depending on the gate bias, the defect either goes back to state 1 or, eventually into the positive state 2 or the neutral state 1', where the right Si has moved through the plane of its three O neighbors, forming a puckered configuration by bonding to a neighboring O in the right.

observe time constants for defect signals disappearing in the volatile state, τv, typically in the range of hours to weeks. The upper limit is clearly limited by the measurement time. The lower limit has not yet been rigorously tested. We speculate that a τv as low as one second could well be detected for a defect normally capturing and emitting in the microsecond regime. However, up to now the lowest observed τv has been 20 minutes. Assuming that the dynamics are determined by a thermally activated rearrangement of the atomic structure, we are again dealing with a two-state process (active/inactive). Similar to RTN and 1/f noise we can estimate the corresponding reaction barrier with an Arrhenius law [25, 52, 59]:

$$\frac{1}{\tau v} = \nu \cdot e^{\frac{E_B}{k_B T}} \tag{24}$$

Assuming an attempt frequency of $\nu = 10^{13} s^{-1}$ [26, 27], the corresponding rearrangement barrier height E_B at room temperature should be about 1.0 eV. This value only increases to about 1.2 eV for a τv of one month. Of course, higher barriers can be overcome when measuring at higher temperatures and for longer times.

As was shown in the previous report, both the HB and hydroxyl-E$'$ centers exhibit the bi-stability and the trap level positions favorable for RTN and NBTI observed in Si MOSFETs. Since both of them contain a hydrogen atom and several publications have shown that hydrogen can be released during electrical stress [9, 14, 8, 1, 54, 49], we investigated whether the dynamics of the hydrogen atom could be a possible cause of volatility. For example, the presence of the hydrogen atom in the HB moves its level into a more favorable position for hole trapping with respect to the OV. Thus losing hydrogen could take the defect out of the TDDS measurement window. This H relocation corresponds to either a neutral hydrogen atom moving away from the neutral defect state or a proton from the positive defect state.

4.4.2 Hydrogen bridge

To describe the disappearance of the hydrogen containing defects in the measurements, the hydrogen has to move away from the defect to form a configuration which we refer to as precursor configuration. Our calculations show that this barrier is on average 2.6 eV with $\sigma = 0.67$ eV, which is still too high to explain the majority of the data. We therefore conclude
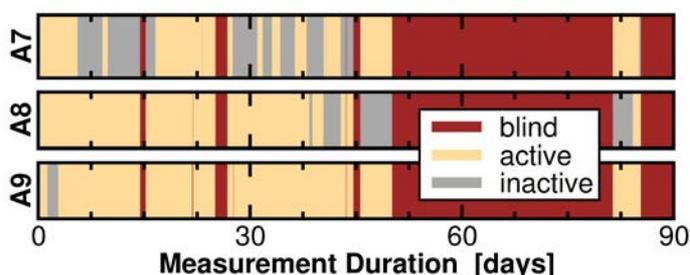
Figure 23

TDDS measurements for three selected defects which were monitored over three months. The plots show when the defect is electrically active or inactive (volatile). Occasionally, the experimental conditions did not allow for an observation ("blind" phases), for instance during a long high-temperature bake around the beginning of the third month.
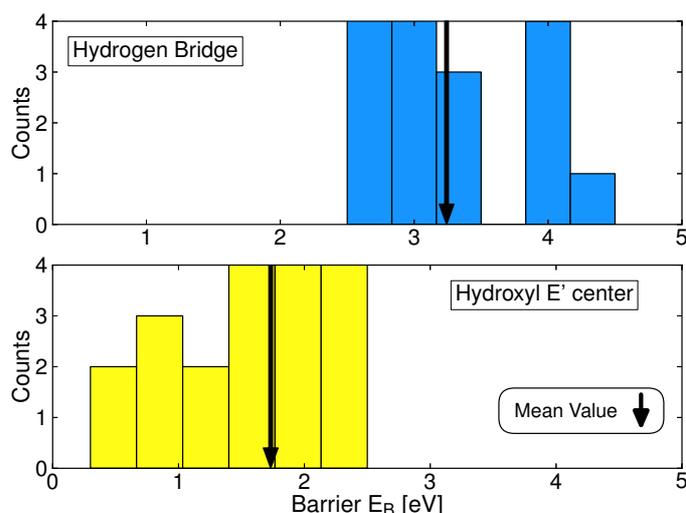
that the characteristics of the HB in its neutral charge state are unlikely to change as a result of hydrogen dynamics in such a way as to explain defect volatility [83].

From the positively charged HB, a proton can be released by displacing away from the vacancy to bind to the next available neighboring oxygen, similar to the proton hopping described in the work of Karna *et al.* [39] and Blöchl [4]. This proton movement to the neighboring oxygen atom yields a new configuration which we call 0^+ in its positively charged state. Our NEB calculations on selected transitions for the HB yield reaction barriers with a minimum of 2.54 eV. These values are much too high to explain the volatility of the defects (see Fig. 24 top for the barrier value distribution). Thus in both charge states of the HB the calculated barriers are too high to explain the volatility seen in experiments [83].

4.4.3 Hydroxyl-E' center

In previous work [18] we have shown that the mean barrier for dissociation of the neutral hydroxyl-E' center and formation of an interstitial H atom is 1.66 eV with $\sigma = 0.37$ eV. This is already much lower than for the HB, but still slightly too high for this reaction to satisfactorily explain volatility.

Proton relocation to a neighboring oxygen atom

The second possible reaction would again be the relocation of the proton in the positively charged configurations 2 and 2' onto a neighboring bridging oxygen atom. For this reaction calculations [84] demonstrated that the reaction barriers involving positively charged states (Fig. 25 top) are considerably lower than for the neutral case. We will therefore focus on this proton relocation.

The NEB calculations performed for the positively charged hydroxyl-E' center clearly showed that the reaction $2' \to 0^+$ is always preferred over $2 \to 0^+$ [84]. Even though the mean value

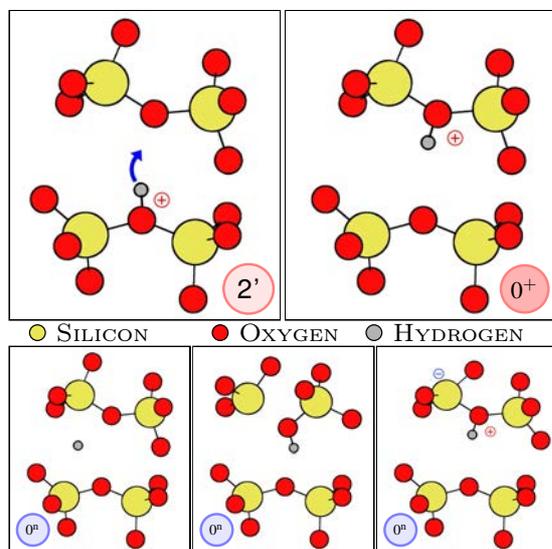of these transition barrier still lies quite high (1.73 eV), much lower barriers, in the range of 1.0 eV and smaller, were found for the transition $2' \to 0^+$ for the hydroxyl-E' (see Fig. 24 bottom). We should note that the states $2'$ and 0^+ of the hydroxyl-E' are nearly isoenergetic, with 20% even being lower in state 0^+ [84]. This means that the reverse reaction barriers (and time constants) $0^+ \to 2'$ back to defect activity would be in the same range as the forward reaction $2' \to 0^+$. This is in agreement with TDDS measurements [29], making the hydroxyl-E' center a plausible candidate for explaining volatility effects. An extended model of possible transitions between different defect states is schematically depicted in Fig. 26. Based on the results discussed above, we assume that the transition into the inactive state is $2' \to 0^+$. This figure is an extension of Fig. 21 including volatility. Similar to Fig. 21, the transitions involving charge transfer are considered in the NMP model. The transitions between states of the same charge are again assumed to be purely thermally activated as well as the volatility transition $2' \to 0^+$. The applied voltage moves the neutral (blue) and positive (red) parabolas relative to each other, thereby changing the barriers for the NMP transitions.

It has been shown in [83] that, due to their properties not all of these defects would be visible or identifiable in RTN or TDDS measurements. Overall the hydroxyl-E' center is a good candidate to explain not only the electrically active branch but also the volatility effect. Furthermore, as discussed above, we also found that there are defects that eventually could release their hydrogen atom. This could be a possible mechanism to explain the complete disappearance of defects in our measurements. It also provides a possible link to hydrogen release during electrical stress [32, 9, 14, 8, 1, 54, 49].
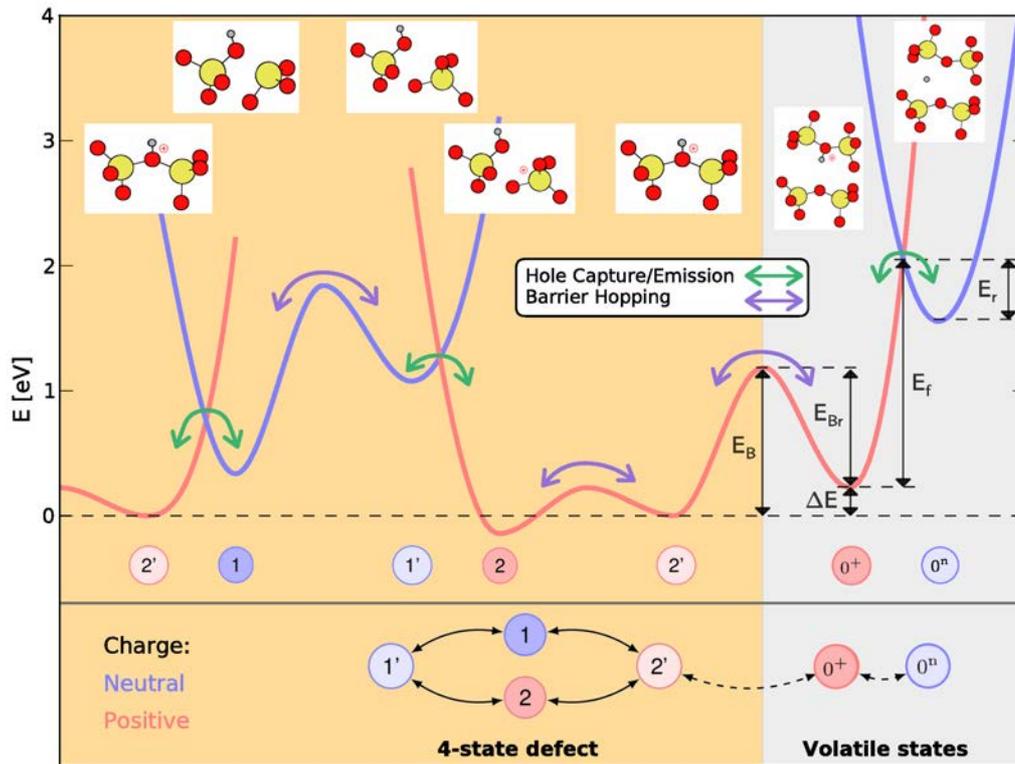
Figure 26

Example of a potential energy surface of a hydroxyl-E′ center defect along the reaction coordinates between different states. Possible transitions can occur by charge capture or emission (green arrows) or barrier hopping (purple arrows). The defect is electrically active when on the left side of the plot (orange). When it overcomes the barrier $2' \rightarrow 0^+$ it is electrically-inactive (grey) and therefore in general not visible in the measurements (given certain conditions for the barrier between the states 0^+ and 0^n as described in the text). Depending on the applied gate bias, the parabolas of the neutral states (blue) will be shifted up or down along the energy axis, thereby changing the barriers and time constants for charge-trapping and emission. Note that in this extended model there are now three possibilities to leave state $2'$ (to 1, 2 or 0^+).

4.5 Hot-carrier degradation modeling in high-voltage devices

Modeling of hot-carrier degradation (HCD) becomes even more complicated in the case of LDMOS transistors. This is because proper treatment of carrier transport becomes challenging due to the large device dimensions, high operating voltages and such architectural peculiarities as the bird's beak and the non-planar interface, see Fig. 27. Furthermore, we have shown recently [2, 79, 72, 73, 76, 75, 74, 74, 78, 77, 65] that both the single- and multiple-carrier mechanisms of bond dissociation can provide substantial contributions to HCD even in long-channel transistors. On other words, the multiple-carrier bond-breakage process appears to be a crucial component for HCD in nMOSFETs with gate lengths as long as 2μm and stressed at high voltages. Thus, both components need to be considered in a comprehensive HCD model.
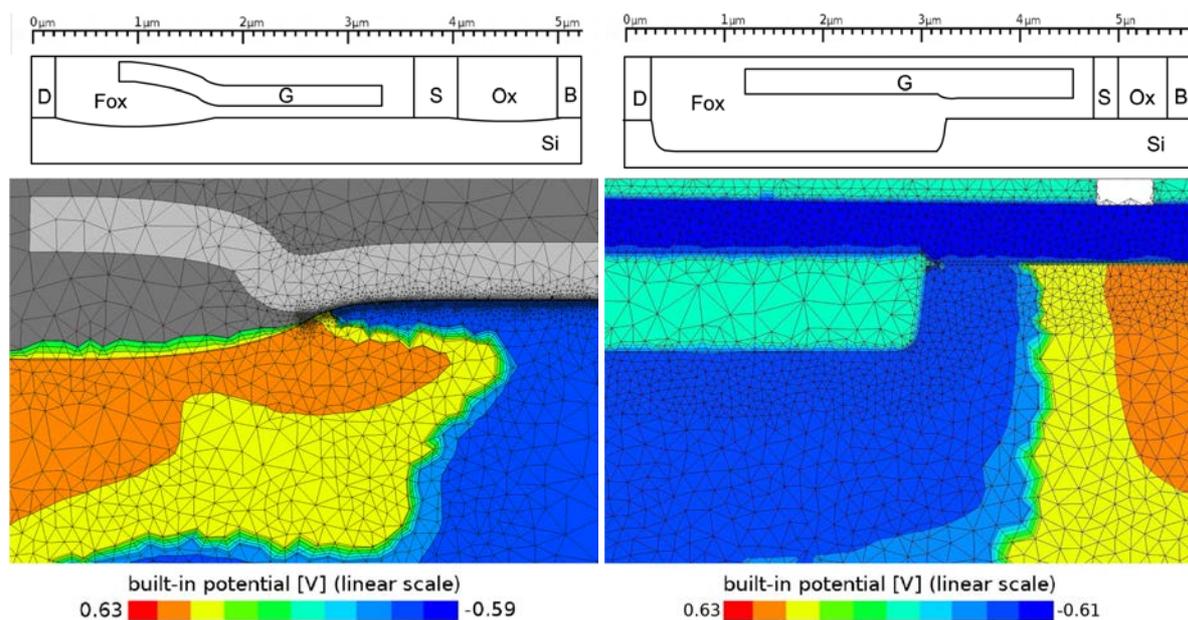
Figure 27

Upper panel: sketch of the n-LDMOS and p-LDMOS transistors with all the segments marked: D - drain, S - source, Ox - oxide, Fox - field oxide, G - gate, B - bulk contact. Lower panel: the adaptive mesh for a near interface device section with the built-in potential represented by the color map.

Therefore, some HCD models try avoid a thorough BTE solution and substitute the information about the DF by some empirical factors which are connected to device characteristics such as the drain current. In this context, an attractive idea would be to use simplified approaches to the Boltzmann transport equation solution such as the drift-diffusion (DD) or the energy transport schemes. As we have shown [65], these schemes are not applicable to model HCD in planar CMOS nMOSFETs with short gate lengths. However, they can be useful for the case of LDMOS transistors which typically have quite long channel and drift regions and are operated at high voltages. In the case of HCD in high-voltage devices we present and verify two versions of out physics-based model [65, 37, 71, 85, 66, 67, 64, 68, 69]: the first is

based on the precise BTE solution obtained with ViennaSHE, while the second one employs the simplified drift-diffusion scheme. Both versions are calibrated in order to represent HCD in LDMOS devices. We perform a thorough check of these two versions step by step and compare their results in terms of carrier DFs, interface state density profiles, and degradation traces.

We used n- and p-LDMOS transistors (sketched in Fig. 27) fabricated on standard 0.35 and $0.18\mu m$ processes with maximum operating drain voltages of 20 and $-50V$. The n-channel devices have a Si/SiO$_2$ interface length of $\sim 3.4\mu$m, and a gate length of $\sim 2.5\mu$m, while the p-channel devices have an interface length of $\sim 4.4\mu$m, and a gate length of $\sim 3.3\mu$m. The n-LDMOS devices were subjected to hot-carrier stress at different combinations of gate and drain voltages V_{gs} and V_{ds}. We used V_{ds} values of 18, 20, and $22V$, while V_{gs} was set to be 1.2, 1.5, and 2.0V. The devices were stressed for $1Ms$ at room temperature. The p-channel devices have been stressed at $V_{ds} = -50$V, $V_{gs} = -1.5$V and $V_{ds} = -50$V, $V_{gs} = -1.7$V for $\sim 40ks$. All measurements were performed at room temperature. To assess HCD, the normalized changes in the linear drain current $\Delta I_{d,lin}$ and the saturation drain current $\Delta I_{d,sat}$ and of the threshold voltage V_t were recorded as a function of stress time.
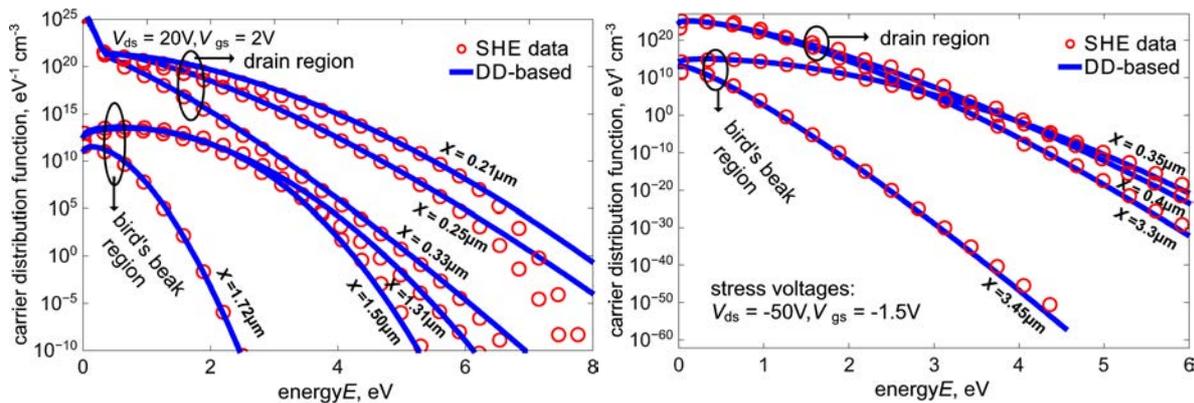
Figure 28

The distribution functions for minority carriers simulated for the n-LDMOS (for $V_{ds} = 20V$ and $V_{gs} = 2V$) and p-LDMOS ($V_{ds} = -50V$, $V_{gs} = -1.5V$) devices using the solution of the Boltzmann transport equation with ViennaSHE and the DD-based model. The DFs are shown for different values of the lateral coordinate related to the drain and bird's beak/STI corner positions.

The SHE-based version of our model employs the full solution of the Boltzmann transport equation using ViennaSHE. The second and more compact version of our HCD model is based on the drift-diffusion scheme. In the latter version the electric field profile $F(x)$, carrier mobility $\mu(x)$, and carrier concentration $n(x)$ are obtained from the DD simulations. Then the carrier temperature is estimated:

$$T_n = T_L + \frac{2}{3}\frac{q}{k_B}\tau\mu F^2 \tag{25}$$

where this q is the carrier charge, TL the lattice temperature, and τ the energy relaxation time, and k_B the Boltzmann constant. Then the carrier DF is calculated according to this

expression:

$$f(E) = A\exp\left[-\left(\frac{E}{E_{\text{ref}}}\right)^b\right] + C\exp\left[-\frac{E}{k_B T_L}\right]. \tag{26}$$

This formula for the DF considers the contribution of both the hot and the cold carriers. The parameters A, C, and E_{ref} are found using the moments of the Boltzmann transport equation, i.e. the carrier concentration, carrier temperature, and the DF normalization:

$$\int_0^\infty f(E)g(E)dE = n; \tag{27}$$

$$\int_0^\infty E f(E)g(E)dE = \frac{3}{2}nk_B T_n; \tag{28}$$

$$\int_0^\infty f(E)dE = 1. \tag{29}$$

The parameter b is assigned a constant value of 1 near the drain and source regions and 2 otherwise.

The DFs for minority carriers in the n- and p-LDMOS devices evaluated with the SHE method and with the DD-based analytical model are summarized in Fig.28. The exemplary DFs given in Fig. 28 are calculated for $V_{\text{ds}} = 20\text{V}$ and $V_{\text{gs}} = 2\text{V}$ (n-LDMOS transistor) and $V_{\text{ds}} = -50\text{V}$, $V_{\text{gs}} = -1.5\text{V}$ (p-LDMOS device) and plotted for different values of the lateral coordinate x, which correspond to the bird's beak in the n-LDMOS, the STI corner in the p-LDMOS, and the drain region. One can see that the DFs are severely non-equilibrium in both the devices. Another important pronounced peculiarity is that the drain region of the n-LDMOS device has a high concentration of cold carriers which is not visible for the p-LDMOS. Such a trend is attributed to the difference in the device topology and the operating voltages. The p-LDMOS has been stressed at very high voltages ($V_{\text{ds}} = -50\text{V}$) as compared to the n-LDMOS ($V_{\text{gs}} = -1.5\text{V}$). One can see that the agreement between the DFs simulated with ViennaSHE and those obtained with the analytic model is very good for both types of carriers in all device regions.
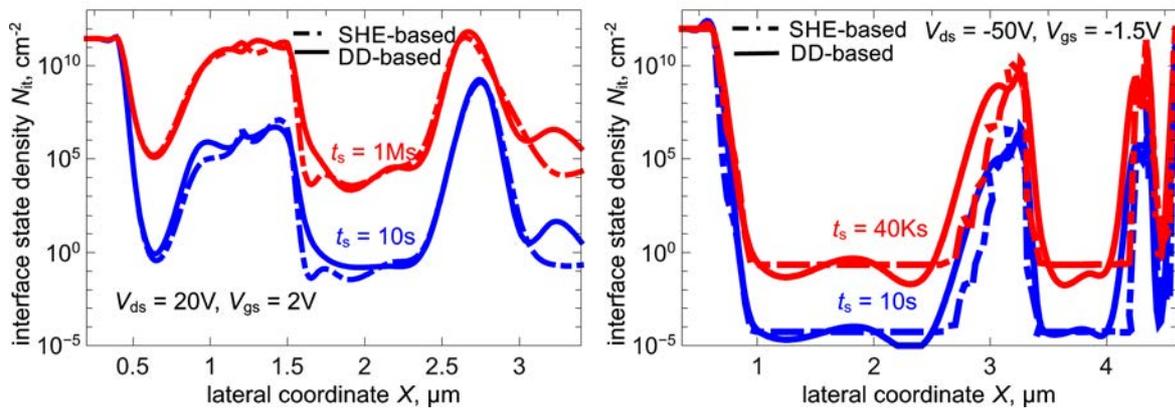
Figure 29

The interface trap density profiles evaluated with the SHE- and DD-based version of our HCD model for the n-LDMOS (stress time steps are 10s and 1Ms) and p-LDMOS devices (stress times are 10s and 40ks). The stress voltages used are the same as in Fig. 29.
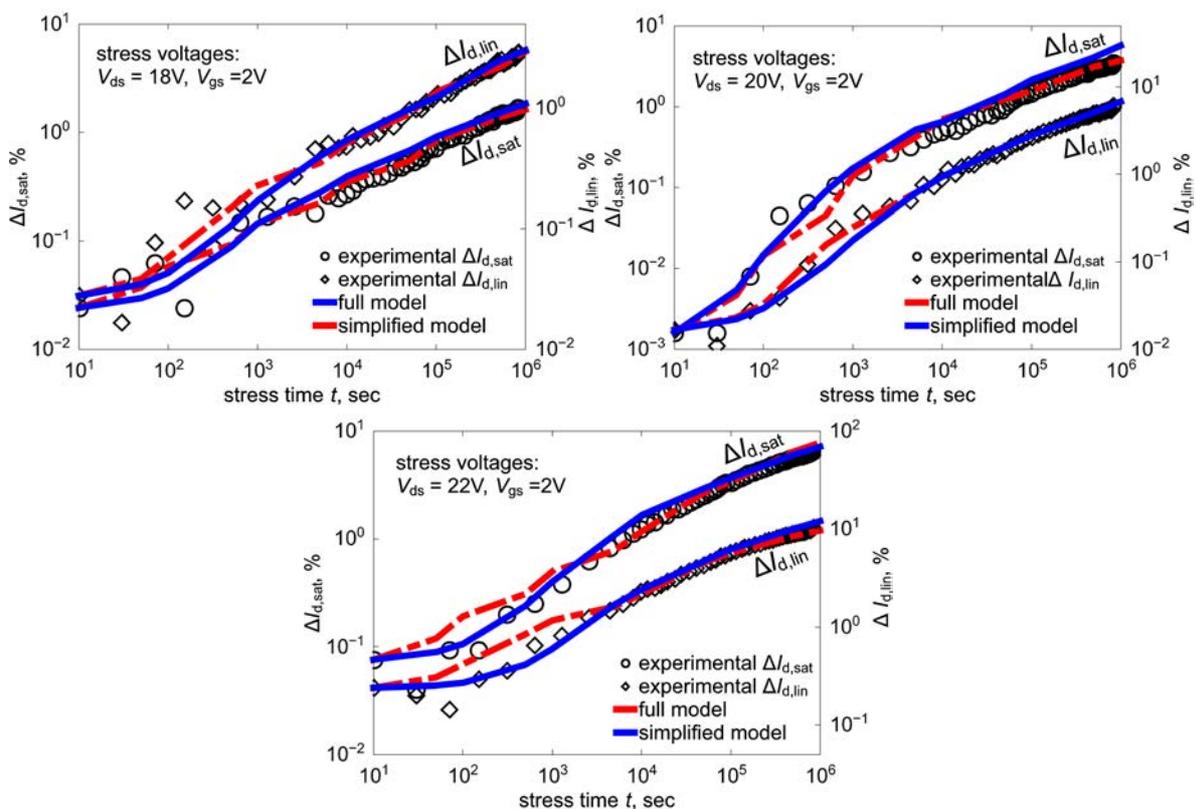
Figure 30

Comparison of the change in the saturation and linear drain currents in the n-LDMOS device obtained from experiments and simulations, using the SHE- and DD-based models, for stress voltages $V_{gs} = 2V$ and $V_{ds} = 18, 20,$ and $22V$ using stress times up to 1Ms. Excellent agreement is obtained.

The $N_{\text{it}}(x)$ profiles evaluated with the SHE- and DD-based DFs for the same combinations of stress V_{ds} and V_{gs} as those used in Fig. 28 are shown in Fig. 29. Remarkably for both devices, $N_{\text{it}}(x)$ profiles simulated with different versions of the model are very similar. The peak in $N_{\text{it}}(x)$ profiles at the drain region is attributed to the saturation of both the single- and the multiple-carrier mechanisms. This trend stems from a combination of high energies typical for the near drain device area and high particle concentrations. In the case of the n-LDMOS transistor, the second Nit peak is pronounced near the bird's beak which is the outcome of the interplay between the single-carrier Si-H bond-breakage process and the interaction of the bond dipole moment with the electric field which peaks at this position. The rate of the multiple-carrier process is very low in this region as the concentration of colder carrier is not very high as was seen for the drain region. Similarly, the Nit peak near the STI corner for the p-LDMOS is attributed to the bond breakage by hot carriers in this area. The third peak in the channel of both types of devices is due to the multiple-carrier process and also the interaction of the bond's dipole moment with the electric field because the carrier concentration and the average carrier energy are high in this region of the device.

Figure 32

$\Delta I_{d,sat}(t)$ degradation traces in the case of the p-LDMOS transistor: experiment vs. SHE- and DD-based versions of the model. One can see that agreement between measurements and simulation results is excellent.

Fig. 30 summarizes the experimental change of the linear and saturation drain currents in the n-LDMOS device plotted as a function of stress time for a fixed V_{gs} of 2.0V and varyin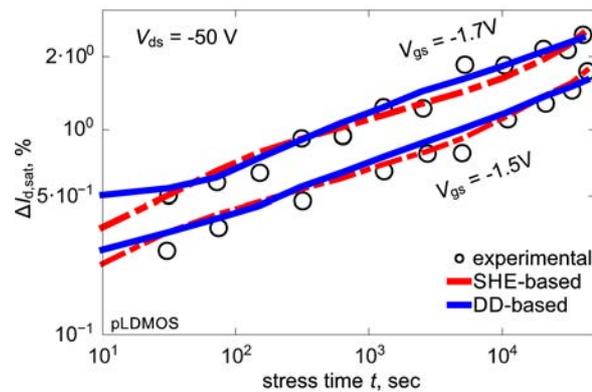g V_{ds} of 18, 20 and 22V. In addition, the simulated data obtained with the SHE- and DD-based versions of our model are shown for comparison. One can see that agreement between experimental and theoretical $\Delta I_{d,lin}(t)$ and $\Delta I_{d,sat}(t)$ degradation traces is very good for both versions of the model. The degradation curves from both our approaches are almost the same within the whole experimental window. Good agreement between experiment and model results is also obtained for the case of the threshold voltage degradation, see Fig.31. One can see that also for ΔV_t data obtained at $V_{gs} = 2V$ and two different values of V_{ds} the model provides excellent agreement. The same is typical also for the p-LDMOS transistor which experimental $\Delta I_{d,sat}(t)$ degradation traces are well represented by both versions of our HCD model (see Fig. 32).

The more computationally expensive variant of the model uses the exact solution of the Boltzmann transport equation, while the simplified version employs the drift-diffusion scheme. Although the first approach is more accurate, the DD-based model can represent the carrier DFs and N_{it} profiles with very good accuracy. The good agreement between experiments and our hot-carrier degradation model which uses the drift-diffusion scheme allows us to conclude that this scheme is suitable for predictive HCD simulations in n-LDMOS transistors.

Conclusion

We have applied our physical HCD model to represent the degradation in an nLDMOS transistor. Two versions of the model have been examined, i.e., a version which employs the carrier DFs obtained from a deterministic BTE solver and one which uses the simpler DD approach. The electron DFs obtained with the DD-based model were compared with those simulated with the SHE approach and good agreement between them was shown. Although some discrepancy between the DFs computed with these two models is visible in the drain region, this discrepancy was shown to not translate into an error in the DD-based

HCD model. Such a conclusion can be drawn based on the good agreement between the carrier AIs evaluated with the two versions of the model for both single- and multiple-carrier processes of Si-H bond dissociation [68]. The corresponding interface state density profiles are also almost identical for a wide range of stress times and stress conditions. The changes of the linear and saturation drain currents and the threshold voltage shift were represented by both versions of our model for different combinations of drain and gate voltages using a unique set of parameters. Good agreement between the results obtained with SHE- and DD-based versions of the model suggests that the efficient DD model is well suited for describing HCD in nLDMOS devices.

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5 Publications

5.1 Master and Doctoral Theses

Wolfhard H. Zisser, *"Electromigration in Interconnect Structures"*. PhD Thesis, TU Wien, Institute for Microelectronics, June 2016.

Marco Rovitto, *"Electromigration Reliability Issue in Interconnects for Three-Dimensional Integration Technologies"*. PhD Thesis, TU Wien, Institute for Microelectronics, December 2016.

Santo Papaleo, *"Mechanical Reliability of Open Through Silicon Via Structures for Integrated Circuits"*. PhD Thesis, TU Wien, Institute for Microelectronics, December 2016.

5.2 Publications with Peer Review

5.2.1 Journal Papers

S. Papaleo, W. H. Zisser, A. P. Singulani, H. Ceric, and S. Selberherr. *"Stress Evolution During Nanoindentation in Open TSVs,"* IEEE Transactions on Device and Materials Reliability, 56, pp. 470 - 474 (2016).

P. Sharma, S. E. Tyaginov, M. Jech, Y. Wimmer, F. Rudolf, H. Enichlmair, J. M. Park, H. Ceric, and T. Grasser. *"The Role of Cold Carriers and the Multiple-Carrier Process of Si-H Bond Dissociation for Hot-Carrier Degradation in n- and p-channel LDMOS Devices,"* Solid-State Electronics, 115, pp. 185 - 191, (2016).

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H. Ceric, R. Lacerda de Orio, W. H. Zisser, S. Selberherr. *"Microstructural Impact on Electromigration: A TCAD Study,"* Facta universitatis - series: Electronics and Energetics, 27, pp. 1 - 11, (2014).

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5.2.2 Conference Papers

S. Papaleo, M. Rovitto, and H. Ceric. *"Mechanical Effects of the Volmer-Weber Growth in the TSV Sidewall,"* in Proceedings of IEEE Electronic Components and Technology Conference (ECTC), pp. 1617 - 1622, (2016).

M. Rovitto and H. Ceric. *"Electromigration Induced Voiding and Resistance Change in Three-Dimensional Copper Through Silicon Vias,"* in Proceedings of IEEE Electronic Components and Technology Conference (ECTC), pp. 550 - 556, (2016).

H. Ceric, R. Lacerda de Orio, and M. Rovitto. *"TCAD Approach for the Assessment of Interconnect Reliability,"* in Abstracts of 14th International Conference Reliability and Stress-Related Phenomena in Nanoelectronics - Experiment and Simulation (IRSP), p. 21 (2016).

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