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Introduction

In its last official year the Christian Doppler Laboratory for Technology CAD in Microelectronics has completely focused on the most prominent reliability issues in modern MOS transistors, namely the negative Bias Temperature Instability (NBTI) and Hot Carrier Degradation (HCD). NBTI, being the central topic of research, was shown to be very well explainable by a model based on electrochemical reactions involving oxide defects with distributed reaction rates, in contrast to the usual reaction-diffusion description. This new point of view links NBTI to other defect-related effects in oxides, such as Hot-Carrier (HC) degradation and flicker noise. In cooperation with our industrial partners it was possible to obtain new and exciting experimental input from a study of small-scale transistors. These efforts led to a new characterization technique for these devices, as will be laid out in the following section. The observed behavior and the exploration of the physical foundation of our new model has moved the physical details of electron transfer in solid-state materials into the focus of our attention and aided our effort to gain insight by the atomistic modeling of defects at the semiconductor-oxide interface.

Time dependent defect spectroscopy

Trap sites in the gate dielectrics of MOSFETs play a crucial role in a number of effects unrelated to each other at the first sight. By assuming a suitable energetic and spatial distribution of trap sites, a model for excess noise in the drain current of MOSFETs was presented in 1957. More recently, oxide traps were found to be involved in reliability issues such as the Negative Bias Temperature Instability (NBTI). While in large-area transistors the drain current excess noise takes the ubiquitous $1/f$ spectral shape, which consists of a superposition of Lorentzian spectra due to individual defects, visible in small-area devices. Similarly, NBTI degradation and -recovery appear to be continuous processes on large-area devices, while on small-area transistors, which contain just a handful of traps, discrete levels can be observed in the recovering drain current. In steady-state, these levels and the abrupt transitions between them are commonly referred to as Random Telegraph Noise (RTN). With NBTI degradation and recovery, although the device is in pronounced non-equilibrium then, similar transitions between discrete levels can be observed. The study of these discrete relaxation curves has led to the development of a sophisticated method termed time dependent defect spectroscopy (TDDS): by carrying out a number of carefully designed stress/relaxation experiments, it is possible to extract the statistical parameters of the individual traps present in the transistor, provided that the latter is small enough such that the drain current steps can be assigned unambiguously to distinct traps. This is aided by the non-uniform drain current distribution in the channel of a real MOSFET, causing individual traps to cause distinctive drain current steps. Binning of the emission times and step amplitudes into a two-dimensional histogram - called a spectral map - reveals marked clusters of events. Since the underlying physical process is approximately Poissonian, the temporal probability distribution of events is exponential. A computer code was developed for the extraction of steps and the generation of the spectral map from the huge amount of measurement data.

Justification for the method was found in the fact that under variation of the stress time it shows that the clusters do not move within the spectral map, i.e. step amplitude and emission time are independent of stress time, ruling out e.g. diffusive processes. Furthermore, the amplitude of the probability distribution of a particular trap increases with stress time, consistent with the picture that for a trap to show an emission event it has to capture a carrier within the preceding stress phase, which becomes more probable when this stress phase is longer. From a set of experiments with different stress times and the resulting probability amplitudes it is therefore possible to extract the capture time constants of the traps. Repeating this block of experiments at different temperatures and/or different stress voltages and/or different relaxation voltages, the investigation of the dependencies of the emission- and capture times on these parameters becomes possible.

Together with Infineon Technologies state-of-the-art production quality pMOSFETs were examined using TDDS. We were able to extract capture- and emission time constants for several distinct defects and to study their dependence on variation of the temperature, and stress and recovery gate voltage. These results are the foundation of our current NBTI modeling efforts.

Improvement of the two-stage model for NBTI

The two-stage model (TSM) for NBTI, which we introduced in early 2009, was able to explain a broad range of experimental findings that were not explainable using established theories. The aforementioned experiments as well as our attempts to extract relevant parameters for the TSM from atomistic calculations moved the detailed dynamics of electron capture and release into the focus of our interest.

Electron transfer processes are of enormous importance in many fields of chemistry and have been receiving a lot of attention starting from the first half of the 20th century on. An intense study of the available literature was done to shed light on the physical processes involved in the tunneling of electrons to and from localized states as is the case in MOS transistor degradation. It shows that the thermal movement of the lattice has to be properly taken into consideration leading to a complex dependence of the capture and release rates on temperature and the electric field in the oxide. A broad spectrum of models for electron transfer is available in literature, ranging from formulations based on classical statistical mechanics (Marcus theory) to quantum theory based descriptions, based on overlaps of vibrational wave-functions (Huang-Rhys model).

While the fundamental assumptions employed in the TSM appear to be basically correct, the rate equations were formulated in an ad hoc manner and the metastable charged state of the defect's primary configuration was neglected. This state, being a natural part in our atomistic calculations, was shown to be necessary in order to fully capture the non-linearity in the experimental data. A further improvement of the old model concerns the rather approximately treated field dependence of the capture rates. These terms were replaced by a more rigorous formulation using semiclassical nonradiative multiphonon theory. A simulation of our model using the stochastic simulation algorithm (SSA) has made the comparison to experimental data obtained from TDDS measurements possible. It showed that in this new formulation, defects showing a variety of different behavior ranging from temporary RTN defects to those without observable switching-trap behavior can be explained within the same model.

Quantum chemistry calculation of oxide-defects

The basic parameters required for a proper description of electron transfer are hardly accessible by experiments and have to be extracted from atomistic calculations including the electronic structure, such as DFT or quantum chemistry methods. State-of-the-art DFT-based electronic structure calculation methods such as SP-KKR, LAPW, and numerical-local orbital based DFT have been evaluated for the application to defect calculations.

Due to the high purity of oxides in modern semiconductor technology, the expected defects are self-defects of the materials or impurities of species that are part of the processing. As a promising defect candidate, hydrogen bridges in an amorphous silica lattice have been intensively studied using the embedded cluster method. In this approach, large (nanometer sized) atomic structures are separated into one part treated quantum-mechanically (using DFT) and one described by classical empirical potentials. The calculations were executed using the GUESS code, developed at the University College London by the group of Prof. Alex Shluger. First results support the view of the hydrogen bridge as a useful candidate for NBTI, but the analysis of the data is still in progress.

The beneficial role of nitrogen as a blocking barrier against impurity penetration has initially driven the interest in nitrogen incorporation into dielectrics. Besides this, nitrogen reduces

the leakage current since its larger dielectric constant allows for physically thicker oxides and thus prolongs the lifetime of silicon dioxide-based dielectrics. On the other hand side, NBTI has been reported to be dramatically pronounced at the incorporation of nitrogen.

In the search for a defect that could be activated during NBT stress, a promising nitrogen-related complex (NRC) has been encountered. It consists of an oxygen vacancy in combination with a nitrogen atom situated suitably to stabilize the secondary (puckered) state of the vacancy. The hole capture levels of the neutral variant of the NRC is situated far below the substrate bandgap so that no appreciable amount of charge can be injected into the dielectric this way. However, there exist hole capture levels in the negative charge state which are located in a region close to the substrate bandgap. Furthermore, their stable configurations differ by only a small amount of energy, allowing thermal transitions over the separating barriers within experimental times. For this reason, the NRC can be viewed as another promising candidate that might play a part in NBTI. A calculation of its ESR signal will aid the identification of the NRC in real dielectrics.

Modeling of Hot-Carrier Degradation

The understanding and modeling of Hot Carrier (HC) degradation is not only one of the most crucial reliability issues of field effect transistors besides NBTI, it is also even more challenging, requiring the movement of carriers in the channel to be properly taken into account. The essential properties of HC damage are a strong localization and the less pronounced temperature activation compared to NBTI. The degradation of the device characteristics during stress is strongly dependent on the spatial location of the damage which, in turn, is determined by the device architecture. Interestingly, the HC degradation occurs even for extremely scaled devices where carriers in the channel cannot be treated as “hot” because they do not gain sufficiently high energy. It is therefore assumed that in this case the degradation is triggered by multi-particle processes, while the degradation of long devices is dominated by single-carrier mechanisms.

At the core of the physical model for HC degradation is the carrier acceleration integral which accounts for carriers of all possible energies weighted with the cross-section of the process times the probability of finding particles in the energy range. The distribution of particles over energy, the energy distribution function (DF), is obtained considering the device architecture and given stress conditions from a full-band Monte-Carlo device simulator which solves the Boltzmann transport equation considering electron-phonon and electron-electron scattering. Using this approach we analyzed two types of devices, namely a long channel low-voltage n-MOSFET of standard topology and a high-voltage p-LDMOS. We have shown that in both cases the HC degradation is dominated by the single-electron process. However, the multi-particle contribution – although being small – is still pronounced and important. The worst-case conditions for HC stressing have been analyzed as well. Our simulations compare well with experiment, showing that for n-channel transistors worst-case conditions are encountered at $V_{gs}=(0.4-0.5)V_{ds}$ while for p-channel devices at $V_{gs}=V_{ds}$.

Publications

Contributions to Books

- [B8] O. Triebel and T. Grasser, “Numerical Power/HV Device Modeling,” in *Power/HV MOS Devices Compact Modeling*, pp. 1–32. Springer, 2010, (invited).
- [B7] W. Goes, F. Schanovsky, Ph. Hehenberger, P.J. Wagner, and T. Grasser, “Charge Trapping and the Negative Bias Temperature Instability,” pp. 565–589. ECS Transactions, 2010, (invited).
- [B6] T. Grasser, W. Goes, and B. Kaczer, “Critical Modeling Issues in Negative Bias Temperature Instability,” pp. 265–287. ECS Transactions, 2009, (invited).
- [B5] T. Grasser, W. Goes, and B. Kaczer, “Towards Engineering Modeling of Negative Bias Temperature Instability,” in *Defects in Microelectronic Materials and Devices*, D. Fleetwood, R. Schrimpf, and S. Pantelides, Eds., pp. 399–436. Taylor and Francis/CRC Press, 2008, (invited).
- [B4] B. Kaczer, T. Grasser, R. Fernandez, and G. Groeseneken, “Toward Understanding the Wide Distribution of Time Scales in Negative Bias Temperature Instability,” in *Silicon Nitride, Silicon Dioxide, and Emerging Dielectrics 9*, R. Sah, J. Zhang, Y. Kamakura, M. Deen, and J. Yota, Eds., vol. 6, pp. 265–281. ECS Transactions, 2007, (invited).
- [B3] H. Ceric, R. Heinzl, Ch. Hollauer, T. Grasser, and S. Selberherr, “Microstructure and Stress Aspects of Electromigration Modeling,” in *Stress-Induced Phenomena in Metallization*, pp. 262–268. American Institute of Physics, Melville, 2006.
- [B2] T. Grasser, “Closure Relations for Macroscopic Transport Models in Semiconductor Device Simulation,” in *Recent Res. Devel. Applied Phys.*, vol. 7, pp. 423–446. Research Signpost, 2004, (invited).
- [B1] T. Grasser, H. Kosina, and S. Selberherr, “Hot Carrier Effects within Macroscopic Transport Models,” in *Advanced Device Modeling and Simulation*, T. Grasser, Ed., pp. 173–201. World Scientific, Inc., Sept. 2003, (invited).

Contributions to Journals

- [J40] T. Grasser, H. Reisinger, P.-J. Wagner, and B. Kaczer, “The Time Dependent Defect Spectroscopy for the Characterization of Border Traps in Metal-Oxide-Semiconductor Transistors,” *Physical Review B*, vol. 82, no. 24, pp. 245318, 2010.
- [J39] F. Schanovsky, W. Goes, and T. Grasser, “An Advanced Description of Oxide Traps in MOS Transistors and its Relation to DFT,” *J.Comp.Elec.*, vol. 9, no. 3-4, pp. 135–140, 2010, (invited).
- [J38] J.T. Ryan, P.M. Lenahan, T. Grasser, and H. Enichlmair, “Observations of Negative Bias Temperature Instability Defect Generation via On The Fly Electron Spin Resonance,” *Applied Physics Letters*, vol. 96, no. 22, pp. 223509–1–223509–3, 2010.
- [J37] B. Kaczer, Ph. Roussel, T. Grasser, and G. Groeseneken, “Statistics of Multiple Trapped Charges in the Gate Oxide of Deeply Scaled MOSFET Devices-Application to NBTI,” *IEEE Electron Device Letters*, vol. 31, no. 5, pp. 411–413, 2010.
- [J36] Th. Aichinger, M. Nelhiebel, and T. Grasser, “Energetic Distribution of Oxide Traps Created under Negative Bias Temperature Stress and their Relation to Hydrogen,” *Appl.Phys.Lett.*, vol. 96, pp. (133511–1)–(133511–3), 2010.
- [J35] Th. Aichinger, M. Nelhiebel, S. Einspieler, and T. Grasser, “Observing Two Stage Recovery of Gate Oxide Damage Created under Negative Bias Temperature Stress,” *J.Appl.Phys.*, vol. 107, pp. (024508–1)–(024508–8), 2010.
- [J34] Th. Aichinger, M. Nelhiebel, S. Einspieler, and T. Grasser, “In Situ Polyheater – A Reliable Tool for Performing Fast and Defined Temperature Switches on Chip,” *IEEE Trans.Dev.Mat.Rel.*, vol. 10, no. 1, pp. 3–8, 2010.

- [J33] T. Grasser, B. Kaczer, W. Goes, Th. Aichinger, Ph. Hehenberger, and M. Nelhiebel, “Understanding Negative Bias Temperature Instability in the Context of Hole Trapping,” *Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1876–1882, 2009, (invited).
- [J32] T. Grasser and B. Kaczer, “Evidence that Two Tightly Coupled Mechanism are Responsible for Negative Bias Temperature Instability in Oxynitride MOSFETs,” *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1056–1062, 2009.
- [J31] S. Tyaginov, V. Sverdlov, I. Starkov, W. Goes, and T. Grasser, “Impact of O-Si-O Bond Angle Fluctuations on the Si-O Bond-Breakage Rate,” *Microelectronics Reliability*, vol. 49, pp. 998–1002, 2009.
- [J30] H. Reisinger, R.P. Vollertsen, P.J. Wagner, T. Huttner, A. Martin, S. Aresu, W. Gustin, Grasser T., and C. Schlünder, “A Study of NBTI and Short-Term Threshold Hysteresis of Thin Nitrided and Thick Non-Nitrided Oxides,” *IEEE Trans. Dev. Mat. Rel.*, vol. 9, no. 2, pp. 106–114, 2009.
- [J29] B. Kaczer, A. Veloso, Ph.J. Roussel, T. Grasser, and G. Groeseneken, “Investigation of Bias-Temperature Instability in Work-Function-Tuned High-k/Metal-Gate Stacks,” *Journal of Vacuum Science & Technology B*, vol. 27, no. 1, pp. 459–462, 2009.
- [J28] Ph. Hehenberger, P.-J. Wagner, H. Reisinger, and T. Grasser, “On the Temperature and Voltage Dependence of Short-Term Negative Bias Temperature Stress,” *Microelectronics Reliability*, vol. 49, pp. 1013–1017, 2009.
- [J27] Th. Aichinger, M. Nelhiebel, and T. Grasser, “A Combined Study of p- and n-Channel MOS Devices to Investigate the Energetic Distribution of Oxide Traps after NBTI,” *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 3018–3026, 2009.
- [J26] T. Grasser, P.-J. Wagner, Ph. Hehenberger, W. Goes, and B. Kaczer, “A Rigorous Study of Measurement Techniques for Negative Bias Temperature Instability,” *IEEE Trans. Dev. Mat. Rel.*, vol. 8, no. 3, pp. 526–535, 2008.
- [J25] T. Grasser, W. Goes, and B. Kaczer, “Dispersive Transport and Negative Bias Temperature Instability: Boundary Conditions, Initial Conditions, and Transport Models,” *IEEE Trans. Dev. Mat. Rel.*, vol. 8, no. 1, pp. 79–97, 2008, (invited).
- [J24] K. Martens, B. Kaczer, T. Grasser, B. Jaeger, M. Meuris, H.E. Maes, and G. Groeseneken, “Applicability of Charge Pumping on Germanium MOSFETs,” *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1364–1366, 2008.
- [J23] W. Goes, M. Karner, V. Sverdlov, and T. Grasser, “Charging and Discharging of Oxide Defects in Reliability Issues,” *IEEE Trans. Dev. Mat. Rel.*, vol. 8, no. 3, pp. 491–500, 2008.
- [J22] Th. Aichinger, M. Nelhiebel, and T. Grasser, “On the Temperature Dependence of NBTI Recovery,” *Microelectronics Reliability*, vol. 48, no. 3, pp. 1178–1184, 2008.
- [J21] T. Grasser and S. Selberherr, “Modeling the Negative Bias Temperature Instability (Editorial),” *Microelectronics Reliability*, vol. 47, no. 4-5, pp. 839–840, 2007.
- [J20] T. Grasser and S. Selberherr, “Modeling of Negative Bias Temperature Instability,” *Journal of Telecommunications and Information Technology*, vol. 7, no. 2, pp. 92–102, 2007, (invited).
- [J19] O. Triebel and T. Grasser, “Vector Discretization Schemes in Technology CAD Environments,” *ROMJIST*, vol. 10, no. 2, pp. 167–176, 2007.
- [J18] M. Spevak and T. Grasser, “Discretization of Macroscopic Transport Equations on Non-Cartesian Coordinate Systems,” *IEEE Trans. Computer-Aided Design*, vol. 26, no. 8, pp. 1408–1416, 2007.
- [J17] S. Holzer, A. Sheikholeslami, M. Karner, T. Grasser, and S. Selberherr, “Comparison of Deposition Models for a TEOS LPCVD Process,” *Microelectronics Reliability*, vol. 47, no. 4-5, pp. 623–625, 2007.
- [J16] R. Entner, T. Grasser, O. Triebel, H. Enichlmair, and R. Minixhofer, “Negative Bias Temperature Instability Modeling for High-Voltage Oxides at Different Stress Temperatures,” *Microelectronics Reliability*, vol. 47, no. 4-5, pp. 697–699, 2007.
- [J15] J. Cervenka, W. Wessner, E. Al-Ani, T. Grasser, and S. Selberherr, “Generation of Unstructured Meshes for Process and Device Simulation by Means of Partial Differential Equations,” *IEEE Trans. Computer-Aided Design*, vol. 25, no. 10, pp. 2118–2128, 2006.

- [J14] T. Grasser, R. Kosik, C. Jungemann, H. Kosina, and S. Selberherr, “Non-Parabolic Macroscopic Transport Models for Device Simulation Based on Bulk Monte Carlo Data,” *J.Appl.Phys.*, vol. 97, no. 9, pp. 1–12, 2005.
- [J13] T. Grasser, “Non-Parabolic Macroscopic Transport Models for Semiconductor Device Simulation,” *Physica A*, vol. 349, no. 1/2, pp. 221–258, 2005.
- [J12] S. Wagner, T. Grasser, C. Fischer, and S. Selberherr, “An Advanced Equation Assembly Module,” *Engineering with Computers*, vol. 21, no. 2, pp. 151–163, 2005.
- [J11] S.C. Kim, W. Bahng, N.K. Kim, E.D. Kim, T. Ayalew, T. Grasser, and S. Selberherr, “Numerical Simulation and Optimization for 900V 4H-SiC DiMOSFET Fabrication,” *Material Science Forum*, vol. 483-485, pp. 793–796, 2005.
- [J10] T. Ayalew, S.C. Kim, T. Grasser, and S. Selberherr, “Numerical Analysis of SiC Merged PiN Schottky Diodes,” *Material Science Forum*, vol. 483-485, pp. 949–952, 2005.
- [J9] T. Ayalew, T. Grasser, H. Kosina, and S. Selberherr, “Modeling of Lattice Site-Dependent Incomplete Ionization in α -SiC Devices,” *Material Science Forum*, vol. 483-485, pp. 845–848, 2005.
- [J8] T. Grasser, R. Kosik, C. Jungemann, H. Kosina, B. Meinerzhagen, and S. Selberherr, “A Non-Parabolic Six Moments Model for the Simulation of Sub-100 nm Semiconductor Devices,” *J.Comp.Electron.*, vol. 3, no. 3/4, pp. 183–187, 2004.
- [J7] S. Wagner, V. Palankovski, T. Grasser, G. Röhler, and S. Selberherr, “A Direct Extraction Feature for Scattering Parameters of SiGe-HBTs,” *J.Appl.Surface Science*, vol. 224, no. 1-4, pp. 365–369, 2004.
- [J6] J.M. Park, S. Wagner, T. Grasser, and S. Selberherr, “New SOI Lateral Power Devices with Trench Oxide,” *Solid-State Electron.*, vol. 48, no. 6, pp. 1007–1015, 2004.
- [J5] S. Holzer, R. Minixhofer, C. Heitzinger, J. Fellner, T. Grasser, and S. Selberherr, “Extraction of Material Parameters Based on Inverse Modeling of Three-Dimensional Interconnect Fusing Structures,” *Microelectronics Journal*, vol. 35, no. 10, pp. 805–810, 2004.
- [J4] T. Ayalew, A. Gehring, T. Grasser, and S. Selberherr, “Enhancement of Breakdown Voltage for Ni-SiC Schottky Diodes Utilizing Field Plate Edge Termination,” *Microelectronics Reliability*, vol. 44, no. 9-11, pp. 1473–1478, 2004.
- [J3] T. Grasser, H. Kosina, and S. Selberherr, “Hot Carrier Effects within Macroscopic Transport Models,” *Int.J.High Speed Electronics and Systems*, vol. 13, no. 3, pp. 873–901, Sept. 2003, (invited).
- [J2] T. Grasser, T.-w. Tang, H. Kosina, and S. Selberherr, “A Review of Hydrodynamic and Energy-Transport Models for Semiconductor Device Simulation,” *Proc.IEEE*, vol. 91, no. 2, pp. 251–274, 2003.
- [J1] T. Ayalew, A. Gehring, J.M. Park, T. Grasser, and S. Selberherr, “Improving SiC Lateral DMOSFET Reliability under High Field Stress,” *Microelectronics Reliability*, vol. 43, no. 9-11, pp. 1889–1894, 2003.

Contributions to Conferences

- [C145] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, Th. Aichinger, Ph. Hehenberger, P.-J. Wagner, F. Schanovsky, J. Franco, Ph. Roussel, and M. Nelhiebel, “Recent Advances in Understanding the Bias Temperature Instability,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, Dec. 2010, pp. 82–85, (invited).
- [C144] T. Grasser, Th. Aichinger, H. Reisinger, J. Franco, P.-J. Wagner, M. Nelhiebel, C. Ortolland, and B. Kaczer, “On the ‘Permanent’ Component of NBTI,” in *Proc. Intl.Integrated Reliability Workshop*, Oct. 2010.
- [C143] T. Grasser, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, and B. Kaczer, “The Time Dependent Defect Spectroscopy (TDDS) Technique for the Bias Temperature Instability,” in *Proc. Europ.Symp. on Rel.Electr.Dev., Failure Physics and Analysis (ESREF)*, Oct. 2010, (invited, best paper IRPS ’10).

- [C142] T. Grasser, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, and B. Kaczer, “The Time Dependent Defect Spectroscopy (TDDS) Technique for the Bias Temperature Instability,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, May 2010, pp. 16–25, (**best paper award**).
- [C141] T. Grasser, “Transport Modeling in Modern Semiconductor Devices,” in *CoMoN Workshop 2010*, June 2010, (**invited**).
- [C140] T. Grasser, “Recent Developments in Device Reliability Modeling,” in *MOS-AK/ESSDERC Workshop 2010*, Sept. 2010, (**invited**).
- [C139] T. Grasser, “Statistical Reliability in Nanoscale Devices,” in *SISPAD Workshop “Simulation and Characterization of Statistical CMOS Variability and Reliability”*, A. Asenov and G. Baccarani, Eds., Sept. 2010, (**invited**).
- [C138] T. Grasser, “Characterization and Modeling of the Negative Bias Temperature Instability,” in *VDE/VDI GMM Workshop “Reliability of Semiconductor Devices”*, Mar. 2010, (**invited**).
- [C137] S. Tyaginov, I. Starkov, O. Triebel, J. Cervenka, C. Jungemann, S. Carniello, J.M. Park, H. Enichlmair, M. Karner, Ch. Kernstock, E. Seebacher, R. Minixhofer, H. Ceric, and T. Grasser, “Interface Traps Density-of-States as a Vital Component for Hot-Carrier Degradation Modeling,” in *Proc. Europ.Symp. on Rel.Electr.Dev., Failure Physics and Analysis (ESREF)*, 2010, pp. 1267–1272.
- [C136] M. Toledano-Luque, B. Kaczer, Ph.J. Roussel, R. Degraeve, J. Franco, T. Kauerauf, T. Grasser, and G. Groeseneken, “Depth Localization of Trapped Holes in SiON after Positive and Negative Gate Stress,” in *Proc. Semic.Interface Specialists Conference (SISC)*, 2010.
- [C135] M. Toledano-Luque, B. Kaczer, Ph. Roussel, M.J. Cho, T. Grasser, and G. Groeseneken, “Temperature Dependence of the Emission and Capture Times of SiON Individual Traps after Positive Bias Temperature Stress,” in *Proc. Workshop on Dielectrics in Microelectronics*, 2010, pp. 1–2.
- [C134] I. Starkov, S. Tyaginov, H. Enichlmair, O. Triebel, J. Cervenka, C. Jungemann, S. Carniello, J.M. Park, H. Ceric, and T. Grasser, “HC Degradation Model: Interface State Profile-Simulations vs. Experiment,” in *Proc. Workshop on Dielectrics in Microelectronics*, 2010, p. 128.
- [C133] F. Schanovsky, W. Goes, and T. Grasser, “Multi-Phonon Hole-Trapping from First-Principles,” in *Proc. Workshop on Dielectrics in Microelectronics*, 2010, p. 54.
- [C132] F. Schanovsky, W. Goes, and T. Grasser, “Hole Capture into Oxide Defects in MOS Structures from First Principles,” in *Ψ_k - 2010 Conference*, 2010, p. 435.
- [C131] F. Schanovsky, W. Goes, and T. Grasser, “Ab-Initio Calculation of the Vibrational Influence on Hole-Trapping,” in *Proc. Intl.Workshop Comp.Electronics (IWCE)*, 2010, pp. 163–166.
- [C130] J.T. Ryan, P. Lenahan, T. Grasser, and H. Enichlmair, “Recovery-Free Electron Spin Resonance Observations of NBTI Degradation,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2010, pp. 43–49, (**best student paper award**).
- [C129] H. Reisinger, T. Grasser, K. Hofmann, W. Gustin, and C. Schlunder, “The Impact of Recovery on BTI Reliability Assessments,” in *Proc. Intl.Integrated Reliability Workshop*, Oct. 2010.
- [C128] H. Reisinger, T. Grasser, W. Gustin, and C. Schlunder, “The Statistical Analysis of Individual Defects Constituting NBTI and its Implications for Modeling DC- and AC-Stress,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2010, pp. 7–15.
- [C127] G. Pobegen, Th. Aichinger, M. Nelhiebel, and T. Grasser, “Dependence of the Negative Bias Temperature Instability on the Gate Oxide Thickness,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2010, pp. 1073–1077.
- [C126] B. Kaczer, T. Grasser, J. Franco, M. Toledano-Luque, Ph.J. Roussel, and G. Groeseneken, “Recent Trends in Bias Temperature Instability,” in *Proc. Workshop on Dielectrics in Microelectronics*, 2010, p. 55, (**invited**).
- [C125] B. Kaczer, T. Grasser, Ph.J. Roussel, J. Franco, R. Degraeve, L.A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, “Origin of NBTI Variability in Deeply Scaled PFETs,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2010, pp. 26–32.

- [C124] Ph. Hehenberger, H. Reisinger, and T. Grasser, “Recovery of Negative and Positive Bias Temperature Stress in pMOSFETs,” in *Proc. Intl.Integrated Reliability Workshop*, Oct. 2010.
- [C123] W. Goes, F. Schanovsky, Ph. Hehenberger, P.J. Wagner, and T. Grasser, “Charge Trapping and the Negative Bias Temperature Instability,” in *ECS Meeting*, S. Kar, M. Houssa, S. Van Elshocht, D. Landheer, D. Misra, and K. Kita, Eds. Oct. 2010, (invited).
- [C122] J. Franco, B. Kaczer, G. Eneman, J. Mitard, A. Stesmans, V.V. Afanas’ev, T. Kauerauf, Ph. Rousel, M. Toledano-Luque, M. Cho, R. Degraeve, T. Grasser, L.A. Ragnarsson, L. Witters, J. Tseng, S. Takeoka, W.-E. Wang, T.Y. Hoffmann, and G. Groeseneken, “6Å EOT Si_{0.45}Ge_{0.55} pMOSFET with Optimized Reliability ($V_{DD}=1V$): Meeting the NBTI Lifetime Target at Ultra-Thin EOT,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2010, pp. 70–73.
- [C121] J. Franco, B. Kaczer, J. Mitard, G. Eneman, Ph.J. Roussel, F. Crupi, T. Grasser, L. Witters, T.Y. Hoffmann, and G. Groeseneken, “Implications of Channel Hot Carrier Degradation in Si_{0.45}Ge_{0.55} pMOSFETs,” in *Proc. Semic.Interface Specialists Conference (SISC)*, 2010.
- [C120] J. Franco, B. Kaczer, M. Cho, G. Eneman, G. Groeseneken, and T. Grasser, “Improvements of NBTI Reliability in SiGe p-FETs,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2010, pp. 1082–1085.
- [C119] M.F. Bukhori, T. Grasser, B. Kaczer, H. Reisinger, and A. Asenov, “‘Atomistic’ Simulation of RTS Amplitudes Due to Single and Multiple Charged Defect States and Their Interactions,” in *Proc. Intl.Integrated Reliability Workshop*, Oct. 2010.
- [C118] Th. Aichinger, S. Puchner, M. Nelhiebel, T. Grasser, and H. Hutter, “Impact of Hydrogen on Recoverable and Permanent Damage following Negative Bias Temperature Stress,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2010, pp. 1063–1068.
- [C117] T. Grasser, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, and B. Kaczer, “Understanding Negative Bias Temperature Instability in the Context of Hole Trapping,” in *Proc. Insulating Films Semicond. (INFOS)*, June 2009, (invited).
- [C116] T. Grasser, W. Goes, and B. Kaczer, “Critical Modeling Issues in Negative Bias Temperature Instability,” in *ECS Meeting*. May 2009, (invited).
- [C115] T. Grasser, “Physical Mechanisms and Modeling of the Bias Temperature Instability,” in *Proc. Europ.Symp. on Rel.Electr.Dev., Failure Physics and Analysis (ESREF)*, Oct. 2009, (tutorial).
- [C114] T. Grasser, H. Reisinger, W. Goes, Th. Aichinger, Ph. Hehenberger, P.J. Wagner, M. Nelhiebel, J. Franco, and B. Kaczer, “Switching Oxide Traps as the Missing Link between Negative Bias Temperature Instability and Random Telegraph Noise,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2009, pp. 729–732.
- [C113] T. Grasser, B. Kaczer, W. Goes, Th. Aichinger, Ph. Hehenberger, and M. Nelhiebel, “A Two-Stage Model for Negative Bias Temperature Instability,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2009, pp. 33–44.
- [C112] P.J. Wagner, Th. Aichinger, T. Grasser, M. Nelhiebel, and L.K.J. Vandamme, “Possible Correlation Between Flicker Noise And Bias Temperature Degradation,” in *Proc. 20th Intl.Conf. Noise and Fluctuations*, 2009, pp. 621–624.
- [C111] S. Tyaginov, V. Sverdlov, W. Goes, Ph. Schwaha, R. Heinzl, F. Stimpfl, and T. Grasser, “Si-O Bond-Breakage Energetics under Consideration of the Whole Crystal,” in *Proc. Intl. Semiconductor Technology Conference & China Semiconductor Technology International Conference*, 2009, p. 84.
- [C110] S. Tyaginov, V. Sverdlov, W. Goes, Ph. Schwaha, R. Heinzl, F. Stimpfl, and T. Grasser, “Impact of the Surrounding Network on the Si-O Bond-Breakage Energetics,” in *Proc. 2009 MRS Spring Meeting*, 2009.
- [C109] S. Tyaginov, V. Sverdlov, W. Goes, and T. Grasser, “Statistics of Si-O Bond-Breakage Rate Variations induced by O-Si-O Angle Fluctuations,” in *Proc. Intl.Workshop Comp.Electronics (IWCE)*, 2009, pp. 29–32.
- [C108] S. Tyaginov, W. Goes, T. Grasser, V. Sverdlov, Ph. Schwaha, R. Heinzl, and F. Stimpfl, “Description of Si-O Bond Breakage Using Pair-Wise Interatomic Potentials Under Consideration of the Whole Crystal,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2009, pp. 514–522.

- [C107] I. Starkov, S. Tyaginov, and T. Grasser, “Green’s Function Asymptotic in Two-Layered Periodic Medium,” in *Proceedings of the International Symposium NANOSTRUCTURES: Physics and Technology*, 2009, pp. 111–112.
- [C106] R. Southwick, B. Knowlton, B. Kaczer, and T. Grasser, “On the Thermal Activation of Negative Bias Temperature Instability,” in *Proc. Intl.Integrated Reliability Workshop*, 2009, pp. 36–41.
- [C105] J.T. Ryan, P.M. Lenahan, T. Grasser, and H. Enichlmair, “What Triggers NBTI? An “On The Fly” Electron Spin Resonance Approach,” in *Proc. Intl.Integrated Reliability Workshop*, 2009, pp. 42–45.
- [C104] J.T. Ryan, P.M. Lenahan, T. Grasser, and H. Enichlmair, “What Triggers NBTI? An “On The Fly” Electron Spin Resonance Approach,” in *Proc. Semic.Interface Specialists Conference (SISC)*, 2009.
- [C103] H. Reisinger, T. Grasser, and C. Schlünder, “A Study of NBTI by the Statistical Analysis of the Properties of Individual Defects in pMOSFETs,” in *Proc. Intl.Integrated Reliability Workshop*, 2009, pp. 30–35.
- [C102] B. Kaczer, T. Grasser, J. Martin-Martinez, E. Simoen, M. Aoulaiche, Ph.J. Roussel, and G. Groeseneken, “NBTI from the Perspective of Defect States with Widely Distributed Time Scales,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2009, pp. 55–60.
- [C101] Ph. Hehenberger, P.J. Wagner, H. Reisinger, and T. Grasser, “On the Temperature and Voltage Dependence of Short-Term Negative Bias Temperature Stress,” in *Proc. Europ.Symp. on Rel.Electr.Dev., Failure Physics and Analysis (ESREF)*, 2009.
- [C100] Ph. Hehenberger, P.J. Wagner, H. Reisinger, and T. Grasser, “Comparison of Fast Measurement Methods for Short-Term Negative Bias Temperature Stress and Relaxation,” in *Proc. ESSDERC*, 2009, pp. 311–314.
- [C99] Ph. Hehenberger, Th. Aichinger, T. Grasser, W. Goes, O. Triebel, B. Kaczer, and M. Nelhiebel, “Do NBTI-Induced Interface States Show Fast Recovery? A Study Using a Corrected On-The-Fly Charge-Pumping Measurement Technique,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2009.
- [C98] W. Goes, T. Grasser, M. Karner, and B. Kaczer, “A Model for Switching Traps in Amorphous Oxides,” in *Proc. Simulation of Semiconductor Processes and Devices*, 2009, pp. 159–162.
- [C97] J. Franco, B. Kaczer, A. Stesmans, V.V. Afanas’ev, K. Martens, M. Aoulaiche, T. Grasser, J. Mitard, and G. Groeseneken, “Impact of Si-Passivation Thickness and Processing on NBTI Reliability of Ge and SiGe pMOSFETs,” in *Proc. Semic.Interface Specialists Conference (SISC)*, 2009, (**best student paper award**).
- [C96] B. Bindu, W. Goes, B. Kaczer, and T. Grasser, “Analytical Solution of the Switching Trap Model for Negative Bias Temperature Stress,” in *Proc. Intl.Integrated Reliability Workshop*, 2009, pp. 93–96.
- [C95] Th. Aichinger, M. Nelhiebel, and T. Grasser, “Unambiguous Identification of the NBTI Recovery Mechanism using Ultra-Fast Temperature Changes,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2009, pp. 2–7.
- [C94] Th. Aichinger, M. Nelhiebel, and T. Grasser, “On the Temperature Dependence of NBTI Recovery,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2009, p. 1, (**invited, best paper ESREF ’08**).
- [C93] T. Grasser, W. Goes, and B. Kaczer, “Modeling Bias Temperature Instability During Stress and Recovery,” in *Proc. Simulation of Semiconductor Processes and Devices*, 2008, pp. 65–68.
- [C92] T. Grasser, “Towards Understanding Negative Bias Temperature Instability,” in *Proc. Intl.Integrated Reliability Workshop*, Oct. 2008, (**tutorial**).
- [C91] T. Grasser, B. Kaczer, Th. Aichinger, W. Goes, and Michael Nelhiebel, “Defect Creation Stimulated by Thermally Activated Hole Trapping as the Driving Force Behind Negative Bias Temperature Instability in SiO₂, SiON, and High-k Gate Stacks,” in *Proc. Intl.Integrated Reliability Workshop*, Apr. 2008, pp. 91–95.
- [C90] T. Grasser, B. Kaczer, and W. Goes, “An Energy-Level Perspective of Bias Temperature Instability,” in *Proc. Europ.Symp. on Rel.Electr.Dev., Failure Physics and Analysis (ESREF)*, 2008, (**invited, best paper IRPS ’08**).

- [C89] T. Grasser, B. Kaczer, and W. Goes, “An Energy-Level Perspective of Bias Temperature Instability,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2008, pp. 28–38, (**best paper award**).
- [C88] T. Grasser, “Negative Bias Temperature Instability: Modeling Challenges and Perspectives,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2008, (**tutorial**).
- [C87] H. Reisinger, R.P. Vollertsen, P.J. Wagner, T. Huttner, A. Martin, S. Aresu, W. Gustin, T. Grasser, and C. Schlünder, “The Effect of Recovery on NBTI Characterization of Thick Non-Nitrided Oxides,” in *Proc. Intl.Integrated Reliability Workshop*, 2008, pp. 1–6.
- [C86] B. Kaczer, T. Grasser, Ph.J. Roussel, J. Martin-Martinez, R. O’Connor, B.J. O’Sullivan, and G. Groeseneken, “Ubiquitous Relaxation in BTI Stressing-New Evaluation and Insights,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2008, pp. 20–27.
- [C85] W. Goes, M. Karner, S. Tyaginov, Ph. Hehenberger, and T. Grasser, “Level Shifts and Gate Interfaces as Vital Ingredients in Modeling of Charge Trapping,” in *Proc. Simulation of Semiconductor Processes and Devices*, 2008, pp. 69–72.
- [C84] W. Goes, M. Karner, V. Sverdlov, and T. Grasser, “A Rigorous Model for Trapping and Detrapping in Thin Gate Dielectrics,” in *Proc. Intl.Symp. on Physical and Failure Analysis of Integrated Circuits*, 2008, pp. 249–254.
- [C83] Th. Aichinger, M. Nelhiebel, and T. Grasser, “On the Temperature Dependence of NBTI Recovery,” in *Proc. Europ.Symp. on Rel.Electr.Dev., Failure Physics and Analysis (ESREF)*, 2008, pp. 1178–1184, (**best paper award**).
- [C82] T. Grasser, B. Kaczer, Ph. Hehenberger, W. Goes, R. O’Connor, H. Reisinger, W. Gustin, and C. Schlünder, “Simultaneous Extraction of Recoverable and Permanent Components Contributing to Bias-Temperature Instability,” in *Proc. Intl.Electron Devices Meeting (IEDM)*, 2007, pp. 801–804.
- [C81] T. Grasser, P.-J. Wagner, Ph. Hehenberger, W. Goes, and B. Kaczer, “A Rigorous Study of Measurement Techniques for Negative Bias Temperature Instability,” in *Proc. Intl.Integrated Reliability Workshop*, 2007, pp. 6–11.
- [C80] T. Grasser and B. Kaczer, “Negative Bias Temperature Instability: Recoverable versus Permanent Degradation,” in *Proc. ESSDERC*, 2007, pp. 127–130.
- [C79] T. Grasser, W. Goes, V. Sverdlov, and B. Kaczer, “The Universality of NBTI Relaxation and its Implications for Modeling and Characterization,” in *Proc. Intl.Rel.Phys.Symp. (IRPS)*, 2007, pp. 268–280.
- [C78] O. Triebel and T. Grasser, “Investigation of Vector Discretization Schemes for Box Volume Methods,” in *NSTI Nanotech Proceedings*, 2007, pp. 61–64.
- [C77] H. Kosina, O. Triebel, and T. Grasser, “Box Method for the Convection-Diffusion Equation Based on Exponential Shape Functions,” in *Proc. Simulation of Semiconductor Processes and Devices*, 12, 2007, pp. 317–320, Springer-Verlag Wien New York.
- [C76] W. Goes and T. Grasser, “Charging and Discharging of Oxide Defects in Reliability Issues,” in *Proc. Intl.Integrated Reliability Workshop*, 2007, pp. 27–32.
- [C75] W. Goes and T. Grasser, “First-Principles Investigation on Oxide Trapping,” in *Proc. Simulation of Semiconductor Processes and Devices*, 12, 2007, pp. 157–160, Springer-Verlag Wien New York.
- [C74] O. Baumgartner, M. Karner, S. Holzer, M. Pourfath, T. Grasser, and H. Kosina, “Adaptive Energy Integration of Non-Equilibrium Green’s Functions,” in *NSTI Nanotech Proceedings*, 2007, pp. 145–148.
- [C73] T. Grasser, W. Goes, and B. Kaczer, “Modeling of Dispersive Transport in the Context of Negative Bias Temperature Instability,” in *Proc. Intl.Integrated Reliability Workshop*, 2006, pp. 5–10.
- [C72] T. Grasser, R. Entner, O. Triebel, H. Enichlmair, and R. Minixhofer, “TCAD Modeling of Negative Bias Temperature Instability,” in *Proc. Simulation of Semiconductor Processes and Devices*, Monterey, USA, Sept. 2006, pp. 330–333.
- [C71] T. Grasser and S. Selberherr, “Modeling of Negative Bias Temperature Instability,” in *Abstracts 7th Symposium Diagnostics & Yield: Advanced Silicon Devices and Technologies for ULSI ERA*, Warszawa, June 2006, pp. 1–2, (**invited**).

- [C70] O. Triebel and T. Grasser, "Vector Discretization Schemes Based on Unstructured Neighbourhood Information," in *Proc. CAS*, 2006, pp. 337–340.
- [C69] M. Spevak, R. Heinzl, P. Schwaha, and T. Grasser, "A Computational Framework for Topological Operations," in *Proceedings of the PARA Conference*, Umea, June 2006, pp. 57–60.
- [C68] M. Spevak, R. Heinzl, P. Schwaha, and T. Grasser, "Process and Device Simulation With a Generic Scientific Simulation Environment," in *Proceedings International Conference on Microelectronics (MIEL)*, Beograd, Apr. 2006, pp. 475–478.
- [C67] M. Spevak, R. Heinzl, P. Schwaha, and T. Grasser, "Simulation of Microelectronic Structures Using A Posteriori Error Estimation and Mesh Optimization," in *5th Mathmod Vienna Proceedings*, Wien, Feb. 2006, p. 317, invited.
- [C66] A. Sheikholeslami, R. Heinzl, S. Holzer, C. Heitzinger, M. Spevak, M. Leicht, O. Häberlen, J. Fugger, F. Badrieh, F. Parhami, H. Puchner, T. Grasser, and S. Selberherr, "Applications of Two- and Three-Dimensional General Topography Simulator in Semiconductor Manufacturing Processes," in *Proceedings of the 14th Iranian Conference on Electrical Engineering ICEE 2006*, Tehran, May 2006, pp. 1–4.
- [C65] P. Schwaha, R. Heinzl, M. Spevak, and T. Grasser, "Advanced Equation Processing for TCAD," in *Proceedings of the PARA Conference*, Umea, June 2006, pp. 65–68.
- [C64] P. Schwaha, R. Heinzl, W. Brezna, J. Smoliner, H. Enichlmair, R. Minixhofer, and T. Grasser, "Leakage Current Analysis of a Real World Silicon-Silicon Dioxide Capacitance," in *Proceedings International Caribbean Conference on Devices, Circuits and Systems (ICCDACS)*, Playa del Carmen, Apr. 2006, pp. 365–370.
- [C63] M. Karner, A. Gehring, M. Wagner, R. Entner, S. Holzer, W. Goes, M. Vasicek, T. Grasser, H. Kosina, and S. Selberherr, "VSP-A Gate Stack Analyzer," in *WODIM 2006 14th Workshop on Dielectrics in Microelectronics Workshop Programme and Abstracts*, Catania, June 2006, pp. 101–102.
- [C62] M. Karner, A. Gehring, S. Holzer, M. Pourfath, M. Wagner, H. Kosina, T. Grasser, and S. Selberherr, "VSP-A Multi-Purpose Schrödinger-Poisson Solver for TCAD Applications," in *11th International Workshop on Computational Electronics Book of Abstracts*, Wien, May 2006, pp. 255–256.
- [C61] M. Karner, M. Wagner, T. Grasser, and H. Kosina, "A Physically Based Quantum Correction Model for DG MOSFETs," in *San Francisco 2006 MRS Meeting Abstracts*, San Francisco, Apr. 2006, pp. 104–105.
- [C60] S. Holzer, A. Sheikholeslami, M. Karner, and T. Grasser, "Comparison of Deposition Models for TEOS CVD Process," in *WODIM 2006 14th Workshop on Dielectrics in Microelectronics Workshop Programme and Abstracts*, Catania, June 2006, pp. 158–159.
- [C59] S. Holzer, Ch. Hollauer, H. Ceric, M. Karner, T. Grasser, E. Langer, and S. Selberherr, "Three-Dimensional Transient Interconnect Analysis With Regard to Mechanical Stress," in *Proceedings 13th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Singapore, July 2006, pp. 154–157.
- [C58] R. Heinzl, M. Spevak, P. Schwaha, and T. Grasser, "A High Performance Generic Scientific Simulation Environment," in *Proceedings of the PARA Conference*, Umea, June 2006, pp. 61–64.
- [C57] R. Heinzl, M. Spevak, P. Schwaha, and T. Grasser, "High Performance Process and Device Simulation with a Generic Environment," in *Proceedings of the 14th Iranian Conference on Electrical Engineering ICEE 2006*, Tehran, May 2006, pp. 1–4.
- [C56] R. Heinzl, M. Spevak, P. Schwaha, and T. Grasser, "Multidimensional and Multitopological TCAD with a Generic Scientific Simulation Environment," in *Proceedings International Caribbean Conference on Devices, Circuits and Systems (ICCDACS)*, Playa del Carmen, Apr. 2006, pp. 173–176.
- [C55] R. Heinzl, M. Spevak, P. Schwaha, and T. Grasser, "A Generic Scientific Simulation Environment for Multidimensional Simulation in the Area of TCAD," in *NSTI Nanotech Proceedings*, Princeton, May 2006, pp. 526–529.

- [C54] R. Heinzl, P. Schwaha, M. Spevak, and T. Grasser, “Concepts for High Performance Generic Scientific Computing,” in *5th Mathmod Vienna Proceedings*, Wien, Feb. 2006, pp. 4.1–4.9.
- [C53] R. Entner, T. Grasser, H. Enichlmair, and R. Minixhofer, “Influence of Interface and Oxide Traps on Negative Bias Temperature Instability,” in *Abstracts IEEE 2006 Silicon Nanoelectronics Workshop*, Honolulu, June 2006, pp. 163–164.
- [C52] R. Entner, T. Grasser, H. Enichlmair, and R. Minixhofer, “Investigation of NBTI Recovery During Measurement,” in *San Francisco 2006 MRS Meeting Abstracts*, San Francisco, Apr. 2006, pp. 110–111.
- [C51] R. Entner, T. Grasser, H. Enichlmair, and R. Minixhofer, “Negative Bias Temperature Instability Modeling for High-Voltage Oxides at Different Stress Temperatures,” in *Proc. Workshop on Dielectrics in Microelectronics*, 2006, pp. 96–97.
- [C50] T. Grasser, “Mixed Mode Device/Circuit Simulation,” in *MOS-AK/ESSDERC Workshop 2005* (<http://www.mos-ak.org/grenoble>), Grenoble, Sept. 2005, (invited).
- [C49] T. Grasser, “Higher-Order Moment Models for Engineering Applications,” in *SEMIC 2005* (<http://mox.polimi.it/semic2005>), Milan, Feb. 2005, (invited).
- [C48] M. Wagner, M. Karner, and T. Grasser, “Quantum Correction Models for Modern Semiconductor Devices,” in *Proc. 15th Intl. Workshop on the Physics of Semiconductor Devices*, New Dehli, India, Dec. 2005, pp. 458–461.
- [C47] M. Spevak and T. Grasser, “Discretization Schemes for Macroscopic Transport Equations on Non-Cartesian Coordinate Systems,” in *Proc. European Simulation and Modeling Conference*, Porto, Oct. 2005, pp. 474–478.
- [C46] A. Sheikholeslami, F. Parhami, R. Heinzl, E. Al-Ani, C. Heitzinger, F. Badrieh, H. Puchner, T. Grasser, and S. Selberherr, “Applications of Three-Dimensional Topography Simulation in the Design of Interconnect Lines,” in *Proc. Simulation of Semiconductor Processes and Devices*, Tokyo, Japan, Sept. 2005, pp. 187–190.
- [C45] A. Sheikholeslami, S. Holzer, C. Heitzinger, M. Leicht, O. Häberlen, J. Fugger, T. Grasser, and S. Selberherr, “Inverse Modeling of Oxide Deposition Using Measurements of a TEOS CVD Process,” in *Proc. PhD Research in Microelectronics and Electronics*, Lausanne, July 2005, pp. 279–282.
- [C44] A. Sheikholeslami, E. Al-Ani, R. Heinzl, C. Heitzinger, F. Parhami, F. Badrieh, H. Puchner, T. Grasser, and S. Selberherr, “Level Set Method Based General Topography Simulator and its Applications in Interconnect Processes,” in *Proc. 6th European Workshop on Ultimate Integration of Silicon*, Bologna, Italy, Apr. 2005, pp. 139–142.
- [C43] P. Schwaha, R. Heinzl, W. Brezna, J. Smoliner, H. Enichlmair, R. Minixhofer, and T. Grasser, “Fully Three-Dimensional Analysis of Leakage Current in Non-Planar Oxides,” in *Proc. European Simulation and Modeling Conference*, Porto, Oct. 2005, pp. 469–473.
- [C42] P. Schwaha, M. Spevak, R. Heinzl, and T. Grasser, “Coupling Three-Dimensional Mesh Adaptation with an A Posteriori Error Estimator,” in *Proc. Simulation of Semiconductor Processes and Devices*, Tokyo, Japan, Sept. 2005, pp. 235–238.
- [C41] S. Holzer, Ch. Hollauer, H. Ceric, S. Wagner, E. Langer, T. Grasser, and S. Selberherr, “Three-Dimensional Transient Electro-Thermal Interconnect Simulation for Stress and Electromigration Analysis,” in *Proc. NSTI Nanotech*, Anaheim, California, USA, May 2005, vol. 3, pp. 620–623.
- [C40] S. Holzer, Ch. Hollauer, H. Ceric, S. Wagner, E. Langer, T. Grasser, and S. Selberherr, “Transient Electro-Thermal Investigations of Interconnect Structures Exposed to Mechanical Stress,” in *Proc. SPIE’s 2nd Intl. Symposium on Microtechnologies for the New Millennium: VLSI Circuits and Systems*, Sevilla, Spain, May 2005, pp. 380–387.
- [C39] R. Heinzl, P. Schwaha, M. Spevak, and T. Grasser, “Adaptive Mesh Generation for TCAD with Guaranteed Error Bounds,” in *Proc. European Simulation and Modeling Conference*, Porto, Oct. 2005, pp. 425–429.
- [C38] R. Heinzl and T. Grasser, “Generalized Comprehensive Approach for Robust Three-Dimensional Mesh Generation for TCAD,” in *Proc. Simulation of Semiconductor Processes and Devices*, Tokyo, Japan, Sept. 2005, pp. 211–214.

- [C37] R. Heinzl, M. Spevak, P Schwaha, and T. Grasser, “A Novel Technique for Coupling Three Dimensional Mesh Adaption With An A Posteriori Error Estimator,” in *Proc. PhD Research in Microelectronics and Electronics*, Lausanne, July 2005, pp. 175–178.
- [C36] R. Entner, A. Gehring, H. Kosina, T. Grasser, and S. Selberherr, “Modeling of Tunneling Currents for Highly Degraded CMOS Devices,” in *Proc. Simulation of Semiconductor Processes and Devices*, Tokyo, Japan, Sept. 2005, pp. 219–222.
- [C35] R. Entner, A. Gehring, H. Kosina, T. Grasser, and S. Selberherr, “Impact of Multi-Trap Assisted Tunneling on Gate Leakage of CMOS Memory Devices,” in *Proc. NSTI Nanotech*, Anaheim, California, USA, May 2005, vol. 3, pp. 45–48.
- [C34] E. Al-Ani, R. Heinzl, P. Schwaha, T. Grasser, and S. Selberherr, “Three-Dimensional State-Of-The-Art Topography Simulation,” in *Proc. European Simulation and Modeling Conference*, Porto, Oct. 2005, pp. 430–432.
- [C33] T. Grasser, R. Kosik, C. Jungemann, H. Kosina, B. Meinerzhagen, and S. Selberherr, “A Non-Parabolic Six Moments Model for the Simulation of Sub-100 nm Semiconductor Devices,” in *Proc. 10th Intl. Workshop on Computational Electronics, IWCE-10*, West Lafayette, USA, 2004, pp. 36–37.
- [C32] T. Grasser, C. Jungemann, H. Kosina, B. Meinerzhagen, and S. Selberherr, “Advanced Transport Models for Sub-Micrometer Devices,” in *Proc. Simulation of Semiconductor Processes and Devices*, Munich, Germany, Sept. 2004, pp. 1–8, (invited).
- [C31] T. Grasser, H. Kosina, and S. Selberherr, “On the Validity of the Relaxation Time Approximation for Macroscopic Transport Models,” in *Proc. Simulation of Semiconductor Processes and Devices*, Munich, Germany, Sept. 2004, pp. 109–112.
- [C30] S. Wagner, T. Grasser, and S. Selberherr, “Physical Modeling of Semiconductor Devices for Microwave Applications,” in *Proc. Asia Pacific Microwave Conference (APMC)*, New Delhi, India, 2004, pp. 1–4, (invited).
- [C29] S. Wagner, T. Grasser, and S. Selberherr, “Evaluation of Linear Solver Modules for Semiconductor Device Simulation,” in *Proc. 5th Intl. Conference on Mathematical Problems in Engineering and Aerospace Sciences (ICNPAA)*, Timisoara, Romania, June 2004, pp. 1–4.
- [C28] S. Wagner, T. Grasser, and S. Selberherr, “Performance Evaluation of Linear Solvers Employed for Semiconductor Device Simulation,” in *Proc. Simulation of Semiconductor Processes and Devices*, Munich, Germany, Sept. 2004, pp. 351–354.
- [C27] S. Wagner, T. Grasser, and S. Selberherr, “Mixed-Mode Device and Circuit Simulation,” in *Proc. 11th Intl. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES)*, Szczecin (Poland), 2004, pp. 36–41, (invited).
- [C26] S. Wagner, T. Grasser, and S. Selberherr, “Benchmarking Linear Solvers with Semiconductor Simulation Examples,” in *Proc. Intl. Conf. on Scientific and Engineering Computation (ICSEC)*, Singapore, 2004.
- [C25] S. Wagner, T. Grasser, C. Fischer, and S. Selberherr, “Concepts and Implementation of an Advanced Equation Assembly Module,” in *Proc. 8th World Multiconference on Systemics, Cybernetics and Informatics*, Orlando (Florida), 2004, pp. 150–155.
- [C24] A. Sheikholeslami, C. Heitzinger, E. Al-Ani, R. Heinzl, T. Grasser, and S. Selberherr, “Three-Dimensional Surface Evolution Using a Level Set Method,” in *1st Iranian Ph.D. Students Seminar on Computer Science, Mathematics and Statistics (ICSMS)*, Paris, France, Dec. 2004.
- [C23] A. Sheikholeslami, C. Heitzinger, T. Grasser, and S. Selberherr, “Three-Dimensional Topography Simulation for Deposition and Etching Processes Using a Level Set Method,” in *Proc. 24th Intl. Conference on Microelectronics (MIEL 2004)*, Niš, Serbia, 2004, vol. 1, pp. 241–244.
- [C22] R. Kosik, T. Grasser, R. Entner, and K. Dragosits, “On the Highest Order Moment Closure Problem,” in *Proc. IEEE International Spring Seminar on Electronics Technology*, Sophia, Bulgaria, 2004, pp. 118–121.

- [C21] S.C. Kim, W. Bahng, N.K. Kim, E.D. Kim, T. Ayalew, T. Grasser, and S. Selberherr, “Numerical Simulation and Optimization for 900V 4H-SiC DiMOSFET Fabrication,” in *Proc. 5th European Conference on Silicon Carbide and Related Materials (ECSCRM)*, Bologna, Italy, Sept. 2004, pp. 492–493.
- [C20] S. Holzer, A. Sheikholeslami, S. Wagner, C. Heitzinger, T. Grasser, and S. Selberherr, “Optimization and Inverse Modeling for TCAD Applications,” in *Symposium on Nano Device Technology*, Hsinchu, Taiwan, May 2004, pp. 113–116.
- [C19] R. Entner, A. Gehring, T. Grasser, and S. Selberherr, “A Comparison of Quantum Correction Models for the Three-Dimensional Simulation of FinFET Structures,” in *Proc. IEEE International Spring Seminar on Electronics Technology*, Sophia, Bulgaria, 2004, pp. 114–117, (best poster).
- [C18] H. Ceric, R. Sabelka, S. Holzer, W. Wessner, S. Wagner, T. Grasser, and S. Selberherr, “The Evolution of the Resistance and Current Density During Electromigration,” in *Proc. Simulation of Semiconductor Processes and Devices*, Munich, Germany, Sept. 2004, pp. 331–334.
- [C17] T. Ayalew, S.C. Kim, T. Grasser, and S. Selberherr, “Numerical Analysis of SiC Merged PiN Schottky Diodes,” in *Proc. 5th European Conference on Silicon Carbide and Related Materials (ECSCRM)*, Bologna, Italy, Sept. 2004, pp. 476–477.
- [C16] T. Ayalew, S. Wagner, T. Grasser, and S. Selberherr, “Numerical Simulation of Microwave MESFETs in 4H-SiC Fabricated Using Epitaxial Layers on Semi-Insulating Substrates,” in *Proc. 5th European Conference on Silicon Carbide and Related Materials (ECSCRM)*, Bologna, Italy, Sept. 2004, pp. 76–77.
- [C15] T. Ayalew, T. Grasser, H. Kosina, and S. Selberherr, “Accurate Modeling of Lattice Site-Dependent Incomplete Ionization in α -SiC Devices,” in *Proc. 5th European Conference on Silicon Carbide and Related Materials (ECSCRM)*, Bologna, Italy, Sept. 2004, pp. 92–93.
- [C14] T. Ayalew, T. Grasser, H. Kosina, and S. Selberherr, “Accurate Modeling of Lattice Site-Dependent Ionization Level of Impurities in α -SiC Devices,” in *Proc. Simulation of Semiconductor Processes and Devices*, Munich, Germany, Sept. 2004, pp. 295–298.
- [C13] T. Grasser, “Closure Relations for Macroscopic Transport Models,” in *Proc. Intl. Semiconductor Device Research Symposium*, Washington DC, USA, Dec. 2003, pp. 504–505, (invited).
- [C12] T. Grasser, H. Kosina, and S. Selberherr, “Reformulation of Macroscopic Transport Models Based on the Moments of the Scattering Integral,” in *Proc. Simulation of Semiconductor Processes and Devices*, Boston, USA, Sept. 2003, pp. 63–66.
- [C11] T. Grasser, H. Kosina, and S. Selberherr, “Rigorous Modeling of Mobilities and Relaxation Times Using Six Moments of the Distribution Function,” in *Proc. 4th European Workshop on Ultimate Integration of Silicon*, Udine, Italy, Mar. 2003, pp. 105–108.
- [C10] S. Wagner, T. Grasser, C. Fischer, and S. Selberherr, “Advanced Equation Assembling Techniques for Numerical Simulators,” in *Proc. 2003 European Simulation and Modeling Conference*, Naples, Oct. 2003, pp. 390–394.
- [C9] S. Wagner, T. Grasser, C. Fischer, and S. Selberherr, “A Simulator Module for Advanced Equation Assembling,” in *Proc. 15th European Simulation Symposium and Exhibition*, Delft, Oct. 2003, pp. 55–64.
- [C8] S. Wagner, T. Grasser, C. Fischer, and S. Selberherr, “A Generally Applicable Approach for Advanced Equation Assembling,” in *Proc. 7th IASTED Intl. Conf. on Software Engineering and Applications*, Marina del Rey, CA, Nov. 2003, pp. 494–499.
- [C7] S. Wagner, V. Palankovski, R. Quay, T. Grasser, and S. Selberherr, “Numerical Simulation of High-Speed High-Breakdown Indium Phosphide HBTs,” in *Proc. 13th Intl. Workshop on the Physics of Semiconductor Devices*, V. Kumar and P.K. Basu, Eds., Madras, India, Dec. 2003, pp. 836–838.
- [C6] S. Wagner, V. Palankovski, G. Röhrer, T. Grasser, and S. Selberherr, “Numerische Berechnung von Silizium-Germanium Heterostruktur-Bipolartransistoren,” in *Informationstagung Mikroelektronik, ME’2003*, G. Fiedler, Ed., Austria, Wien, Oct. 2003, pp. 383–388.

- [C5] S. Wagner, V. Palankovski, T. Grasser, G. Röhrer, and S. Selberherr, "A Direct Extraction Feature for Scattering Parameters of SiGe-HBTs," in *Proc. Intl. SiGe Technology and Device Meeting (ISDTM)*, Nagoya, Japan, Jan. 2003, pp. 83–84.
- [C4] J.M. Park, T. Grasser, and S.Selberherr, "High-Voltage Super-Junction SOI-LDMOSFETs with Reduced Drift Length," in *Proc. 11th Intl. Symp. on Silicon-On-Insulator Technology and Devices*, Paris, Apr. 2003, pp. 273–282.
- [C3] S. Holzer, R. Minixhofer, C. Heitzinger, J. Fellner, T. Grasser, and S. Selberherr, "Extraction of Material Parameters Based on Inverse Modeling of Three-Dimensional Interconnect Structures," in *Proc. THERMINIC*, Aix-en-Provence, France, Sept. 2003, pp. 263–268.
- [C2] T. Ayalew, J.M. Park, A. Gehring, T. Grasser, and S. Selberherr, "Silicon Carbide Accumulation-Mode Laterally Diffused MOSFET," in *Proc. 33th European Solid-State Device Research Conference*, Estoril, Sept. 2003, pp. 581–584.
- [C1] T. Ayalew, J.M. Park, A. Gehring, T. Grasser, and S.Selberherr, "Modeling and Simulation of SiC MOSFETs," in *Proc. IASTED Intl. Conf. on Applied Simulation and Modeling, ASM'2003*, Marbella, Sept. 2003, pp. 552–556.