

STAND-ALONE PROJECT

FINAL REPORT

Project number

P23958-N24

Project title¹

__Physikalische_Modellierung_von_Hot-Carrier_Degradation__

Project leader

__Tibor_Grasser__

¹ Short title in English and German language

I. Summary for public relations work

1. Zusammenfassung für die Öffentlichkeitsarbeit

Die Zuverlässigkeit von elektronischen Bauelementen, wie zum Beispiel die der omnipräsenten Metall-Oxid-Halbleiter-Feldeffekttransistoren (MOSFET), ist die Basis für eine ausfallsichere Funktionalität von elektronischen Geräten. In diesem Zusammenhang sieht die *International Technology Roadmap for Semiconductors* (ITRS), welche eine Prognose über die zukünftige Entwicklung der Halbleitertechnik darstellt, Mechanismen, die die Zuverlässigkeit mindern, als größte Herausforderung. Dabei wird der Degradierungsprozess der *hot-carrier degradation* (HCD, Degradation durch hochenergetische/heiße Ladungsträger) besonders hervorgehoben, da er auf Grund der ständigen Verkleinerung von MOSFETs und der damit verbundenen Erhöhung der elektrischen Feldstärken an Bedeutung gewonnen hat. Um sich dieser Herausforderung stellen zu können, müssen die physikalischen Ursachen für HCD verstanden und akkurat beschrieben werden. Nur so ist die Weiterentwicklung der Mikro- bzw. Nanoelektronik sichergestellt.

Das im Rahmen dieses Projektes entwickelte und validierte physikalische Modell für HCD verknüpft drei wesentliche Aspekte, welche mit HCD in Verbindung gebracht werden: eine sorgfältige Beschreibung des Ladungsträgertransportes, eine mikroskopische Darstellung der Defektgenerierung und die Modellierung des degradierenden MOSFETs mit der Zeit. Die Grundannahme ist, dass Dissoziation von Silizium-Wasserstoff-Bindungen im Materialübergang zwischen Bulk und Oxid die Hauptursache für HCD ist. In den Dissoziationsprozess einer Bindung können ein einzelner oder mehrere Ladungsträger mit ausreichend hohen Energien involviert sein. Die dazugehörigen Wahrscheinlichkeiten werden mittels der Verteilungsfunktion der Ladungsenergien modelliert. Diese wird durch Lösung der Boltzmann'schen Transportgleichung für eine bestimmte MOSFET Architektur unter bestimmten Stressspannungen (Spannungen höher als die Betriebsspannung) ermittelt. Für die Bewältigung dieser Aufgabe haben wir den auf dem Institut für Mikroelektronik entwickelte Boltzmannlöser ViennaSHE verwendet. ViennaSHE berücksichtigt sowohl die volle Bandstruktur von Silizium, als auch Streumechanismen wie Stoßionisation, Streuung an ionisierten Verunreinigungen, Elektron-Phonon-Wechselwirkung und Elektron-Elektron-Wechselwirkung.

Das Modell wurde erfolgreich mithilfe einer umfangreichen Reihe an Messdaten validiert. Dafür wurden MOSFETs verschiedener Architekturen über einen weiten Spannungsbereich vermessen. Wir haben die Auswirkung jedes Modellbausteins auf jeden einzelnen Transistor überprüft und können daraus folgende, teilweise unerwartete, Schlüsse ziehen. Entgegen des bisherigen Verständnisses, kann die Dissoziation einer Silizium-Wasserstoff-Bindung durch mehrere Ladungsträger auch in Hochspannungstransistoren eine wesentliche Rolle spielen während die Dissoziation verursacht durch einzelne Ladungsträger in MOSFETs mit Geometrien im Nanometer-Bereich den dominierenden Beitrag leisten kann. Eine ebenfalls neue Erkenntnis ist, dass die

Elektron-Elektron-Wechselwirkung auch in MOSFETs mit langen Kanälen (Kanallänge größer als 100nm) zu HCD beiträgt. Des Weiteren zeigt das Temperaturverhalten, dass bei höheren Temperaturen HCD auch in MOSFETs mit kurzen Längen wenig ausgeprägt ist. Das Temperaturverhalten von HCD wird daher durch eine Kombination aus Stressspannungen und Transistorarchitektur bestimmt.

2. Summary for public relations work

The International technology roadmap for semiconductors considers the problem of transistor reliability as a major issue to be addressed in order to ensure further evolution of modern micro/nanoelectronics. Among the different degradation modes, hot-carrier degradation (HCD) is suggested to be the major concern. This is because in modern metal-oxide-semiconductor field-effect-transistors (MOSFETs) the operating voltage cannot be scaled beyond certain values as the linear dimensions continue to shrink, thereby resulting to high electric fields in the device and thus significant HCD. Therefore, a detailed understanding of the degradation physics is required followed by an accurate physics-based description.

Within this project, we developed and validated the first physics-based model for HCD which covers and links three main aspects related to this effect: thorough carrier transport treatment, a microscopic description of the defect generation mechanisms, and modeling of the degraded devices. This model assumes that HCD is related to the dissociation of silicon-hydrogen bonds at the interface driven by single- and multiple-carrier bond-breakage mechanisms. The rates of these mechanisms (as well as the rates of their superpositioned effect) are modeled using the carrier energy distribution function (DF) which is obtained by solving the Boltzmann transport equation (BTE) for a particular device architecture and defined stress/operating conditions. To accomplish this task we use the deterministic BTE solver ViennaSHE, which has been also developed at our Institute. ViennaSHE considers the full band structure of silicon as well as scattering mechanisms such as impact ionization, scattering at ionized impurities, electron-phonon and electron-electron interactions. In particular electron-electron scattering (EES) determines HCD in short-channel devices (<100nm) and is therefore an important component of the model.

The model has been validated against an extensive set of HCD experimental data acquired in scaled transistors as well as in high-voltage devices over a wide range of stress conditions. For all these devices we carefully checked the importance of each model ingredient and obtained a number of non-trivial conclusions. First, in contrast to the previous understanding, the multiple-carrier process of Si-H dissociation can play a substantial role even in high-voltage devices, while the single-carrier mechanism can be dominant in ultra-scaled MOSFETs. Second, at high stress voltages EES can make a significant contribution to HCD also in long-channel transistors. Finally, even in devices with gate length of less than 100nm HCD can become less pronounced at higher temperatures and the temperature behavior of this phenomenon is determined by the combination of stress conditions and device architecture.

Typically, if one switches from accelerated stress to milder operating conditions, the degradation physics change, thereby making simplified empirical models not applicable. Careful validation of our approach and detailed understanding of the physical picture behind HCD make our model predictive, i.e. the model allows for device life-time extraction under both stress and operating conditions.

II. Brief project report

1. Report on research work

1.1 Information on the development of the research project

The main goal of the project was the development and validation of a physics-based model for hot-carrier degradation (HCD) in ultra-scaled and high-voltage MOS transistors which should be valid for both stress and operating conditions and applicable to HCD in transistors with different geometries and dimensions. Therefore, the model must properly address the physical mechanisms driving HCD. The physical picture behind HCD can be conditionally separated into three main sub-tasks: modeling of carrier transport, a microscopic description of defect generation, and simulation of the degraded devices. Therefore, the project was organized to include three main modules devoted to these aspects.

Carrier transport module: hot-carrier degradation is associated with the build-up of defects at or near the silicon/dielectric interface due to dissociation of Si-H bonds. There are two competing mechanisms for Si-H bond-breakage, namely single- and multiple-carrier processes. The former mechanism is triggered by a solitary hot carrier which has sufficient energy to break the Si-H bond in a single collision, while the latter process is related to the multiple vibrational excitation of the bond by collisions with several lower energetic (“colder”) carriers. In order to properly model the rates of these mechanisms one needs to be able to distinguish between hot and cold carriers. To do so, the carrier energy distribution function is needed. The carrier DFs are obtained by solving the Boltzmann transport equation with our deterministic solver ViennaSHE. However, this solution is complicated and computationally expensive. As a result, despite better knowledge, in practice the carrier DF is often not incorporated in simplified modeling approaches which thus remain empirical. Therefore, our HCD model is the first approach which employs detailed information on carrier transport and can adequately describe the bond dissociation rates.

We have developed and verified two versions of our HCD model: the first one is based on the accurate BTE solution using ViennaSHE, while the second one employs the more computationally efficient drift-diffusion (DD) scheme. ViennaSHE considers the full band structure of Si and essential scattering mechanisms such as impact ionization, surface scattering, scattering at ionized impurities as well as electron-phonon and electron-electron scattering (EES). We have demonstrated that EES is one of the main contributors to HCD in decananometer transistors because it populates the high-energy fraction of the carrier ensemble, thereby changing the shape of the DF. As for the DD-based model, the main features of the carrier DF is mimicked using an analytical expression with the

parameters obtained from a DD solution. The effect of EES in the case of short-channel devices was modeled by a rate balance equation developed within the DD-based model. To check the validity of this variant of the model we used carrier DFs obtained with ViennaSHE as reference data. We have shown that the DD-based carrier transport treatment can represent carrier DFs in high-voltage laterally diffused metal oxide semiconductor (LDMOS) transistors with very good agreement. Therefore, we conclude the DD-based variant of the model provides good accuracy and at the same time is computationally less expensive.

Defect generation: one of the main deficiencies of previous HCD paradigms is that single- and multiple-carrier processes were considered as independent mechanisms. This simplified treatment is doubtful because these two mechanisms are just two competing pathways of the same reaction, which converts virgin Si-H bond to electrically active dangling Si- bonds, and must therefore be considered consistently. This is done in the latest version of our approach. We also take into account the strong coupling of these mechanisms when the bond is first preheated (weakened) by several colder particles due to multi-vibrational excitation and then dissociated by a single not-quite-that-hot carrier. Our model also considers statistical variations of the bond-breakage energy as well as lowering of this energy by the dipole-field interaction.

Another important improvement related to our model is the idea that Si-H dissociation occurs not via the vibrational bending mode but via the stretching mode. Note that previous HCD models assumed that bond-rupture has an activation energy of $\sim 1.5\text{eV}$, a value corresponding to the bending mode. However, this idea contradicts experimental data which show that the bond-breakage energy lies in the range of $2.5\text{-}2.9\text{eV}$, i.e. corresponds to the stretching mode. It is important to emphasize that the vibrational life-time of the bond strongly depends on temperature and this trend is also captured by our model.

The mutual effect of carrier transport and defect generation has also been analyzed. We showed that build-up of interface states can substantially change carrier DFs, which, in turn, changes the rates of both single- and multiple-carrier processes. Therefore, for an accurate description of HCD one needs to consider these two aspects self-consistently.

Simulation of degraded devices: the model was calibrated and validated against HCD data measured for scaled transistors with gate lengths of 65, 100, and 150nm and for high-voltage devices, i.e. LDMOS transistors with n- and p-channels. This goal has been accomplished in extensive collaboration with imec (Leuven, Belgium), ams AG (Unterpremstätten, Austria), and Infineon (Villach, Austria and München, Germany). To assess HCD we measured changes of the saturation and linear drain currents as well as the threshold voltage shift. To additionally check the model validity we also considered charge-pumping measurements to access the spatial distribution of the interface states across the channel. We have shown that the model can properly describe HCD in a wide class of transistors stressed under different conditions using a unique set of model parameters. Within the calibration/validation step, we also studied the importance of each model ingredient over a wide range of stress conditions and device dimensions. This analysis resulted in a number of

intriguing findings: We showed that – as opposed to the previous understanding of HCD – the single-carrier process can be dominant even in scaled devices with a gate length of 65nm. As for the multiple-carrier process, which was previously assumed to be pronounced only in short-channel MOSFETs, it plays a significant role also in LDMOS devices (with a gate/channel length of several μm) stressed at very high drain voltages. Another important finding is related to the role of electron-electron scattering. The previous HCD paradigm claimed that EES starts to play an important role in devices with gate lengths shorter than 150nm. We have shown, however, that even in nMOSFETs with gate lengths of 200 and 300nm the effect of EES can be substantial. The interplay between the single- and multiple-carrier mechanisms as well as EES determines the temperature behavior of HCD. The old findings suggested that in long-channel devices HCD is more severe at lower temperatures, while in their short-channel counterparts HCD becomes more pronounced at elevated temperatures, and the transition between these two trends was suggested to occur at gate lengths of $\sim 150\text{nm}$. We showed, however, that even in nMOSFETs with a gate length of 65nm HCD can be weaker or stronger at lower temperatures, depending on the stress voltage.

The final conclusion from all these findings, which dramatically changes the understanding of HCD, is that the importance of a particular HCD mechanism is determined not exclusively by the gate/channel lengths but by the entire combination of stress conditions and device topology.

Overall, the initial project plan was followed and additional contributions beyond the initial project goals were made in both modules.

1.2 Most important results and brief description of their significance (main points) with regard to the following:

The main result of this project is the development of a physics-based model for hot-carrier degradation which is reliable and predictive because it considers all essential physical mechanisms responsible for HCD. This is the first model which explicitly links bond-breakage rates with carrier transport. Note that in previous HCD models the treatment of carrier transport was skipped and the impact of the carrier energy distribution was approximated using empirical factors. Such an empirical/phenomenological treatment, however, has limited validity because even a small change in the applied stress conditions can lead to a change of the dominant HCD mechanism, a situation which cannot be captured by these simplified approaches. As a consequence, extrapolation from stress to use conditions becomes inaccurate. Moreover, our modeling framework considers the impact of the generated interface states on the carrier DF. Such a self-consistent consideration of defect generation kinetics and carrier transport is also questionable within empirical/phenomenological approaches.

As has been demonstrated, HCD is a very complex phenomenon which cannot be described by a single process. As such, for an accurate description valid for different technologies, the interplay between various mechanisms needs to be considered. We have shown that even in long-channel and/or high-voltage devices one cannot neglect the contribution of electron-electron scattering and

the multiple-carrier process of bond dissociation. On the other hand, the single-carrier mechanism plays a significant role also in decananometer devices. The same holds true for the intricate temperature behavior of HCD. Only after all the effects are taken into account, combined with the temperature dependent vibrational life-time, the true temperature characteristic of HCD can be revealed. Therefore, the importance of each of these mechanisms is determined by the superposition of the device geometry and applied voltages, not exclusively by one of these factors.

We have also developed and validated a version of the HCD model which is based on an analytical expression for the carrier distribution function with parameters computed using the drift-diffusion scheme. The effect of electron-electron scattering on the electron DF was captured by our approach by using the rate balance equation and a unique set of model parameters. It was shown that the model can properly represent DFs and HCD (including its temperature dependence) in nMOSFETs with gate lengths in a range of 65-300 nm, while for longer devices a similar model without EES was found to be applicable. The main advantage of this model is that it uses the simple and fast DD scheme instead of a computationally intensive solution of the BTE.

1.3 Information on the execution of the project, use of available funds and (where appropriate) any changes to the original project plan relating to the following:

The project started in March 2012 and ended in February 2017. It was extended for 24 months, resulting in a 5 years project. Dr. Stanislav Tyaginov was employed on the project for nearly the first two years and then continued to supervise a range of PhD students who took over the main work. The first PhD student was Oliver Triebel who focused on the modeling of hot-carrier degradation in high-voltage devices and defended his doctoral thesis in November 2012. Then, Yannick Wimmer continued to work on HCD in high-voltage devices and extended our activities towards *ab-initio* (DFT) modeling of the Si-H bond breakage mechanism to solidify the theoretical basis of our model; his PhD defense is planned for autumn 2017. An additional post-doc, Wolfgang Gös, contributed towards a better understanding of the microscopic nature of charge transfer with interface defects. During the final stages of the project the PhD students Bianka Ullmann and Bernhard Stampfer conducted experiments to further validate the model. For this purpose a dedicated small cryogenic probe station was acquired to challenge the model over a wider temperature range.

2. Personnel development – Importance of the project for the research careers of those involved (including the project leader)

The project leaders' scientific track record was broadened through the research conducted in this project, strengthening the international standing of the group.

The main share of the project money was spent on the post-doc researcher Stanislav Tyaginov with over 100k Euro. The work and results of Dr. Tyaginov allowed him to become better known in the reliability/semiconductor device communities and establish/improve contacts with collaborators from imec, ams AG, Infineon, and the group of Prof. Jungemann, RWTH Aachen. Experience gained

within this project allowed him to contribute into the FP7 project Athenis_3D as well as to the FWF project No. P26382 “Single-Trap Characterization Methodology for Nanoscale MOSFETs”. Dr. Wolfgang Gös, accepted a job at SILVACO in Vienna where his focus is physics-based modeling of reliability issues. Based on results obtained in this project, Oliver Triebel has defended his PhD thesis. Experience gained in this project allows Bianka Ullmann to successfully work on the adjacent FWF project P26382 devoted to the single-trap perspective of HCD; her PhD defense is planned for 2017. All researchers employed from this project benefitted from the multitude of activities pursued during these years and from solving the very complex problem of hot-carrier degradation. In particular, interactions with other disciplines in the field of semiconductor physics, physics of semiconductor devices, and materials science were required to broaden the scope of all researchers involved.

3. Effects of the project beyond the scientific field

The research conducted within this project was held in tight collaboration with the carrier transport group of our institute which developed the simulator ViennaSHE (FWF project No. P23598). ViennaSHE is, in full alignment with the targets of Open Research, available as open source. Within this collaboration, we provided feedback on the usability and possible improvements regarding the numerical stability. Based on this feedback, additional features and physical models were implemented in ViennaSHE.

4. Other important aspects (examples)

The results of our research activities were disseminated at several acknowledged international conferences, which include, but are not limited to, the International Electron Device Meeting (IEDM), International Reliability Physics Symposium (IRPS), European Solid-State Device Research Conference (ESSDERC), International Integrated Reliability Workshop (IIRW), International Conference on Simulation of Semiconductor Processes and Devices (SISPAD). Dr. Tyaginov was invited to serve on the technical program committee and later on the management committee of IIRW. In 2012 he gave a tutorial on hot-carrier degradation modeling at the IIRW. A full list of talks at conferences is available in the next section; the most important for this project are:

- [1] S. Tyaginov, T. Grasser (tutorial): “Modeling of Hot-Carrier Degradation: Physics and Controversial Issues”, Proc. International Integrated Reliability Workshop (IIRW-2012)”, pp. 206 – 215 (2012), DOI: 10.1109/IIRW.2012.6468962
- [2] M. Bina, K. Rupp, S. Tyaginov, O. Triebel, T. Grasser: “Modeling of Hot Carrier Degradation Using a Spherical Harmonics Expansion of the Bipolar Boltzmann Transport Equation”; Proc. International Electron Devices Meeting (IEDM-2012), pp. 713 – 716 (2012), DOI: 10.1109/IEDM.2012.6479138
- [3] Y. Illarionov, S. Tyaginov, M. Bina, T. Grasser, “A Method to Determine the Lateral Trap Position in Ultra-Scaled MOSFETs”, Proc. Solid State Devices and Materials Conference (SSDM-2013), pp. 728 – 729 (2013), DOI: 10.7567/SSDM.2013.D-4-4

- [4] S. Tyaginov, M. Bina, J. Franco, D. Osintsev, O. Triebel, B. Kaczer, T. Grasser, "Physical Modeling of Hot-Carrier Degradation for Short- and Long-channel MOSFETs", Proc. International Reliability Physics Symposium (IRPS-2014), pp. XT 16.1-13.8 (2014), DOI: 10.1109/IRPS.2014.6861193
- [5] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, D. Osintsev, B. Kaczer, T. Grasser, "A Predictive Physical Model for Hot-Carrier Degradation in Ultra-Scaled MOSFETs", Proc. International Conference on Simulation of Semiconductor Processes and Devices (SISPAD-2014), pp. 89-92 (2014), DOI: 10.1109/SISPAD.2014.6931570
- [6] Y. Wimmer, S. Tyaginov, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.M. Park, R. Minixhofer, H. Ceric, T. Grasser, "Physical Modeling of Hot-Carrier Degradation in nLDMOS Transistors", Proc. International Reliability Workshop (IIRW-2014), pp. 58-62 (2014), DOI:10.1109/IIRW.2014.7049511
- [7] P. Sharma, S. Tyaginov, Y. Wimmer, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.M. Park, H. Ceric, T. Grasser, "Predictive and Efficient Modeling of Hot-Carrier Degradation in nLDMOS Devices", Proc. 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD-2015), pp. 389-392 (2015), DOI: 10.1109/ISPSD.2015.7123471
- [8] B. Ullmann, M. Jech, S. Tyaginov, M. Watzl, Y. Illarionov, A. Grill, K. Puschkarsky, H. Reisinger, T. Grasser, "The Impact of Mixed Negative Bias Temperature Instability and Hot Carrier Stress on Single Oxide Defects", Proc. International Reliability Physics Symposium (IRPS-2017), pp. XT-10.1-XT-10.6, DOI: 10.1109/IRPS.2017.7936424

III. Attachments

1. Scholarly / scientific publications

Peer-reviewed publications / already published (journals, monographs, anthologies, contributions to anthologies, proceedings, research data, etc.)

- [1] S. Tyaginov, I. Starkov, O. Triebel, M. Karner, C. Kernstock, C. Jungemann, H. Enichlmair, J.M. Park, T. Grasser: "Impact of Gate Oxide Thickness Variations on Hot-Carrier Degradation", Proc. 19th International Symposium on the Physical & Failure Analysis of Integrated Circuits (IPFA-2012), 2012, pp. 1 – 5, DOI:10.1109/IPFA.2012.6306265
- [2] M. Bina, K. Rupp, S. Tyaginov, O. Triebel, T. Grasser: "Modeling of Hot Carrier Degradation Using a Spherical Harmonics Expansion of the Bipolar Boltzmann Transport Equation"; Proc. International Electron Devices Meeting (IEDM-2012), 2012, pp. 713 – 716, DOI: 10.1109/IEDM.2012.6479138
- [3] S. Tyaginov, T. Grasser, tutorial: "Modeling of Hot-Carrier Degradation: Physics and Controversial Issues", Proc. International Integrated Reliability Workshop (IIRW-2012)", 2012, pp. 206 – 215 (2012), DOI: 10.1109/IIRW.2012.6468962
- [4] S. Tyaginov, M. Bina, J. Franco, D. Osintsev, Y. Wimmer, B. Kaczer, T. Grasser: "Essential Ingredients for Modeling of Hot-Carrier Degradation in Ultra-Scaled MOSFETs"; Proc. International Reliability Workshop (IIRW-2013), 2013, pp. 98 – 101, DOI:10.1109/IIRW.2013.6804168
- [5] Y. Illarionov, S. Tyaginov, M. Bina, T. Grasser, "A method to determine the lateral trap position in ultra-scaled MOSFETs", Proc. Solid State Devices and Materials Conference (SSDM-2013), 2013, pp. 728 – 729, DOI:10.7567/SSDM.2013.D-4-4
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- [7] S. Tyaginov, Y. Illarionov, M. I. Vexler, M. Bina, J. Cervenka, J. Franco, B. Kaczer, T. Grasser: "Modeling of deep-submicron silicon-based MISFETs with calcium fluoride dielectric", Journal of Computational Electronics, v. 13, No. 2, 733 – 738 (2014) [OA]
- [8] Y. Illarionov, S. Tyaginov, M. Bina, K. Rott, H. Reisinger, B. Kaczer, and T. Grasser, "A Reliable Method for the Extraction of the Lateral Position of Defects in Ultra-scaled MOSFETs", Proc. International Reliability Physics Symposium (IRPS-2014), 2014, pp. XT 13.1-13. DOI:10.1109/IRPS.2014.6861190
- [9] S. Tyaginov, M. Bina, J. Franco, D. Osintsev, O. Triebel, B. Kaczer, T. Grasser, "Physical Modeling of Hot-Carrier Degradation for Short- and Long-channel MOSFETs", Proc. International Reliability Physics Symposium (IRPS-2014), 2014, pp. XT 16.1-13.8, DOI:10.1109/IRPS.2014.6861193

- [10] S. Tyaginov, M. Bina, J. Franco, B. Kaczer, T. Grasser, "On the Importance of Electron-electron Scattering for Hot-carrier Degradation", International Conference on Solid State Devices and Materials (SSDM-2014), 2014, p. 858
- [11] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, D. Osintsev, B. Kaczer, T. Grasser, "A Predictive Physical Model for Hot-Carrier Degradation in Ultra-Scaled MOSFETs", Proc. International Conference on Simulation of Semiconductor Processes and Devices (SISPAD-2014), 2014, pp. 89-92, DOI:10.1109/SISPAD.2014.6931570
- [12] Y. Wimmer, S. Tyaginov, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.M. Park, R. Minixhofer, H. Ceric, T. Grasser, "Physical Modeling of Hot-Carrier Degradation in nLDMOS Transistors", Proc. International Reliability Workshop (IIRW-2014), 2014, pp. 58-62, DOI:10.1109/IIRW.2014.7049511
- [13] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, F. Rudolf, H. Enichlmair, J.M. Park, B. Kaczer, H. Ceric, T. Grasser, "Dominant Mechanism of Hot-Carrier Degradation in Short- and Long-Channel Transistors", Proc. International Reliability Workshop (IIRW-2014), 2014, pp. 63-68 (2014), DOI:10.1109/IIRW.2014.7049512
- [14] S. Tyaginov, Y. Wimmer, T. Grasser, invited: "Modeling of Hot-Carrier Degradation Based on Through Carrier Transport Treatment", Facta Universitatis v. 27, No. 4, 2014, pp. 479-508
- [15] P. Sharma, S. Tyaginov, Y. Wimmer, F. Rudolf, H. Enichlmair, J.M. Park, H. Ceric, T. Grasser, "A Model for Hot-Carrier Degradation in nLDMOS Transistors Based on the Exact Solution of the Boltzmann Transport Equation Versus the Drift-Diffusion Scheme", Proc. Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS 2015), 2015, p. 21-24, DOI: 10.1109/ULIS.2015.7063763
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- [18] P. Sharma, M. Jech, S. Tyaginov, F. Rudolf, K. Rupp, H. Enichlmair, J.M. Park, T. Grasser, "Modeling of Hot-Carrier Degradation in LDMOS Devices Using a Drift-Diffusion Based Approach", Proc. International Conference on Simulation of Semiconductor Processes and Devices (SISPAD-2015), 2015, pp. 60-63, DOI: 10.1109/SISPAD.2015.7292258

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2. Development of collaborations

N				Nationality of collaboration partner (please use the ISO-3-letter country code)
	G			Gender F (female) M (male)
		E		Extent E1 low (e.g. no joint publications, but mention in acknowledgements or similar); E2 medium (collaboration e.g. with occasional joint publications, exchange of materials or similar, but no longer-term exchange of personnel); E3 high (extensive collaboration with mutual hosting of group members for research stays, regular joint publications, etc.)
			D	Discipline W within the discipline (within the same scientific field) I interdisciplinary (involving two or more disciplines) T transdisciplinary (collaborations outside the sciences)



N	G	E	D	Name	Institution
GER	M	E2	I	Prof. Christoph Jungemann, PhD students Dominic Jabs and Hamed Kamrani	RWTH Aachen: our long-term partner in carrier transport modeling; they provide support in transport modeling and model calibration/validation.
BEL	M	E3	W	Drs. Ben Kaczer and Jacopo Franco	imec (Leuven): our main partner in HCD modeling; they provide experimental data, samples, and inspiration.
AUT	M	E3	W	Drs. Rainer Minixhofer, Ewald Wachmann, Ehrenfried Seebacher, Hubert Enichlmair, and Jong-Mun Park	ams AG: our long-term partner in HCD modeling for high-voltages devices; experimental data and samples.
AUT	M	E2	W	Dr. Gregor Pobegen	Infineon, KAI (Villach): long-term collaboration in HCD modeling in high-voltage devices; experimental support and samples.
GER	M/W		W	Dr. Hans Reisinger, PhD students Gunnar Rott and Katja Puschkarsky	Infineon (München): long-term collaboration in HCD modeling in high-voltage devices; experimental support and samples.
RUS	M	E2	I	Prof. Mikhail Vexler	loffe Physical-Technical Inst., Russian Academy of Sciences:

N G E D Name

Institution

GER	M	E2	I	Prof. Christoph Jungemann, PhD students Dominic Jabs and Hamed Kamrani	RWTH Aachen: our long-term partner in carrier transport modeling; they provide support in transport modeling and model calibration/validation.
					collaboration in transport and tunneling modeling.
USA	M	E2	I	Dr. Stewart Rauch	Globalfoundries: collaboration in compact modeling of HCD.

3. Development of human resources in the course of the project

	In progress	Completed	Gender	
			f	m
Full professorship				
<i>Venia</i> thesis (<i>Habilitation</i>) / Equivalent senior scientist qualification	1			1
Postdoc		2		2
Ph.D. theses	3	1	1	3
Master's theses				
Diploma theses				
Bachelor's theses				

4. Applications for follow-up projects

4.1 Applications for follow-up projects (FWF projects)

Please indicate the project type (e.g. stand-alone project, SFB, DK, etc.)

Project number (if applicable)	P26382		
Project type	Stand-alone Project		
Title / subject	Single-Trap Characterization Methodology for Nanoscale MOSFETs		
Status	granted <input checked="" type="checkbox"/>	pending <input type="checkbox"/>	in preparation <input type="checkbox"/>
Application reference (if a patent is applied)			

4.2 Applications for follow-up projects (international projects) (e.g. EU, ERC or other international funding agencies)

Country	Austria		
Funding agency	Please choose an item: EU		
Project number (if applicable)	619246 ATHENIS_3D		
Project type	FP7 programme		
Title / subject	Automotive Tested High Voltage and Embedded Non-Volatile Integrated System on Chip Platform Employing 3D Integration		
Status	granted <input checked="" type="checkbox"/>	pending <input type="checkbox"/>	in preparation <input type="checkbox"/>
Total costs (granted)	446,096€		

Country	Austria		
Funding agency	Please choose an item: EU		
Project number (if applicable)	619234 MoRV		
Project type	FP7 programme		
Title / subject	Modelling Reliability under Variability		
Status	granted <input checked="" type="checkbox"/>	pending <input type="checkbox"/>	in preparation <input type="checkbox"/>
Total costs (granted)	370,500€		

IV. Cooperation with the FWF

Scale:
 -2 highly unsatisfactory
 -1 unsatisfactory
 0 appropriate
 +1 satisfactory
 +2 highly satisfactory
 X not used

Rating

Application guidelines	Length	+1
	Clarity	+1
	Intelligibility	+1

Procedures (submission, review, decision)

	Advising	+1
	Duration of procedure	0
	Transparency	0

Project support

Advising	Availability	+1
	Level of detail	+1
	Intelligibility	+1

Financial transactions (credit transfers, equipment purchases, personnel management)		+1
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Reporting / review / exploitation

	Effort	+1
	Transparency	+1
	Support in PR work / exploitation	0

Comments on cooperation/interaction with the FWF:

The FWF provided timely feedback during the project and managed our requests highly satisfactory. We thank the FWF for the given opportunity and would like to express our gratitude for letting us focus on research rather than the usual administrative and bureaucratic overhead.