EXACT FIRST PRINCIPLES MODELLING OF SHORT-CHANNEL VMOS TRANSISTORS

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1. INTRODUCTION

The application of exact two-dimensional numerical computer models has found wider use during the past few years. As far as we know these models have been totally limited to simple planar structures. Recently VMOS technology has turned the technology challenge to simple planar MOS in the field of large scale static and dynamic memory devices. The use of the third dimension makes it possible to increase circuit complexity up to 64k RAM memory chips.

In this contribution we present a method and some important results of a two-dimensional exact model for VMOS devices. To gain maximum insight into the influence of the technological and the geometrical variations the modelling of both the technology and the electrical behaviour of the devices have been coupled. This has been performed using a one-dimensional process model and a two-dimensional device model.

2. METHOD AND RESULTS

The structures investigated are transistors which are used for one-transistor dynamic memory cells (e.g. (1)). The doping profile of a typical VMOS device before the selective etching process is shown in fig.1. The transistor is made on a p+ substrate. The n+ buried source is an antimony diffused layer. The channel region is made by p epitaxy. The drain regions are highly phosphorus doped. The channel VMOS devices of a 64k RAM is simulated. Appropriate reduction of geometrical variations. Theory and experiment agree well for all operating conditions down scaled VMOS device. An appropriate reduction of geometrical variations. Theory and experiment agree well for all operating conditions down scaled VMOS device. An appropriate reduction of geometrical variations. Theory and experiment agree well for all operating conditions down scaled VMOS device. An appropriate reduction of geometrical variations. Theory and experiment agree well for all operating conditions. The validity and predictability of our two-dimensional model have been tested with a down scaled VMOS device. An appropriate reduction of geometrical variations. Theory and experiment agree well for all operating conditions. The validity and predictability of our two-dimensional model have been tested with a down scaled VMOS device. An appropriate reduction of geometrical variations. Theory and experiment agree well for all operating conditions.

Due to the lack of space only two results can be given here. The computed profiles have been presented in fig. 1. The channel length L, oxide thickness Tox, and p+ junction depth Rj are also defined. Table 1 lists the complete set of the non-stationary basic semiconductor equations. Heat transfer is included to give complete device simulation at higher current levels. Nearly all of the quantities have their usual meaning. K and s are the heat constant and the density of silicon, respectively. C denotes the specific heat constant. Table 2 shows the data of the transistors investigated. The drain voltage dependence of the threshold voltage is shown in fig. 3. The substrate to source voltage is taken as a parameter. The squares denote the measured points and the full drawn lines give the computer results. Experimentally the threshold voltage has been determined by the extrapolation method. In the saturation region we use the square-root technique and in the ohmic range the curves can be simply extrapolated. Numerically the threshold voltage has been found by use of the inversion criterion at the semiconductor surface. Due to the relatively high substrate doping short channel effects become only visible at the most negative substrate voltage of -8V and higher drain bias. At low drain voltages (between 0.1 and 1V) the threshold voltage shows the same dependence on the substrate voltage as simple planar MOS structures. A more accurate study of VMOS devices can be carried out if one looks at the substrate current behaviour. Fig. 4 shows the substrate current of the short channel device depending on the gate voltage. Circles denote computer results. The substrate current has been measured in the bulk lead of the device. Numerically it is calculated by an integration over the hole distribution. In the saturation region the substrate current shows an exponential dependence on the drain voltage according to an avalanche process which has been exactly modelled with the inclusion of the avalanche generation. The curves reach a maximum value and fall down if the device comes back into the ohmic range. The validity and predictability of our two-dimensional model have been tested with a down scaled VMOS device. An appropriate reduction of junction depths and voltage levels lead to a 4x4x4 VMOS pyramid element. A design based on this device could realize a 256k RAM. Due to the lack of space only two results can be given here.

Fig. 5 shows the behaviour of the carrier densities when the device is switched from deep inversion to accumulation. Fig. 6 depicts the isothermal lines in the device for a high current situation. The maximum internal temperature is calculated to be about 415K at the boundary between channel region and pinch-off area.

3. CONCLUSIONS

The static and dynamic behaviour of short channel VMOS devices of a 64k RAM is simulated estimating the influence of technological and geometrical variations. Theory and experiment agree well for all operating conditions down to 0.7µm channel length. Short channel devices in the limit of punch-through and avalanche conditions are characterized with an error smaller than 30 percent. In the same way a down scaled VMOS transistor is simulated. Appropriate reduction of geometrical dimensions and voltage levels leads to a 4x4x4 VMOS element. A design based on this device could realize a 256k RAM.
4. REFERENCES


**TABLE 1 - Basic Equations**

Poisson Equation: \[ \nabla^2 \phi = -\frac{q}{\varepsilon} (p-n+C) \]

Continuity Equations:
\[ \nabla \cdot J_p = -q \left( R - G + \frac{2p}{\varepsilon t} \right) \]
\[ \nabla \cdot J_n = q \left( R - G + \frac{2n}{\varepsilon t} \right) \]

Heat Transfer: \[ \nabla \cdot (K \nabla T) = -Q + \rho c \frac{dT}{dt} \]

**TABLE 2 - VMOS transistor data**

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>( p^+ ) substrate doping</td>
<td>( 10^{18} \text{cm}^{-3} )</td>
</tr>
<tr>
<td>( n^+ ) buried source</td>
<td>70 \text{ohm/square}</td>
</tr>
<tr>
<td>( p ) epitaxy</td>
<td>( 1.5 \times 10^{16} \text{cm}^{-3} )</td>
</tr>
<tr>
<td>( n^+ ) drain</td>
<td>15 \text{ohm/square}</td>
</tr>
<tr>
<td>oxide thickness</td>
<td>550 \AA</td>
</tr>
<tr>
<td>epilayer thickness</td>
<td>4 \text{µm}</td>
</tr>
<tr>
<td>source thickness</td>
<td>2.5 \text{µm}</td>
</tr>
<tr>
<td>drain junction depth</td>
<td>1.3 \text{µm}</td>
</tr>
<tr>
<td>channel length</td>
<td>1.6 \text{µm}</td>
</tr>
<tr>
<td>channel width</td>
<td>10 \text{µm} (5 \text{µm pyramid})</td>
</tr>
<tr>
<td>mobility</td>
<td>120 \text{cm}^2/\text{Vsec}</td>
</tr>
</tbody>
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Fig. 1: Doping profile of a VMOS transistor before etching.
- (o) 4-point probe,
- (+) 2-point probe,
- (o) computer corrected 2-point probe,
- (-) SUPREM I.

Two-dimensional cross section of a typical VMOS device with a floating source. The dashed lines show the planar generalization used in the numerical computations.
Fig. 3: Threshold voltage behaviour in dependence of drain voltage and substrate voltage. (o) theory, (−) experiment.

Fig. 4: Substrate current in dependence on gate voltage with drain bias as a parameter. (o) theory, (−) experiment.

Fig. 5: Behaviour of carrier densities during switch-off conditions. (−) electrons, (−−) holes, \( U_D(t=0) = 2 \) \( \text{V} \), pulse height \(-2\) \( \text{V} \), rise time 100 psec.

Fig. 6: Isothermal lines at \( U_G = 15 \) \( \text{V} \), \( U_D = 5 \) \( \text{V} \), \( U_{\text{SUB}} = -2 \) \( \text{V} \).