CHARACTERIZATION OF $IN_{0.12}AL_{0.88}N$/GAN HEMTS AT ELEVATED TEMPERATURES SUPPORTED BY NUMERICAL SIMULATION

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ABSTRACT

With the innovation of GaN-based structures and the development of fabrication processes, there are many issues, e.g. current collapse or self-heating effects, which must be addressed. In this work, the DC device behaviour at 300K and at elevated temperatures is studied both experimentally and by means of two-dimensional device simulations. Very good agreement between measurements and simulations with Minimos-NT is achieved using the hydrodynamic transport model including self-heating and impact ionization effects.

1. INTRODUCTION

GaN-based HEMTs attract strong attention due to their material-related properties, such as wide bandgap, high carrier saturation velocity, thermal conductivity, and breakdown field, which are required for high-temperature, high-power, and high-speed applications [1]. Important usages include micro- and millimeter-wave power amplification and power switching [2], where maintaining efficiency at high power is a challenge, and is thought to be limited by parasitic thermal effects [3].

2. DEVICE STRUCTURE AND MODELING

The investigated HEMT device structure is schematically depicted in Fig.6. It consists of a 300nm thick AlN layer grown on the 6H-SiC substrate followed by a 2.5µm GaN buffer layer with a 1nm AlN spacer layer and a 7nm $In_{0.12}Al_{0.88}N$ barrier layer on top. The gate-to-drain and the gate-to-source distances are 4.8µm and 1.6µm, respectively, while the gate length is 1.6µm. The device width is 400µm and there is no passivation. More details about the device fabrication process are reported in [4].
Two-dimensional hydrodynamic numerical device simulations are performed by Minimos-NT [5,6]. Self-heating effects are accounted for by the lattice heat flow equation. The sum of polarization charges at the AlN interfaces equals the polarization charge at the InAlN/GaN interface [7]. Thus, the AlN/InAlN barrier system is represented by an 8nm thick InAlN in the model. Well-calibrated two-valley electron mobility and bandgap energy models are also implemented in the simulator [5]. Due to the divergence of the polarization fields at the InAlN/GaN heterointerface, a two-dimensional electron gas (2DEG) is formed in the quantum well with a density $n_{2DEG}=2.6\times10^{13}$ cm^{-2}. The interface between the GaN buffer layer and the AlN nucleation layer is described by a value of polarization charge $\sigma = -2.5\times10^{11}$ cm^{-2}.

Performing hydrodynamic simulations with self-heating, we introduce a substrate thermal contact (Fig.6). We obtain the best agreement with experimental data by using a thermal contact resistance $R_{th}=10^{-3}$Kcm^{-2}/W. This value lumps the thermal resistance of the nucleation layer and the SiC substrate, and possible three-dimensional thermal effects [8]. The R_{th} value nicely coincides with that obtained from optical measurements [9]. An impact ionization model, based on Monte Carlo simulation results [10], was developed and used in Minimos-NT.

3. RESULTS AND DISCUSSION

I-V measurements were performed using an accurate, fully automated parameter analyzer Agilent 4155C and a thermal chuck where the temperatures are set with an accuracy of 0.1K. Three device samples were measured in the relevant temperature range between 300K and 450K. The device exhibits a threshold voltage of about -2.5V. Figs.1-4 show comparisons of measured and simulated output device characteristics for a V_{GS} sweep from -2V to 1V at 300K, 350K, 400K, and 450K, respectively. Very good agreement between measurements and simulations with Minimos-NT is achieved using the hydrodynamic transport model including self-heating and impact ionization effects up to 400K, while for 450K some discrepancies were observed, which demand deeper investigation. For low drain biases the decrease of drain current with temperature is mostly caused by the reduction of the low-field electron mobility, which follows a power law with power -1.5. For high drain biases self-heating plays a role too. Fig.5, gives the drop of the drain current with increasing temperature at V_{DS}=10V for different gate biases. The peak temperature in the device varies between 380K (for 300K at the substrate) to 500K (for 450K), see Fig.6.

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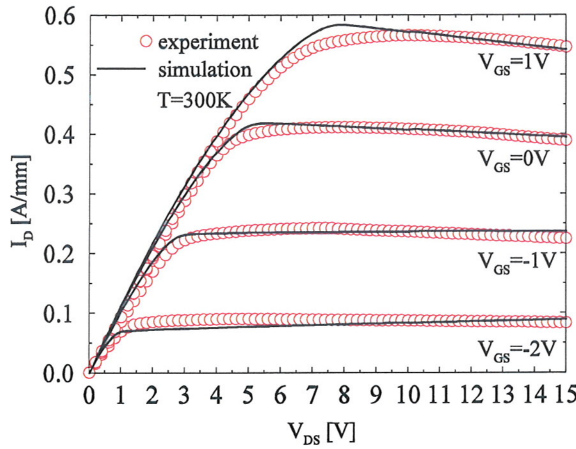

Fig. 1: Measured and simulated output characteristics at 300K and for a V_{GS} sweep from -2V to 1V.

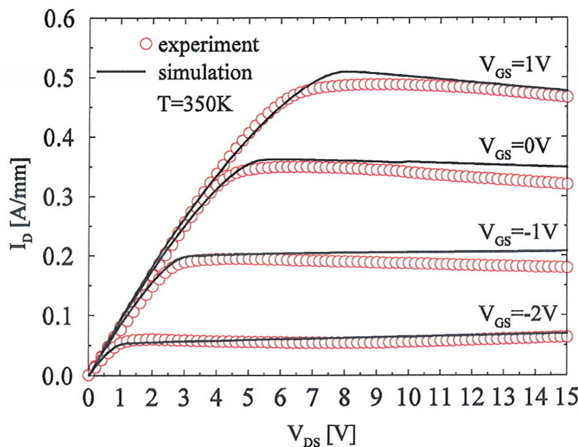

Fig. 2: Measured and simulated output characteristics at 350K and for a V_{GS} sweep from -2V to 1V.

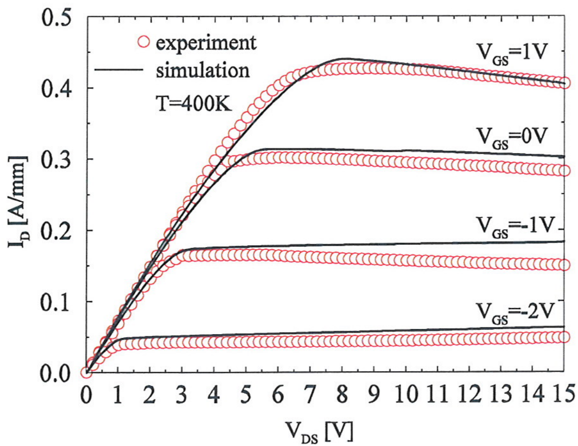

Fig. 3: Measured and simulated output characteristics at 400K and for a V_{GS} sweep from -2V to 1V.

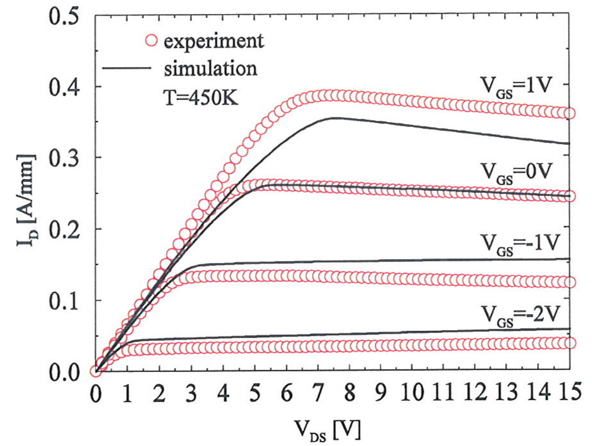

Fig. 4: Measured and simulated output characteristics at 450K and for a V_{GS} sweep from -2V to 1V.

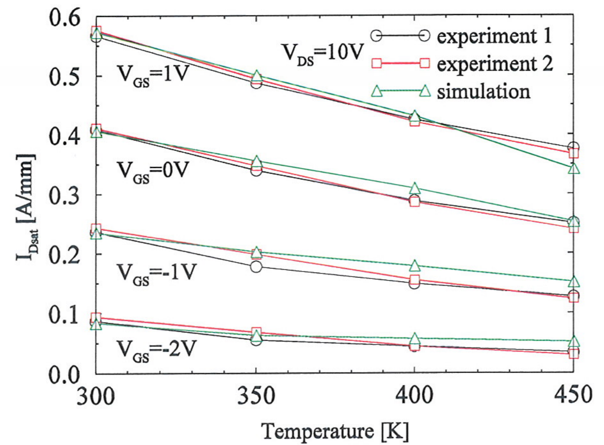

Fig. 5: Measured and simulated drain current vs. temperature for V_{DS}=10V and a V_{GS} sweep from -2V to 1V.

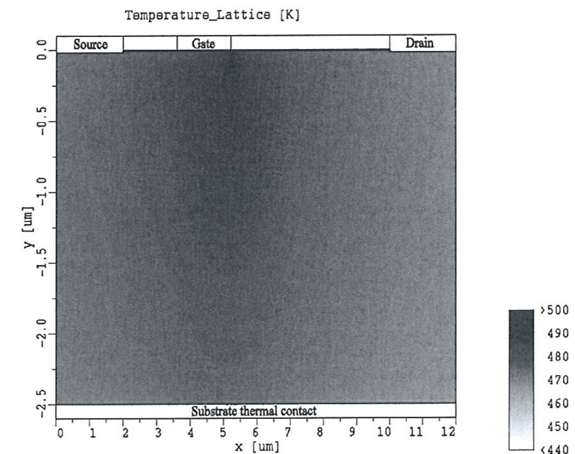

Fig. 6: Lattice temperature map for substrate temperature 450K and for V_{DS}=10V and V_{GS}=1V.

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