MRAM-based Logic Array for Large-Scale Non-Volatile Logic-in-Memory Applications

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***Abstract*— A novel non-volatile logic-in-memory (NV-LIM) architecture is introduced to extend the functionality of the spin-transfer torque magnetoresistive random-access memory (STT-MRAM) to include performing logic operations with no extra hardware added. The access transistors of the one-transistor/one-magnetic tunnel junction (1T/1MTJ) cells are used as voltage-controlled resistors. This provides the structural asymmetry required for realizing a fundamental Boolean logic operation called material implication and inherently realizes a NV-LIM architecture which uses MTJs as the main computing elements (logic gate).**

I. Introduction

Spin-transfer torque magnetoresistive random-access memory (STT-MRAM) is one of the most promising candidates for the next-generation of non-volatile memory due to its unlimited endurance, CMOS compatibility, fast switching speed, and excellent scalability [1]. The one-transistor/one-magnetic tunnel junction (1T/1MTJ) structure shown in Fig. 1a constitutes the basic cell of the STT-MRAM architecture [2] in which the access transistor selects and controls the current flow through the MTJ for reading and (STT) writing. We demonstrate that by using the access transistor as a voltage-controlled resistor; the functionality of the STT-MRAM cells can be extended to perform logic operations with no extra hardware needed. This abolishes the standby power issue, which has become a top concern due to high leakage currents as CMOS technology is shrunk [3] by providing non-volatile logic-in-memory functionality.

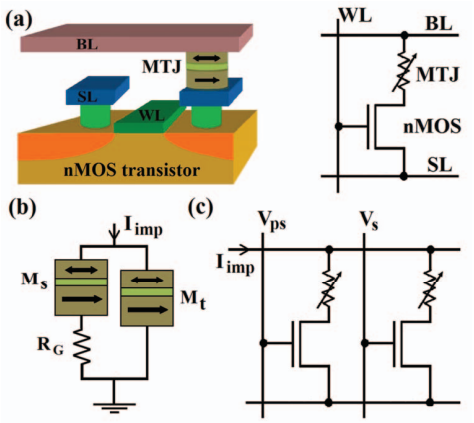

Fig. 1. (a) Structure and equivalent circuit of 1T/1MTJ cell. (b) Current-controlled MTJ-based IMP logic gate [3] including source (M_s), target (M_t) MTJs. (c) Proposed MRAM-based IMP logic gate. By applying V_{ps} (V_s) to a word line the source (target) MTJ is selected.

II. MRAM-based Logic Array

In [4] we presented a novel circuit topology (Fig. 1b) for MTJ-based logic relying on a structural asymmetry caused by the resistor R_G, which induces a conditional switching behavior on the target MTJ (M_t). The realized logic depends on the initial resistance state of the MTJs and corresponds to the fundamental Boolean operation called material implication (IMP). The logic state variables are represented by the resistance states of the MTJs acting as logical input (s and t) and output (t') for binary data. However, for this topology (Fig. 1b) - due to (not) being serially connected to R_G - M_s (M_t) is useable only as an input (output) MTJ which makes the generalization of the IMP gate to a large-scale implication logic circuit problematic. This restriction is lifted in the topology shown in Fig. 1c by applying the current I_{imp} to the common bit line (BL) and selecting and pre-selecting voltages (V_s and V_{ps}) to two arbitrary word lines (WLs) simultaneously. Since the voltage level V_{ps} is lower than V_s the transistors have different channel resistances, therefore the structural asymmetry required for the IMP operation is provided by the pre-selected transistor exhibiting a higher resistance which acts as R_G (Fig. 1b).

The circuit parameters I_{imp}, V_s, and V_{ps} can be optimized to minimize the IMP error (P_{Err}) as shown in Fig. 2. According to the IMP truth table [5], P_{Err} is defined as a function of the undesired switching probabilities (P_u) and the term 1-P_d for the desired switching events as

$$E_{imp} = 1\text{-}P_d(t_1) + P_d(t_1)\,P_u(s_1) + P_u(s_2) + P_u(t_3), \quad (1)$$

where $P(t_i)$ is the switching probability of M_t in State i of the IMP truth table and is given for the thermally activated switching by [2]

$$P = 1\text{-}\exp\{-\tau/\tau_0 \exp[-\Delta(1-I_C/I_M)]\}. \quad (2)$$

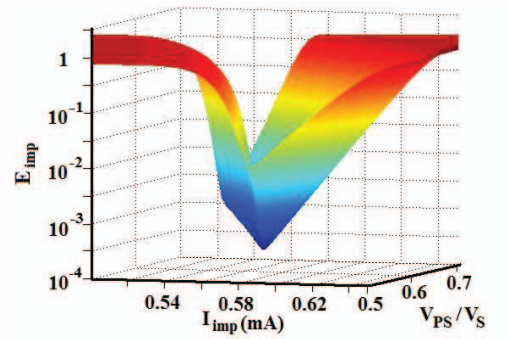

Fig. 2. Circuit parameters (I_{imp} and V_{ps}/V_s) optimization for minimum IMP gate error probability.

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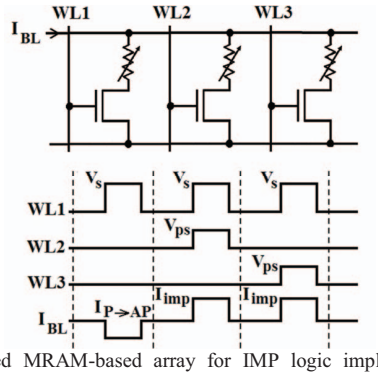

Fig. 3. Proposed MRAM-based array for IMP logic implementation and required circuit signals for performing universal NOR operation in three steps.

Δ is the thermal stability factor, τ is the pulse width (>10 ns), τ_0 is 1ns, I_C is the critical switching current extrapolated to 1ns, and I_M is the current following through the MTJ. In order to calculate the current flowing through each MTJ in the MRAM-based array, we use (3) for modeling the voltage-dependent effective TMR [6] and (4) for the channel resistance in the triode region when the transistor is on [7]:

$$R_{AP} = [1 - TMR_{eff}]\, R_P = [1+TMR/(1+ V_M/ V_C)]\, R_A \quad (3)$$

$$R_{on} = (L/W) / (\mu_n\, C_{ox}\, [V_{GS} - V_{TH}]). \quad (4)$$

TMR_{eff} (TMR) is the tunnel magnetoresistance ratio under non-zero (zero) bias voltage (V_M) and V_0 is the bias voltage equivalent to TMR_{eff} = 0.5 TMR. V_{GS} is the voltage applied to the word line (WL) of the 1T/1MTJ cell.

Fig. 3 shows the required circuit signals for the implementation of the universal NOR operation ($c_1 \leftarrow c_2$ NOR c_3) in three steps (one parallel-to-antiparallel (P→AP) switching and two implication operations [4] as shown in Table I) on three 1T/1MTJ cells (C_1, C_2, and C_3). Depending on the logical definition for AP and P states of the MTJ (AP≡'0' and P≡'1' or vice versa), the realized operation (IMP or negated IMP (NIMP)) in combination with False/True operation forms a computationally complete logic basis enabling arbitrary Boolean logic functions. Fig. 4 compares the energy consumption of IMP-based implementations of the basic Boolean logic operations.

From the MTJ device point of view, a higher TMR ratio provides a higher MTJ resistance modulation and increases the current modulation through the target MTJ required for conditional STT-switching behavior.

Table I: The truth table of performing the NOR operation ($c_1 \leftarrow c_2$ NOR c_3) in three steps including $c_1 \leftarrow$'1', $c'_1 \leftarrow c_1$ NIMP c_2, and $c''_1 \leftarrow c_1$ NIMP c_3. For the implicatin operations C_1 is used as the target cell and C_2 and C_3 remain unchanged because they act as the source cells for the operations.

	Initial state		Step 1	Step 2	Step 3
Case	c_2	c_3	c_1	c'_1	c''_1
1	P ('0')	P ('0')	AP ('1')	AP ('1')	AP ('1')
2	P ('0')	AP ('1')	AP ('1')	AP ('1')	P ('0')
3	AP ('1')	P ('0')	AP ('1')	P ('0')	P ('0')
4	AP ('1')	AP ('1')	AP ('1')	P ('0')	P ('0')

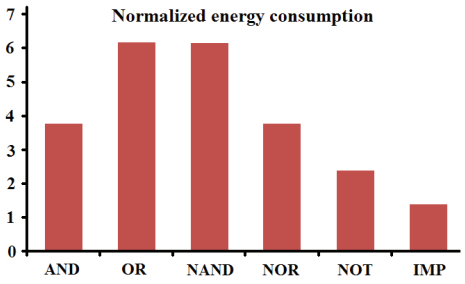

Fig. 4. The normalized energy consumption of IMP-based implementations of basic Boolean logic operations. The energy is normalized in the amount of that required for antiparallel-to-parallel MTJ switching ($E_{AP\rightarrow P}$).

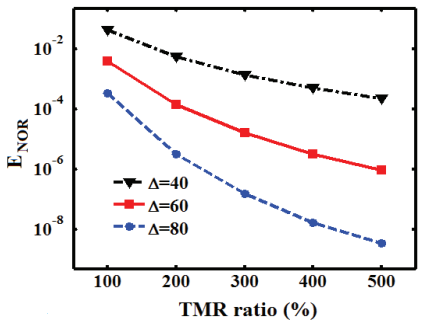

Fig. 5. The error probability for the universal NOR operation implemented based on the proposed MRAM logic array as a function of the TMR ratio plotted for different values of Δ and optimized circuit parameters.

A higher MTJ thermal stability Δ provides sharper switching dynamics [8]. Fig. 5 illustrates the error probability for the IMP-based NOR operation as a function of TMR for different values of Δ.

III. Conclusion

The presented 1T/1MTJ-based logic architecture uses the MTJs as input and output for logic computation. It is computationally complete, has a simple circuit structure (STT-MRAM), and eliminates the need for intermediate circuitry compared to previously proposed non-volatile logic-in-memory architectures [9]. Therefore, it is suited for large-scale integration of complex logic functions and opens an alternative path towards zero-standby power systems, shifting away from the Von Neumann architecture by eliminating the need for data transfer between separate memory and logic units.

Acknowledgment

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