Performance Analysis and Comparison of Two 1T/1MTJ-based Logic Gates

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***Abstract*—A performance analysis and comparison of two one-transistor/one-magnetic tunnel junction (1T/1MTJ)-based logic gates is presented. The energy consumption as well as the reliability of different Boolean logic functions utilizing the two circuit topologies are studied and the adequacy of their employment for specific non-volatile logic applications is discussed. It has been shown that the implication logic design exhibits a more reliable behavior compared to the reprogrammable logic design featuring conventional Boolean logic operations like (N)AND and (N)OR. Although the comparison between the two error optimized logic gate types shows that the fundamental logic operations with the reprogrammable gates require less energy than with the IMP gates, the situation reverses for more complex Boolean logic operations.**

I. Introduction

Because of scalability, unlimited endurance, fast switching speed, and CMOS compatibility [1], the spin-transfer torque magnetic tunnel junction (STT-MTJ) is a promising candidate for the replacement of the CMOS transistor, as the scaling of CMOS technologies becomes harder for every device generation [2], [3]. Recently, MTJ-based logic gates have been proposed which store logic variables as resistance states of the MTJs rather than voltage levels like in CMOS logic [4], [5], [6]. This extends non-volatile spintronics from sole memory applications to logic computation and provides zero-standby power computation. It also allows to shift away from the Von Neumann architecture by eliminating the need for data transfer between separate memory and logic units [7]. Due to easy integration with CMOS, MTJs can be placed within 1T/1MTJ cells (Fig. 1a) in an array to construct large-scale circuits performing complex logic functions, in which all MTJs can be used arbitrarily as input or output for the computations [8].

In this work we present a performance analysis and comparison of implication [5] (Fig. 1b) and reprogrammable [6] (Fig. 1d) logic gates based upon the 1T/1MTJ structure as shown in Fig. 1c and Fig. 1e, respectively. The implication gate implements a fundamental Boolean logic operation called material implication (IMP) and the reprogrammable gate realizes the more common Boolean logic operations AND, OR, NAND, and NOR. For this type of MTJ-based logic gates the logic (resistance) states of the input MTJs act as the logic inputs and provide a state dependent (conditional) STT switching behavior on a target MTJ (M_t in Fig. 1b and the output MTJ in Fig. 1d).

II. 1T/1MTJ Cell Modeling

Non-volatile MTJ-based logic relies on a conditional switching behavior of a target MTJ [5], [6]. Therefore, the reliability of an implemented logic operation is proportional to the product of the terms $(1-E_\mathrm{i})$ of all MTJs in the respective logic gate. E_i denotes the error probability of the i^{th} MTJ and is equal to the switching probability (S_i) of the corresponding MTJ when its logic state has to be left unchanged (an undesired switching event). For example, any switching event in M_s in the implication gate or in an input MTJ in the reprogrammable gate is an undesired event. However, for a desired switching event we have $E_\mathrm{i} = 1 - S_\mathrm{i}$. An example of a desired switching event in the implication gate is a high-to-low resistance switching in M_t when both M_s and M_t are initially in high resistance state (cf. Fig. 1b and Fig. 1c, [5]), according to the IMP truth table [9].

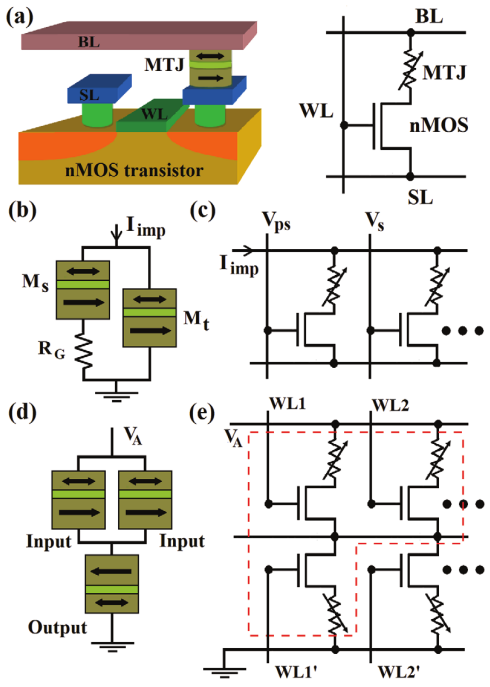

Fig. 1. (a) Structure and equivalent circuit of 1T/1MTJ cell. MTJ-based implication (b) [5] and reprogrammable (d) [6] logic gates. 1T/1MTJ-based realization of implication (c) and reprogrammable (e) logic gates.

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For a given input combination, the error probability of the respective intrinsic logic operation (f) implemented using the implication or the reprogrammable gate is given by

$$E(f) = 1 - \prod_{i=1}^{n} [1 - E_{\rm i}], \tag{1}$$

where n is the total number of the MTJs in the gate. Correct logic behavior of a logic operation is ensured, only when the logic gate has correct logic functionality for all possible input combinations. We further assume equal frequencies of occurrence for all input patterns, which allows us to use the average of $E(f)$ in our simulations.

According to the theoretical model [10] and the measurements [11], the switching probability (S) of an MTJ in the thermally-activated switching regime is given by

$$S_{\rm i} = 1 - \exp\left\{-\frac{t}{\tau_0}\exp\left[-\Delta\left(1 - \frac{I_{\rm i}}{I_{\rm C0}}\right)\right]\right\}, \tag{2}$$

where Δ is the MTJs thermal stability factor (=$E/k_{\rm B}T$ and E denotes the energy barrier between the magnetization states), $I_{\rm i}$ indicates the current flowing through the $i^{\rm th}$ MTJ, t is the current pulse duration, $\tau_0 \sim 1$ns, and $I_{\rm C0}$ represents the critical switching current extrapolated to τ_0 [12]. In order to calculate the current $I_{\rm i}$ for each MTJ, (3) and (4) are used to take into account the channel resistance of the access transistor [13] and the voltage-dependent MTJ resistance (effective TMR model [14]), respectively:

$$R_{\rm on} = \frac{V_{\rm DS}}{\mu_{\rm n} C_{\rm ox}\frac{W}{L}\left[(V_{\rm GS} - V_{\rm TH})V_{\rm DS} - \frac{V_{\rm DS}^2}{2}\right]}, \tag{3}$$

$$R_{\rm i} = (1 + {\rm TMR}_{\rm eff})\, R_{\rm P} = \left(1 + \frac{{\rm TMR}_0}{1 + \frac{V_{\rm i}^2}{V_{\rm h}^2}}\right) R_{\rm P}. \tag{4}$$

Here, $V_{\rm GS}$ ($V_{\rm DS}$) is the voltage difference between the gate (drain) and the source of the access transistor, $\mu_{\rm n}$ is the mobility of electrons, $C_{\rm ox}$ is the oxide thickness, and W (L) is the channel width (length). The transistors are supposed to operate in the triode (ohmic) region ($V_{\rm GS} > V_{\rm TH}$ and $V_{\rm DS} < V_{\rm GS} - V_{\rm TH}$). ${\rm TMR}_0$ (${\rm TMR}_{\rm eff}$) is the tunnel magnetoresistance (TMR) ratio under zero (non-zero) bias voltage ($V_{\rm i}$), and $V_{\rm h}$ is the bias voltage equivalent to ${\rm TMR}_{\rm eff} = {\rm TMR}_0/2$. Although the ON resistance of the access transistors decreases the effective TMR of the 1T/1MTJ cell by about 10% [15], the structural asymmetry restriction of the implication gate (Fig. 1b) due to $R_{\rm G}$ is lifted by the topology shown in Fig. 1c, where the access transistors are used as voltage-controlled resistors [8]. In fact, the IMP operation can be executed by applying the current $I_{\rm imp}$ to the common bit line (BL) and selecting and pre-selecting voltages ($V_{\rm s}$ and $V_{\rm ps}$) to two arbitrary word lines (WLs) simultaneously. As $V_{\rm ps} < V_{\rm s}$, the transistors have different bias points (Fig. 2) and thus exhibit different channel resistances. The circuit parameters $I_{\rm imp}$, $V_{\rm s}$, and $V_{\rm ps}$ in the implication gate and the voltage level $V_{\rm A}$ in the reprogrammable gate can be optimized to minimize their error

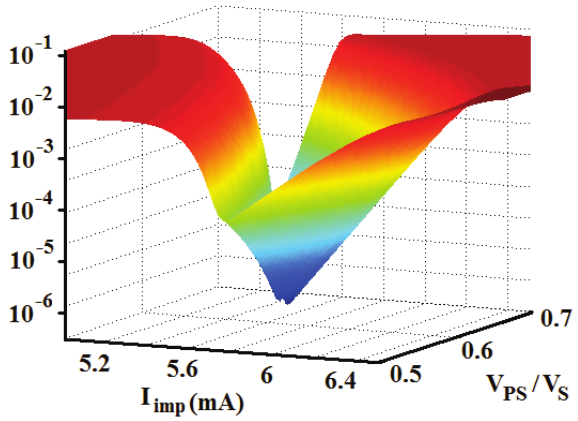

Fig. 3. Circuit parameters ($I_{\rm imp}$, $V_{\rm s}$, and $V_{\rm ps}$) optimization for minimum implication gate error probability with MTJs characterized by $R_{\rm P} = 1.8$kΩ, TMR= 3, and Δ =70.

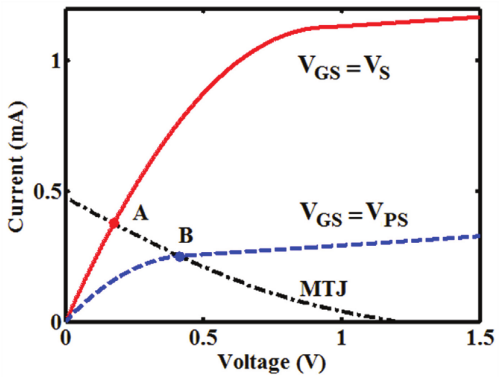

Fig. 2. Bias points of the access transistor in a 1T/1MTJ cell for the selecting (point A) and pre-selecting (point B) voltages applied to the word line of the cell.

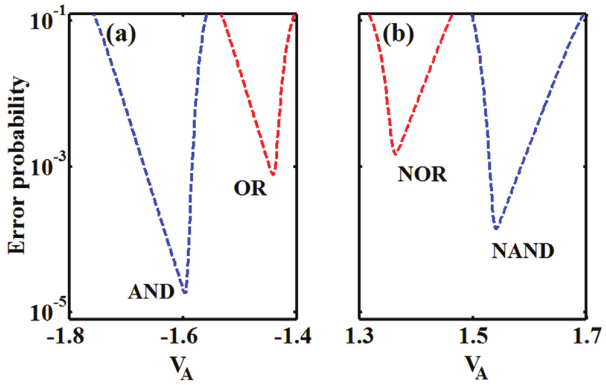

Fig. 4. Circuit parameter ($V_{\rm A}$) optimization for minimum reprogrammable gate error probability with MTJs characterized by $R_{\rm P} = 1.8$kΩ, TMR= 3, and Δ =70.

probabilities ($E(f)$) of each intrinsic operation (f) as shown in Fig. 3 and Fig. 4. According to the logical definitions for the MTJs' high ($R_{\rm AP}$) and low ($R_{\rm P}$) resistance states ($R_{\rm AP} \equiv$ "1" and $R_{\rm P} \equiv$ "0" or vice-versa), the intrinsic logic function executed by the implication gate is corresponding to the IMP or NIMP (negated IMP) operation [5]. In combination with low-to-high resistance switching, the implication operation forms a complete basis [9]. Therefore, any Boolean function can be implemented using implication logic without need for any other gate type. In order to be consistent with [6], we use the convention of Shannon ($R_{\rm AP} \equiv$ "1" and $R_{\rm P} \equiv$ "0"). Thus, the low-to-high resistance switching is equivalent to the TRUE operation and the realized intrinsic function by the implication logic corresponds to the NIMP operation.

III. Results and Discussion

As mentioned before, the IMP/NIMP operation is the intrinsic function of the implication gate in one step. Other logic functions are implemented by using subsequent FALSE/TRUE and IMP/NIMP operations [16]. For example, NOT and NOR operations can be performed in two and three steps as

$$a_2 \leftarrow \text{NOT } a_1 \equiv \{a_2 \leftarrow 1,\ a_2 \leftarrow a_1 \text{ NIMP } a_2\}, \tag{5}$$

$$a_3 \leftarrow a_1 \text{ NOR } a_2 \equiv \{a_3 \leftarrow 1,\ a_3 \leftarrow a_1 \text{ NIMP } a_3,\ a_3 \leftarrow a_2 \text{ NIMP } a_3\}. \tag{6}$$

For the reprogrammable gate the AND, OR, NAND, and NOR operations are the intrinsic logic functions implemented in two steps including a preset (TRUE or FALSE in the output MTJ) and a conditional switching provided by the voltage pulse $V_{\rm A}$. Any other logic function can be performed by using subsequent TRUE, FALSE, and intrinsic operations. For example, NOT and NOR operation can be executed as:

$$b_1 \leftarrow \text{NOT } a_1 \equiv \{a_2 \leftarrow 1,\ b_1 \leftarrow 0,\ b_1 \leftarrow a_1 \text{ NAND } a_2\} \tag{7}$$

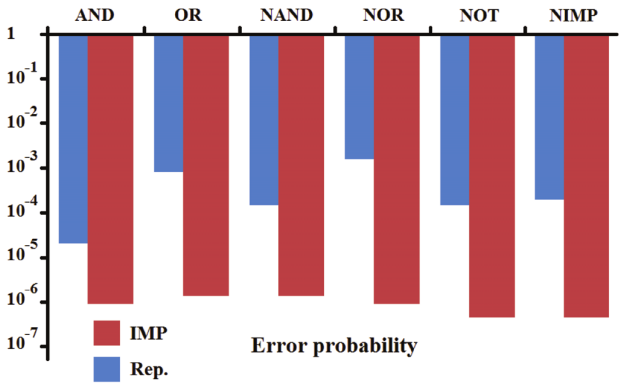

Fig. 5. Minimum error probability of the implication (IMP) and the reprogrammable (Rep.) based implementations of some basic Boolean logic operations.

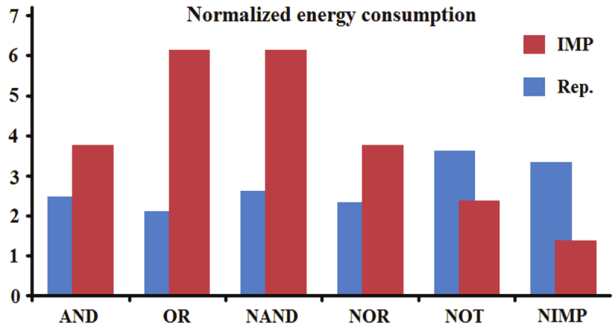

Fig. 6. Normalized energy consumption of the Boolean logic operations shown in Fig. 5. The energy is normalized by the amount of energy required for high-to-low MTJ resistance switching (∼18pJ for $t = 50$ns, based on physical devices characterized in [11]).

$$b_1 \leftarrow a_1 \text{ NOR } a_2 \equiv \{b_1 \leftarrow 0,\ b_1 \leftarrow a_1 \text{ NOR } a_2\}, \tag{8}$$

where $a_{\rm j}$ ($b_{\rm j}$) represents the logic data stored in the $j^{\rm th}$ 1T/1MTJ cell in the input (output) array.

In order to perform a fair comparison, we assume the same device (MTJ and transistor) characteristics for both logic gates and calculate the optimum circuit parameters with respect to their minimum error probabilities of the intrinsic functions (Fig. 3 and Fig. 4). It can be shown that the error probability of a TRUE or FALSE operation is negligible compared to the error probabilities of the conditional switching events required for implementation of the intrinsic functions using implication or reprogrammable gate. Therefore, the same equation (1) is used to calculate the error probability of a more complex Boolean logic function in which $E_{\rm i}$ is the error probability of the $i^{\rm th}$ intrinsic functions and n is the total number of successive conditional switching events based on either implication or reprogrammable gates. Fig. 5 shows the error probabilities for some basic Boolean logic operations using implication and reprogrammable gates with optimized circuit parameters. It illustrates that, even for the intrinsic functions of the reprogrammable gate, the implication logic exhibits about 1-3 orders of magnitude higher reliability than the reprogrammable gate. It is worth mentioning that the AND and the NAND are the most reliable intrinsic functions when using reprogrammable gates.

Fig. 6 shows the energy consumptions of implication- and reprogrammable-based implementations calculated using the Spice model for the STT-MTJs from [12]. Due to the mismatch between the intrinsic logic functions of the gates, the IMP-based implementation requires more energy (by an average factor of ∼1.4) as compared to the reprogrammable-based implementation for the basic Boolean logic operations.

In order to see the performance at larger circuits, we calculated the error probabilities and the energy consumptions of more complex Boolean functions comprising a XOR, a Half Adder, and a Full Adder implemented by implication and

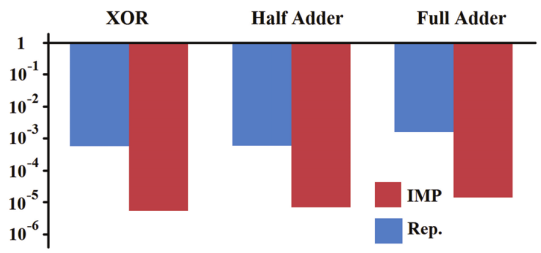

Fig. 7. Minimum error probability of the implication (IMP) and the reprogrammable (Rep.) based implementations of XOR, Half Adder, and Full Adder logic functions. In order to minimize the error probability of the reprogrammable-based implementation, the logic functions are based on AND and NAND operations.

reprogrammable gates. For the reprogrammable gate, we use only AND and NAND operations to provide the most reliable design. For example, although the number of required steps is increased, the following implementation is preferred over (8) in a reliability-based design of the NOR operation:

$$a_3 \leftarrow a_1 \text{ NOR } a_2 \equiv \{b_1 \leftarrow \text{NOT } a_1, b_2 \leftarrow \text{NOT } a_2,\ a_3 \leftarrow b_1 \text{ AND } b_2\}. \quad (9)$$

Fig. 7 shows that the implication-based implementation of more complex functions exhibits about two orders of magnitude higher reliability than the most reprogrammable gates design. Furthermore, for logic functions which are not inherently covered by the gates, e.g. (N)AND, (N)OR for the reprogrammable gate, the implication-based logic also performs better with respect to power consumption (Fig. 8).

IV. Conclusion

A performance analysis and comparison of 1T/1MTJ-based logic implication and reprogrammable logic gates has been presented. It has been shown that for the intrinsic (N)AND and (N)OR operations, the reprogrammable gate requires slightly less power than the corresponding IMP implementation. However, 1T/1MTJ-based implication logic enables a more reliable logic behavior as compared to the reprogrammable gates.

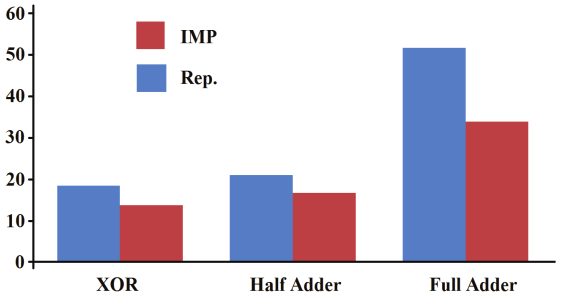

Fig. 8. Normalized energy consumption of the Boolean logic operations shown in Fig. 7.

Furthermore, the IMP implementation outperforms the reprogrammable gate for more complex logic functions and is thus the implementation of choice for large-scale logic circuits.

Acknowledgment

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