Origins and Implications of Increased Channel Hot Carrier Variability in nFinFETs

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***Abstract*—Channel hot carrier (CHC) stress is observed to result in higher variability of degradation in deeply-scaled nFinFETs than bias temperature instability (BTI) stress. Potential sources of this increased variation are discussed and the intrinsic time-dependent variability component is extracted using a novel methodology based on matched pairs. It is concluded that in deeply-scaled devices, CHC-induced time-dependent distributions will be bimodal, pertaining to bulk charging and to interface defect generation, respectively. The latter, high-impact mode will control circuit failure fractions at high percentiles.**

Keywords—FinFETs; Channel Hot Carriers (CHC); Bias Temperature Instability (BTI); Time-Dependent Variability

I. Introduction

Of the MOSFET degradation mechanisms, the variability of Time-Dependent Dielectric Breakdown (TDDB) and Bias Temperature Instability (BTI) in deeply scaled devices has been described with a degree of success [1,2]. In comparison to these cases, Channel Hot Carrier (CHC) degradation is inherently more complex [3,4]. CHC stress is non-uniform, with large currents present, and the resulting degradation is typically localized at the drain, thus offering a wider range of variability sources, as well as potential measurement artifacts. Variability of CHC degradation has been reported previously, mainly in planar devices [5-9]. Here we reexamine this topic in two generations of nFinFET devices and observe that *CHC variability is generally higher than that of BTI, flagging it as the main contributor to time-dependent variability of FinFETs* [10]. We examine in detail several *intrinsic* (random) and *extrinsic* (process-induced, systematic) sources of this increased variability. To aid this procedure, we employ *matched pairs to eliminate extrinsic (process-related) time-dependent variability sources* [11], analogously to time-zero variation [12]. We discuss *the intrinsic variability sources in the defect-centric framework* [2,13] and *provide a blueprint for projecting CHC variability to operating conditions and lifetimes.*

II. Experimental and Methodology

We studied nFinFET devices with (as drawn) gate lengths L_G ranging from 130 nm down to 28 nm, with the number of fins N_{FIN} = 1, 2, 4, and 22, fin widths W_{FIN} = 10 and 20 nm, and fin heights H_{FIN} ~25-30 nm, high-k/metal gates, fabricated in two imec technologies. The total channel area of each device is then $A_G = (W_{FIN}+2H_{FIN})L_G N_{FIN}$. Populations of devices distributed across wafer have been subjected to either CHC or PBTI stress at either room temperature or 125 °C. The initial threshold voltage V_{th0} of each device was obtained from the initial I_D-V_G at fixed I_D. Each device was then separately stressed at elevated V_G and V_D = 50 mV (corresponding to BTI stress) or high V_D (corresponding to CHC stress) for a given duration t_s and the overall threshold voltage shift ΔV_{th} was inferred from ΔI_D at ~1 ms after stress [14]. Devices showing any abnormality, such as increased gate current or the source and drain currents not equal within a specified margin were disqualified. Multiple threshold voltage shifts Δv_{th} due to individual defect-discharging events were also extracted from relaxation traces of the nFinFET devices [15] and analyzed separately.

A. Defect-Centric Statistics and Its Application to Matched Pairs

Together with the mean number of defects per device N_T, the mean impact η of a single charged gate-oxide defect on the FET threshold ΔV_{th} is a crucial parameter of the *defect-centric model* [2,13]. The model provides a fundamental relationship between the first two moments of the ΔV_{th} distribution, i.e., between the mean degradation $\langle \Delta V_{th} \rangle$ and the standard deviation $\sigma_{\Delta Vth}$

$$\eta = \frac{\sigma^2_{\Delta Vth}}{2\langle \Delta V_{th} \rangle}. \quad (1)$$

Because $\sigma_{\Delta Vth}$ increases with progressing device degradation [2], we argue that the time-dependent variability is best described in terms of η [2,11,13,16]. In the following we therefore use this *physically-based* parameter to compare the

variances of degradation. Note the variance is properly normalized in Eq. 1 by the mean degradation $\langle \Delta V_{th} \rangle$, naturally allowing the comparison of conditions with different $\langle \Delta V_{th} \rangle$.

As already discussed in [17], time-dependent variability has *random* (i.e., intrinsic) and *systematic* (i.e., extrinsic) components. In order to allow for a fair comparison, only the *intrinsic* component, free of extrinsic effects, has to be considered. To that end, a novel analysis of Matched Pairs (MPs) is introduced. The methodology is discussed in detail in [11]. The MPs are two FinFET devices laid out in close proximity (~4.2 and ~1.3 µm for the 1st and the 2nd FinFET generation layouts, respectively), each pair thus consisting of left "L" and right "R" devices. Analogously to the analysis of *time-zero* variability using MPs [12], we define the *difference* of the threshold voltage *shifts* of the matched "L" and "R" devices after stress as

$$\delta\Delta V_{th} = \Delta V_{th,L} - \Delta V_{th,R}. \quad (2)$$

Following [11], i.e., *assuming that the systematic component in closely-spaced "L" and "R" devices is identical*, the intrinsic *time-dependent* variance extracted using MPs is

$$\sigma_{\Delta Vth}^2 = \sigma_{\delta\Delta Vth}^2 / 2 \quad (3)$$

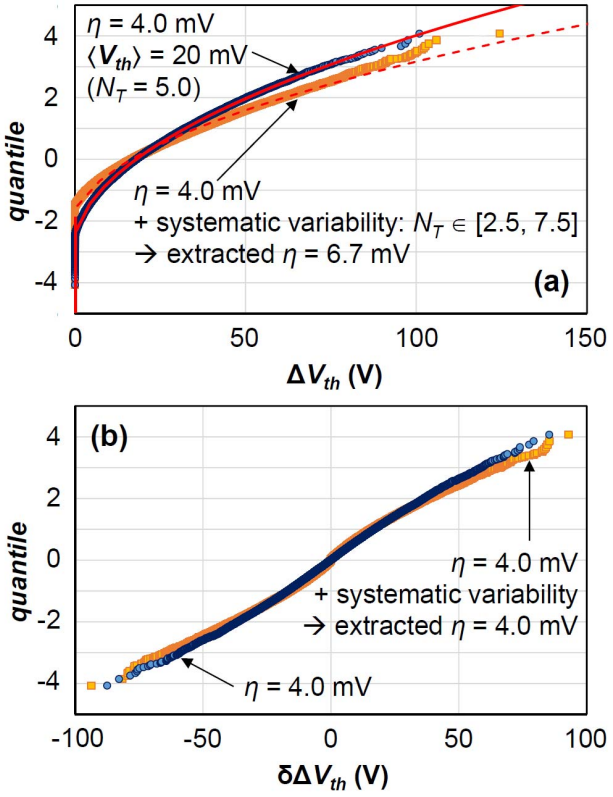

Fig. 1: Probit plots of Monte Carlo simulation of defect-centric distributions in (a) single devices (SD) and (b) matched pairs (MP) [11]. Variance and hence η can be readily extracted from the difference distribution $\delta\Delta V_{th}$ obtained on MPs (b). Note the MP distribution is in general not normal. The *additional systematic variability* in single devices (a), emulated by distributing the mean number of defects N_T across wafer [11], *is fully compensated and the original η is restored* (b).

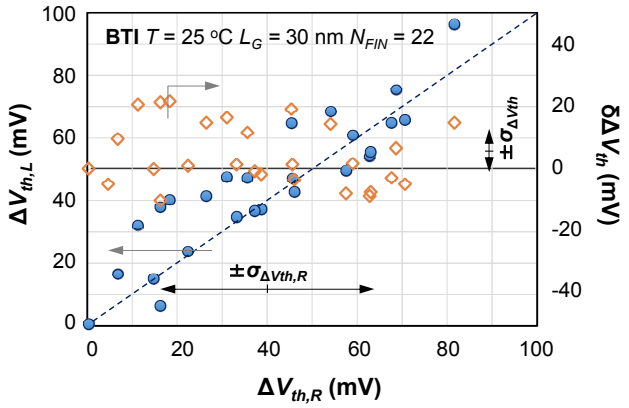

Fig. 2: Illustration of an extreme case of across-wafer variability affecting time-dependent variability due to BTI stress. Note the correlation $\Delta V_{th,L}$ and $\Delta V_{th,R}$ in individual MPs due to the systematic variability (solid circles) and the reduction of variance $\sigma_{\Delta Vth}^2$ when Eq. 3 is used on the MP degradation difference $\delta\Delta V_{th}$ (Eq. 2, open diamonds).

In Fig. 1 we illustrate using a Monte Carlo simulation that *the correct (intrinsic) η can be extracted from the $\delta\Delta V_{th}$ distribution, even if across-wafer process-induced variability is assumed.* Fig. 2 then illustrates the methodology using real nFinFET data.

III. Results and Discussion

The increased spread of CHC degradation with respect to BTI for the same mean threshold voltage shift $\langle \Delta V_{th} \rangle$ is illustrated in Fig. 3. This observation indicates that *the CHC degradation could be the most significant source of time-dependent variability in advanced CMOS technologies.* However, because of the non-uniform nature of the CHC stress and the large currents involved, the increased CHC variability could be easily an artefact of measurement. To correctly understand this increased CHC variability, a thorough discussion of potential sources is required. Several potential sources of the increased CHC variability are identified in Fig. 4.

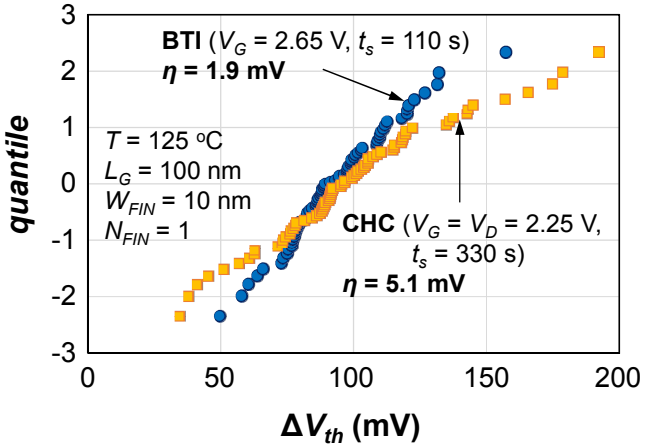

Fig. 3: For the same mean degradation, CHC stress in nFinFETs results in a wider distribution, as compared to uniform BTI stress.

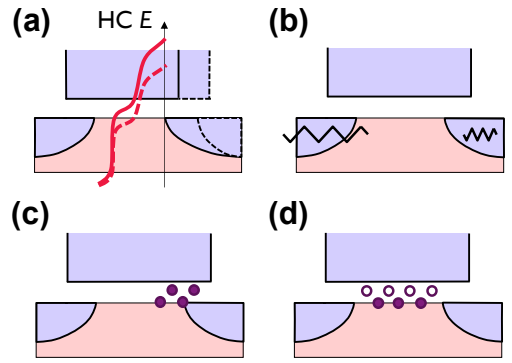

Fig. 4: Sources of increased CHC variability: (a) Channel length/LER and schematic CHC energy distribution, (b) series resistance, (c) longitudinally and (d) vertically non-uniform trapping.

A. Sensitivity to device length and bias variations

Since the CHC energy distribution is an intricate function of the electric field distribution in the device body, a dependence on device length (Fig. 4a) and biases (Fig. 4b) variations can be expected. From CHC $\langle \Delta V_{th} \rangle$ vs. L_G dependence (Fig. 5a) we can readily extract the effect's sensitivity to channel L_G variation to be $s_{LG} \sim 2.5$ mV/nm in our devices. Estimating conservatively the variation in L_G in our devices to be $\sigma_{Leff} =$ 2 nm, the impact on $\sigma_{\Delta Vth}$ is simply

$$\sigma_{\Delta Vth} = s_{LG} \ \sigma_{Leff}. \quad (4)$$

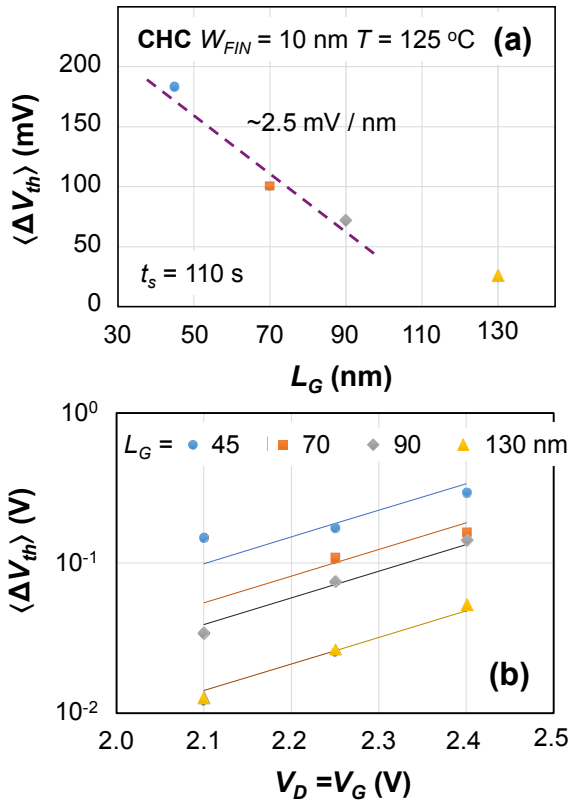

Fig. 5: Sensitivity of CHC to (a) L_G and (b) bias.

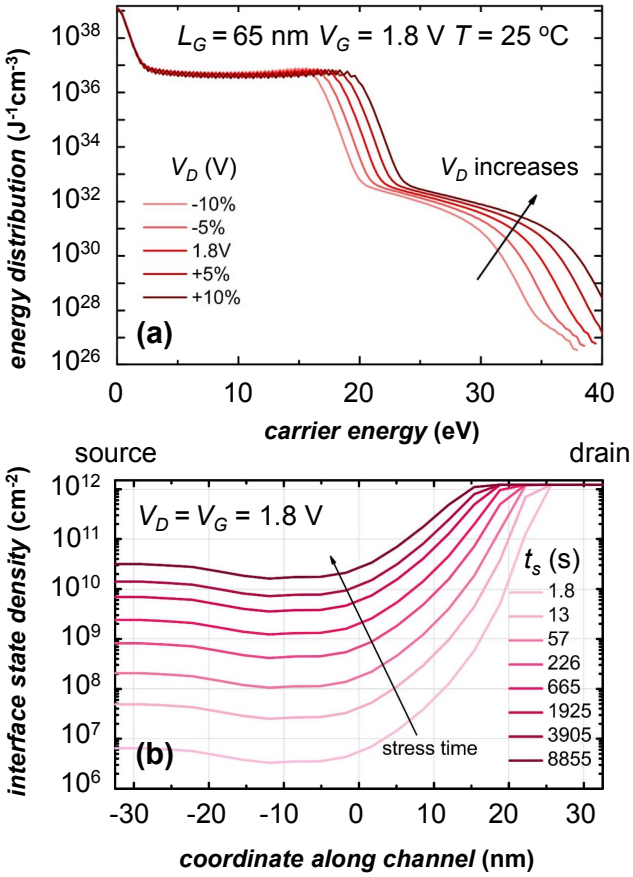

Fig. 6: CHC simulation in a planar device. (a) CHC energy distribution at drain (cf. Fig 4a), responsible for trap generation and charging, is sensitive to drain bias. (b) Increase in CHC degradation along the channel. Note the most damaged region extending ~20 nm from the drain.

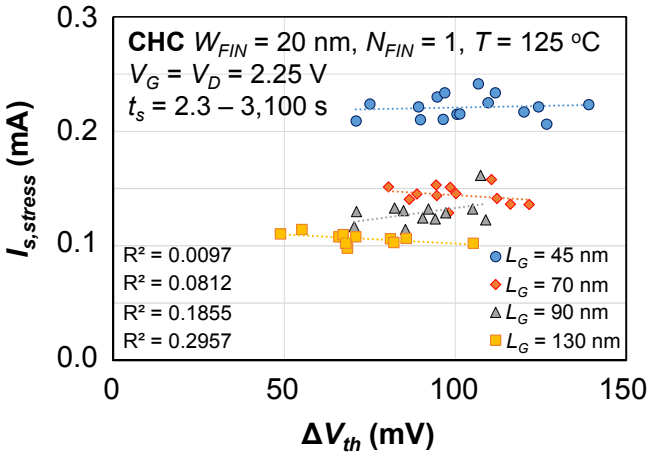

Fig. 7: Channel current during stress is not correlated with degradation (result for $W_{FIN} = 20$ nm shown), disqualifying series resistance as a main source of increased CHC variability. Stress time t_s is adjusted per L_G.

From Eq. 1 we then get $\eta = 0.13$ mV (using $\langle \Delta V_{th} \rangle = 100$ mV, Fig. 5a), suggesting this mechanism is not the main contributor to CHC variability (cf. typical η values in Fig. 3).

Fig. 6a illustrates the sensitivity of CHC energy distribution at the drain to the drain bias V_D (details in [4]). Again from measurements of CHC $\langle \Delta V_{th} \rangle$ vs. V_D (Fig. 5b) we deduce the sensitivity to V_D and can conclude that η is negligible 0.07 mV for σ_{VD} = 10 mV, however, η is considerable 2.2 mV for σ_{VD} = 50 mV. Consequently, device-to-device variations of significant source/drain series resistance (Fig. 4b) could be also responsible for the increased CHC variability. We, however, observe no correlation between channel current during CHC stress and the resulting ΔV_{th} (Fig. 7), as well as similar variability (i.e., η) when CHC is applied with equivalent constant drain *current* (not shown), eliminating this extrinsic source of variability as well.

Regarding the bias sensitivity we finally note that in a real circuit application, V_D and V_G will be varying as the devices are operated and the exact combination of $V_D(t)$ and $V_G(t)$ in each particular device may differ due to the surrounding circuit topology. This circuit-specific effect is expected to add to the already-increased CHC variability.

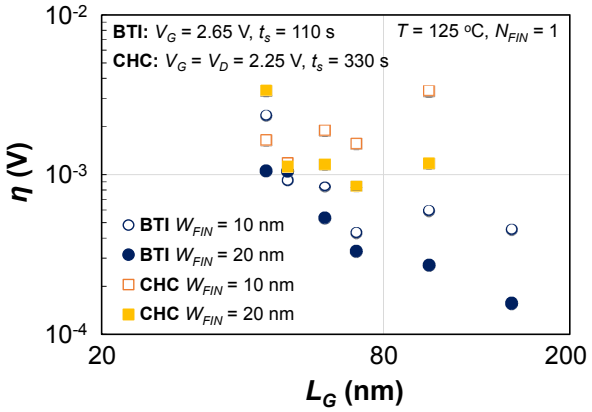

Fig. 8: Gate length dependence of BTI and CHC variability in long nFinFETs, as extracted from MPs (cf. Fig. 1). BTI η dependence follows A_G^{-1} scaling, while CHC η is higher, approx. constant and hence tends to converge at shorter gate lengths.

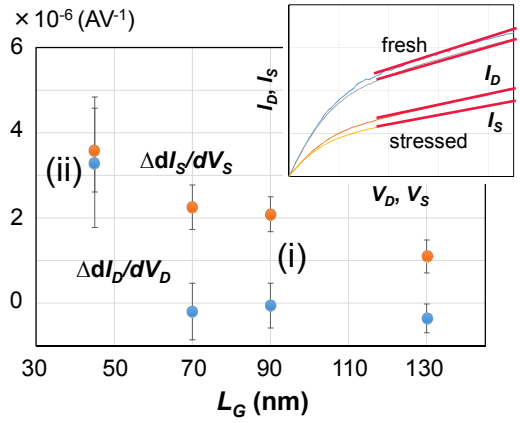

Fig. 9: Change in dI_d/dV_d (dI_s/dV_s) slope after CHC stress (inset) allows visualizing CHC degradation (i) longitudinally localized in longer nFinFETs and (ii) spanning the entire channel in shorter devices. BTI degradation is symmetric at all L_G's (not shown).

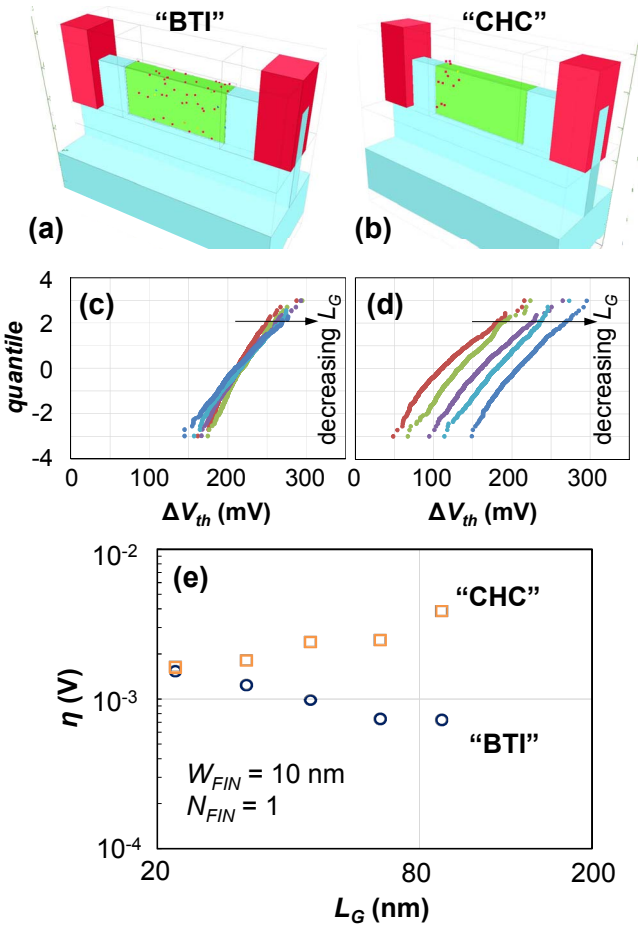

Fig. 10: "Atomistic" TCAD simulation [19] of (a) uniform ("BTI") and (b) localized (20 nm from the drain, "CHC") trapped charge (with constant density) in *synthetic* nFinFETs results in distributions (c) and (d), respectively, as a function of L_G. (a) Values of η calculated through Eq. 1 qualitatively well reproduce measured dependence (open symbols) in Fig. 8.

B. Laterally localized degradation

To resolve the general issue of extrinsic (artefact) variability sources, we introduce matched pairs (MPs) [11] as a means of eliminating extrinsic (process-related) time-dependent variability sources. The method, described in Section II and in [11], is first applied to long, 1st-generation imec FinFETs. Fig. 8 confirms that, even after the elimination of extrinsic components, CHC variability is generally higher than that of BTI. We see that η extracted after BTI stress scales as device area A_G^{-1}, as expected for defects distributed uniformly over the channel [18]. On the other hand, the larger CHC variability is approximately constant and merging with the BTI trend at shorter gate lengths.

This trend can be traced to the CHC degradation localized at the drain (cf. Fig. 4c). As documented in Fig. 9, CHC degradation is asymmetric down to L_G = 45 nm in our devices. This is qualitatively consistent with CHC simulations at V_G = V_D (Fig. 6b), indicating maximum damage ~20 nm from the drain junction into the channel. The CHC vs. BTI trend of Fig.

8 is then qualitatively well reproduced by TCAD simulations [19], see Fig. 10, with uniform ("BTI") and localized ("CHC") trapped charge in the gate oxide, confirming longitudinal localization of damage (Fig. 4e) as a source of increased long-channel nFinFET CHC variability with respect to BTI.

C. *Interface state generation*

Fig. 11 again documents the extraction capability of Matched Pairs for short, 2nd generation devices for both time-zero (Fig. 11a) and time-dependent variability (Figs. 11bc). Again, η after BTI stress scales with A_G^{-1} (Fig. 11b), while *CHC stress again results in higher variability and* η (Fig. 11c).

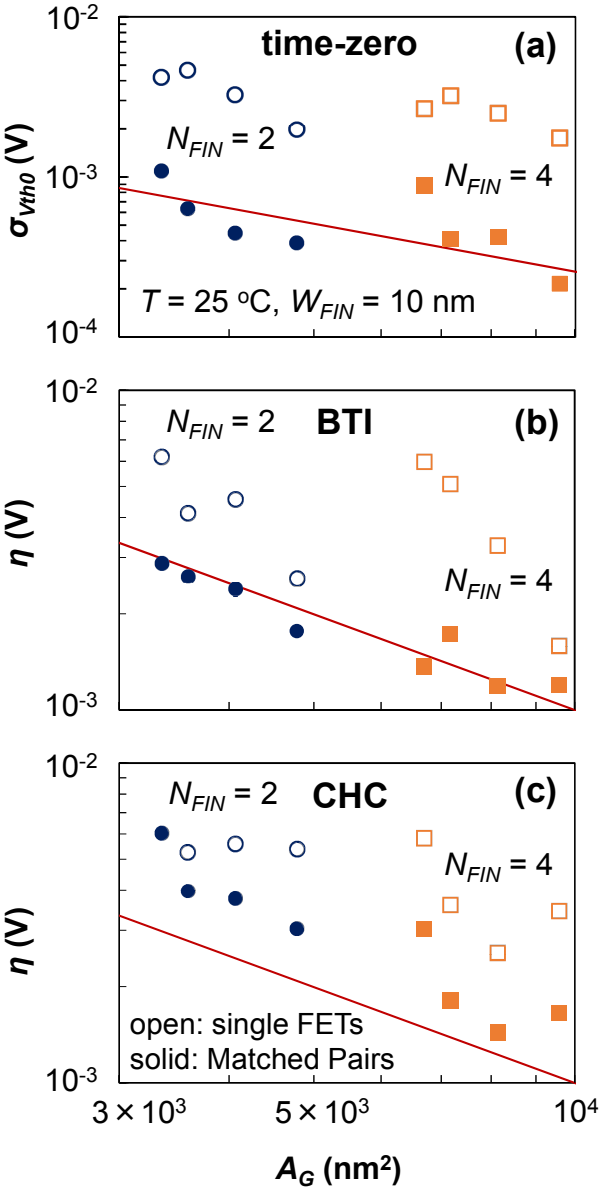

Fig. 11: (a) *Time-zero* variability, represented by σ_{Vth0}, and *time-dependent* variability after (b) BTI and (c) CHC stress, as extracted from *single* short nFinFETs (open symbols) and from *matched pairs* (solid symbols). Unlike single devices, matched pairs yield correct area scaling for both (a) time-zero (lines: $\sigma_{Vth0} \sim A_G^{-1/2}$ [11,12]) and (b) BTI (lines: $\eta \sim A_G^{-1}$ [11,17,21]). (c) CHC stress results in higher variability wrt BTI [fit lines from (b) copied over to (c)] due to defect generation at oxide/substrate (cf. inset of Fig. 13).

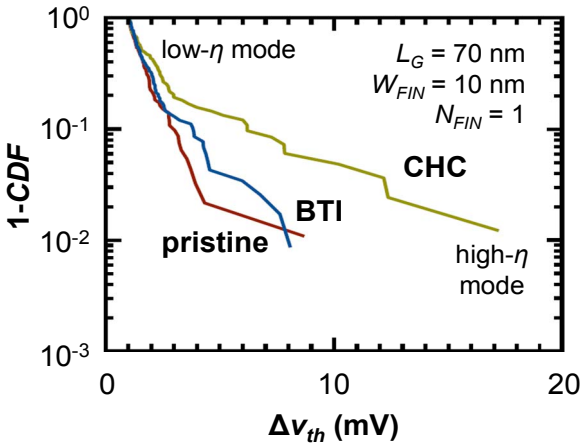

Fig. 12: An example of single-trapping-event Δv_{th} distributions obtained from TDDS measurements [15] show distinct increased defect density close to channel/oxide interface (high-η mode; cf. Fig. 4d) after CHC stress. Low-η mode corresponds to charged defects deeper in the gate oxide.

Compared to PBTI, CHC stress is known to result in significant Si interface defect generation (e.g., ~2×10^{11} cm^{-2} from Charge Pumping on large-area devices of 1st generation FinFETs at applied stress conditions), typically accompanied by a subthreshold slope increase. We conclude that charged defects generated close to/at the substrate [9,20] (cf. Fig. 4d) are the main source of the increased CHC variability in short nFinFET devices. Due to their proximity to the substrate, these charged defects will have a higher impact on the threshold voltage, and will hence correspond to a higher η, which is proportional to charged trap centroid depth in oxide [21,22]. This is also evidenced by TDDS measurements [15] on pristine and previously stressed devices, showing for CHC stress *a high-*η *mode corresponding to defects close to the Si interface* (Fig. 12) [20,23].

IV. Implications

In deeply scaled devices, CHC-generated interface states will superimpose onto BTI and CHC-induced charging of bulk high-k defects, resulting in a *bimodal combined distribution*, illustrated in Fig. 13. Note particularly that the high-impact high-η interface defect mode may not be quantifiable in small populations of devices and for short stress times. After heavier CHC stressing, the high-η interface defects will influence the bulk (i.e., ±2-3σ) of the combined distribution relatively weakly, as is documented in this work and is apparent in Fig. 13. However, the high-percentile tail of the full distribution will be controlled by the CHC-generated high-η defects and may have significant impact on circuit failure fractions.

Consequently, both degradation modes will need to be extracted and their kinetics projected *separately* toward operating/lifetime conditions. This task will be facilitated by *analytic description of multimodal defect-centric statistics,* developed recently and detailed in [24].

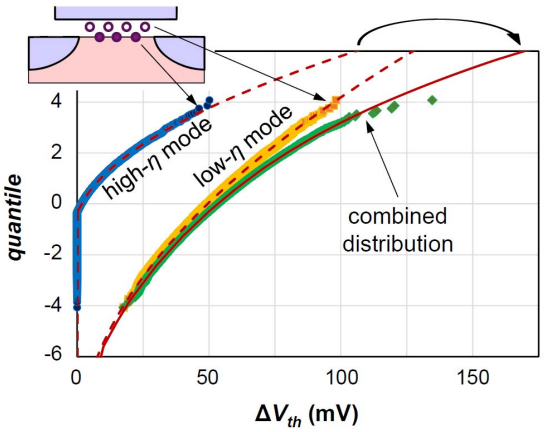

Fig 13: Bimodal defect-centric distribution ΔV_{th} corresponding to CHC stress: Monte Carlo and analytic fit [24]. The high-σ tail of the full distribution is controlled by defects at the substrate (high η; inset: solid symbols).

V. Conclusions

We have observed that CHC stress results in higher variability of degradation in deeply-scaled nFinFETs than BTI stress. Based on the heretofore discussion including careful elimination of potential variability artefacts, we conclude that in *the deeply-scaled nFinFETs the total time-dependent distribution resulting from CHC stress will be bimodal*, pertaining to bulk charging and to interface defect generation, respectively. *Both modes will need to be extracted and their kinetics projected separately* toward operating/lifetime conditions. This task will be facilitated by *analytic description of multimodal defect-centric statistics,* as well as *the use of matched pairs to correct for extrinsic time-dependent variability sources*.

Acknowledgments

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