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Novel Buffered Magnetic Logic Gate Grid

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After many decades of steep progress in semiconductor industry the performance gain due to CMOS scaling will stop in the foreseeable future. This stems from the sharp rise in factory costs and the growing severeness of physical limits.
Power dissipation caused by leakage especially in mobile devices becomes a critical burden nowadays.
A simple way to reduce power dissipation and the total power consumption is to shut down idle circuit parts. However, when these circuits are activated their previous state must be recovered. In order to avoid energy and time consuming recovery cycles non-volatile elements must be added to realize the desired instant ON capability.
Here, spintronics is very appealing due to its non-volatility, fast switching, and high endurance.
Even though some feasible solutions are already available and competitive with respect to energy consumption and speed, e.g. magnetic tunnel junction (MTJ) MRAM [1] and non-volatile CMOS MTJ hybrid circuits [2], they are still not able to challenge pure CMOS with regard to integration density.
The reason is that the spintronic elements (commonly MTJs) are introduced as mere memory, while the actual computation is carried out by CMOS transistors. Therefore, additional transistors are required to read and write the MTJs, which rather leads to a decrease in integration density and power increase.
Therefore, we propose a magnetic non-volatile flip flop [3] and a magnetic non-volatile shift register [4], which perform the actual computation also in the magnetic domain, thus, reducing complexity and allowing extremely small foot prints.
In this work we present an extension of our idea for sequential logic towards a novel non-volatile magnetic logic gate grid facilitating non-volatile magnetic flip flops as buffer as well as shared memory.
The magnetic logic gate grid comprises spin transfer torque (STT) majority gates and the non-volatile flip flops and are positioned at two different levels. The STT majority gates are structurally and operationally compatible with the non-volatile flip flops [5].
The majority gates are arranged in an array and linked to their respective neighbors by the non-volatile magnetic flip flops (see Fig. 1).
This arrangement holds the benefits of a very dense layout, a highly regular structure, allows parallel execution of operations on the logic gates, and minimizes the energy and time spend for information transport. It also supports the shift away from the Von Neumann architecture and its currently performance limiting continuous information flow between physically separated memory and computation units.
Even more, the generic layout of the structure not only eases manufacturing, but also enables, together with the majority gates, highly reconfigureable logic and flexible allocation of employed resources like the number of used gates and buffers depending on the requirements of the task at hand.
In order to illustrate the idea, consider a practical example like a full adder implemented in such a structure. A 1-bit full adder has three inputs A,B,C_{in} and two outputs Sum and C_{out}.
The carry bit C_{out} is defined as Majority(A,B,C_{in}) and the Sum as A XOR B XOR C_{in}.
In a first step Majority(A,B,C_{in}) is calculated and copied into a first flip flop FF1.
Then Majority(A,B,NOT(C_{in})) is calculated and copied into a second flip flop FF2.
Finally Majority(NOT(FF1)),FF2,C_{in}) is calculated by using the results from the previous steps stored in FF1 and FF2 to calculate the Sum, which again is stored in a third flip flop FF3.
One has to note that for a functional complete system negation must be available.
This is realized by inverting the polarity of the applied pulse.
Thus, C_{out} and Sum are calculated via a well defined set of subsequent majority and copy operations in the magnetic domain only. Since C_{out} and Sum are stored in the

flip flops FF1 and FF3 and these are also accessible by neighboring gates their information
can be used for futher processing elsewhere.
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Figure 1

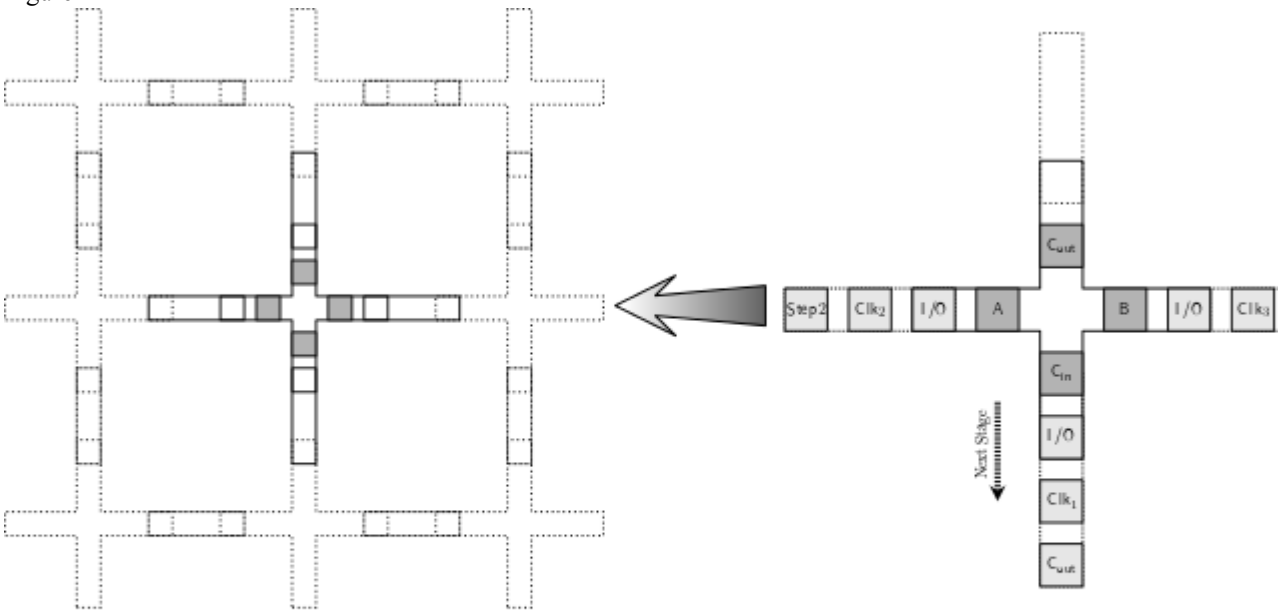

Figure 1: Illustration of the proposed buffered magnetic logic gate gri
and an example for a 1 bit full adder realized with a single majority g
and three flip flops as buffers.